

A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation

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Abstract

We present a sub-nW optical wake-up receiver for wireless sensor nodes. The wake-up receiver supports dual mode operation for both ultra-low standby power and high data rates, while canceling ambient in-band noise. In 0.18 μ m CMOS the receiver consumes 380pW in always-on wake-up mode and 28.1 μ W in fast RX mode at 250kbps.

Introduction

A key component of a truly energy-autonomous wireless sensor node is an always-on wake-up receiver to enable asynchronous wake-up triggered by external interrupt signals at near-zero standby power. RF-based approaches have been widely adopted [1-3] to realize ultra-low power (ULP) wake-up receivers. However the RF frequency oscillator and amplifier limit their energy efficiency to several nJ/bit with high (10s of μ W) standby power. An ULP optical wake-up receiver was proposed with only 695pW power consumption [4]. However, it has a low data rate of \sim 100 bps and lacks a critical capability in optical receivers, namely adaptation to highly variable lighting conditions, which can range from 100s of lux to 100 klux.

Wake-up Receiver Operation Including Noise Cancellation

We present an ULP wireless optical receiver to (re-)program/reset a wireless sensor that enables sub-nW asynchronous wake-up, high data rate data communication, and ambient background light tracking. In order to achieve both ultra-low standby power and high data rates, the proposed receiver employs dual mode operation: 1) Voltage mode for passcode verification at low bit rate: the photodiode voltage is used as the input signal and is directly sensed by a clocked comparator and digital demodulation logic. This approach enables ultra-low power operation by avoiding power hungry analog components. 2) Current mode for fast RX: the diode current is used as the input signal and is sensed by a trans-impedance amplifier to achieve a high bit rate since the effect of diode parasitic capacitance is eliminated. Both modes support a flexible data rate that is dynamically tracked by the clock recovery algorithm employed in the proposed receiver.

A visible light optical receiver is known to be vulnerable to in-band noise from various ambient light sources such as sunlight, incandescent, and fluorescent lighting, resulting in inferior bit rate and sensitivity. Addressing this critical challenge, we propose noise canceling circuitry in both modes, improving bit rate and input sensitivity while enabling operation across 0.3 – 100 klux background light conditions.

Fig. 1 shows the system block diagram of the proposed ULP optical receiver. A 100 \times 100 μ m parasitic photodiode serves as a signal receptor, providing much smaller size compared to a typical inductor/antenna for RF receivers. This enables miniaturization of the entire optical receiver system to the sub-millimeter scale. The fast RX current mode block is power-gated until a valid passcode is successfully verified by matching the on-off keying (OOK) Manchester coded signal to the expected 16-bit passcode. In wake-up mode, the input signal is detected by comparing the diode voltage to a reference voltage (V_{REF}) (Fig. 2). To adapt to different ambient light levels and avoid saturation of the diode voltage, the diode is loaded with a tunable unary-coded resistor bank that consists of 36 off-state medium- V_{TH} transistors with geometric growth. This guarantees a monotonic increase of the resistor value with the selection code (SEL) while covering a background light level from 250 lux to 93 klux (Fig. 3). The use of off-state transistors for diode loading enables a small layout footprint and was previously shown to provide steep light/voltage response [4], thereby improving sensitivity.

Ambient light tracking and pass-code verification operate in parallel using two comparators that each compare the diode voltage to a reference voltage. The ambient light tracking logic searches for the SEL code that has a 50% probability of $D_{OUT_AMB} = 1$ (Fig. 2) and biases the diode output voltage exactly at V_{REF} . Since the underlying modulation is OOK, the light threshold for data detection must reside above the ambient light level. Hence, after the ambient light tracker has tested the light level and updated the SEL code, the selection code is increased by a fixed value (3 in our implementation) for data signal

detection. Fig. 3 shows how the ambient comparison is interspersed between data comparisons. This allows the resistor bank to be reused for both comparators and avoids mismatch issues that would arise if different banks were used for data detection and ambient tracking. At the same time a constant data sampling rate is maintained, which is critical for clock/data recovery. The voltage reference circuit uses two zero- V_{TH} NMOS transistor in series with a SVT PMOS [5] and consumes 50pW. The 50Hz clock is generated using a leakage-based differential thyristor oscillator [6] that also consumes 50pW. The passcode verification block logic uses 3V I/O transistors to achieve ultra-low leakage and hence low standby power.

After successfully verifying the 16-bit passcode, three signals (*power_gate_off*, *oscillator_on*, and *digital_reset*, Fig. 1) are enabled sequentially to power up and initialize the fast RX mode logic. The fast RX mode block consists of analog front-end (AFE) circuitry and digital clock-data-recovery (CDR) logic. The AFE employs a trans-impedance amplifier (TIA) with a DC noise canceling feedback circuit that amplifies the current signal and converts it to a rail-to-rail voltage. The digital CDR logic is synthesized with SVT transistors to support fast decoding speeds. The CDR logic extracts the data as well as the associated clock from the Manchester coded input signal. The AFE contains three amplifiers: 1) the light diode regulation amplifier regulates V_{DIODE} to V_{REF} from the passcode verification block, independent of the light level, 2) the ambient cancelation amplifier ensures the DC value of the V_{SIG} node is the same as the $V_{SIG-REF}$ and generates an adequate gate voltage to sink the DC ambient current to ground, and 3) the post amplifier consists of self-biased cascaded amplifiers to compare V_{SIG} with $V_{SIG-REF}$ and amplify their difference to full rail. A push-pull transistor stage follows the post amplifier to sharpen the data output edge. The fast RX mode CDR circuit is clocked by a current-starved ring oscillator at 2.5 MHz. This CDR circuit takes the signal data stream from the TIA block and generates the decoded *Data* and *CLK* with a flexible data rate (i.e., *CLK* rate) ranging from 0.98 kHz to 250 kHz.

The diode regulation and ambient cancelation amplifiers have an identical two-input cascaded structure, which uses the same three biases generated by the on-chip voltage reference generator (Fig. 4). However, these two amplifiers are sized differently to meet their gain and bandwidth requirements. Decoupling capacitors (C_1 & $C_2 = 3.2$ pF) are inserted for noise-canceling feedback loop stability and also for controlling the bandwidth of the noise cancelation. During fast RX mode, the feedback loop cancels out ambient light noise if the noise spectrum is narrower than the loop bandwidth, which is designed to be 400Hz.

Measurement Results

The proposed design is fabricated in 0.18 μ m CMOS (die photo in Fig. 7) with total area of 0.85mm². Fig. 5 shows the measured waveform of $SEL[35:0]$ and V_{CTRL} signals as the ambient light intensity changes. As expected, $SEL[35:0]$ toggles in steady state and V_{CTRL} tracks the ambient light to cancel the DC noise current. Measured bit error rates (BER) are shown for the fast RX mode using a 3W LED source operating across an ambient light intensity ranging from low office light (500 lux) to full sun (100 klux). The DC noise canceling feedback circuit limits the BER increase to 3.4 \times across 500lux to 100klux at 0.5m TX-RX distance and adapts wide ambient lighting conditions automatically. Minimum required incident power on the 0.01mm² PV diode is 900nW at 850nm wavelength. This enables transmit distance of 25m with a standard 3W LED. The proposed receiver achieves its maximum energy efficiency of 112.5pJ/bit at the highest achieved bit rate, 250kbps. Table. 1 compares the proposed free-space optical receiver to prior work, showing 1.8 \times improvement in standby power, 2700 \times faster bit rate, and 1.25 \times higher energy efficiency.

References

- [1] N. Pletcher, et al., ISSCC, 2008. [2] X. Huang, et al., ISSCC, 2010. [3] D. Y. Yoon, et al., JSSC, 2013. [4] G. Kim, et al., CICC, 2012. [5] M. Seok et al., CICC, 2009. [6] G. Chen et al., ISSCC, 2010.

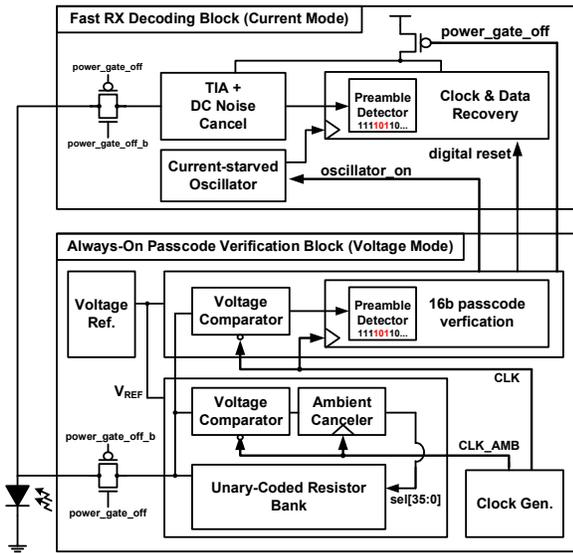


Fig.1 System block diagram

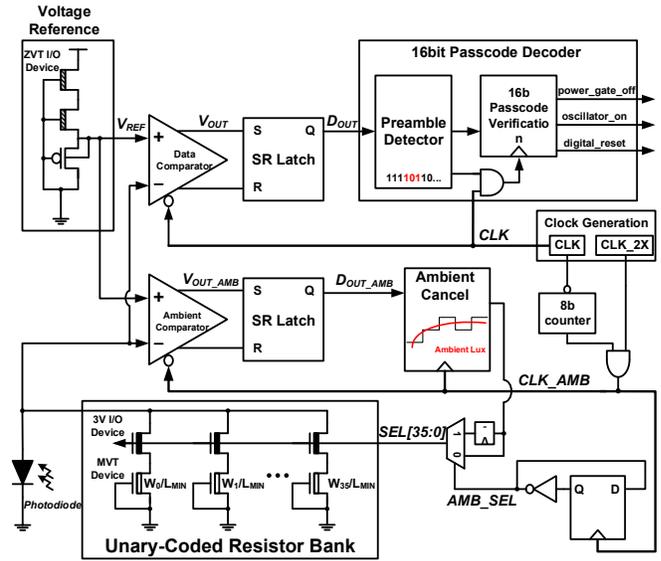


Fig.2 Voltage-mode passcode-verification block diagram

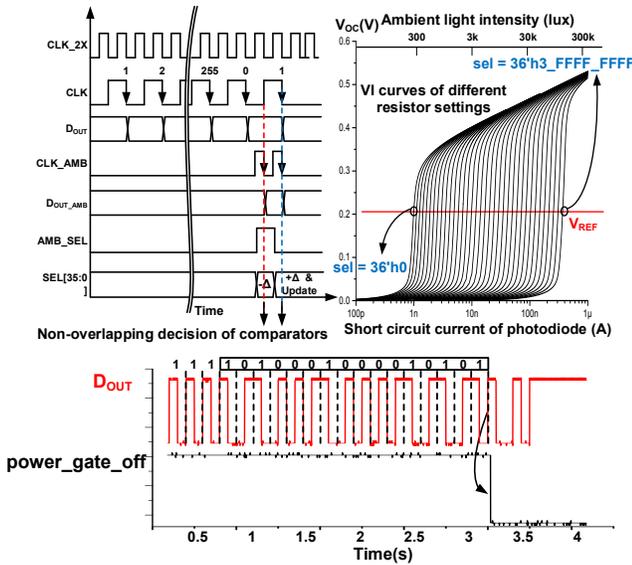


Fig.3 Operation of the passcode-verification block

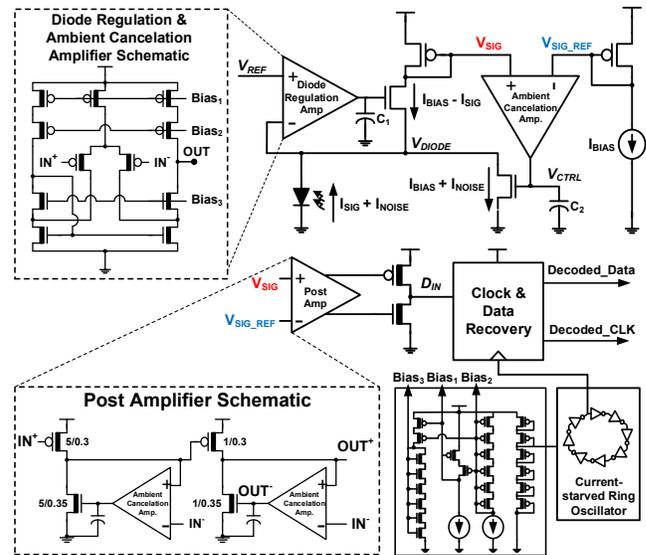


Fig.4 Current-mode fast-RX block diagram

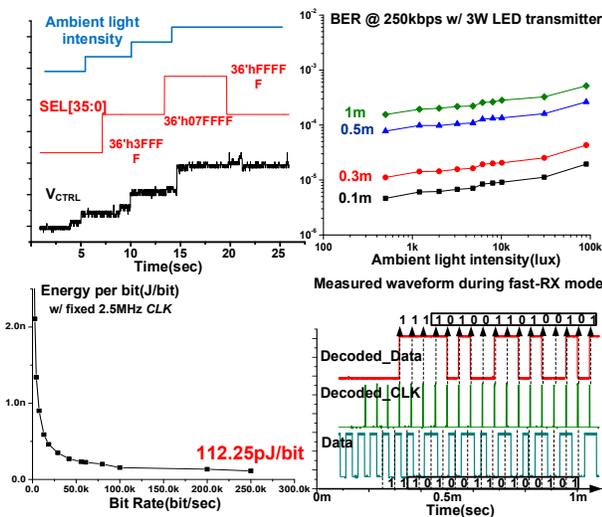


Fig.5 Measured results of fast-RX mode

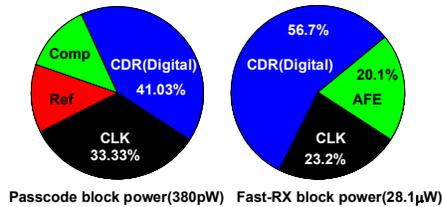


Fig.6 Measured power

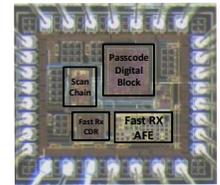


Fig.7 Die Photo

Table 1. Performance summary & comparison

	[1]	[2]	[3]	[4]	This Work
Transmit Method	RF	RF	RF	Optical	Optical
Technology	90nm	180nm	130nm	180nm	180nm
Supply Voltage	0.5V	1.8V	1.2V	1.2V	1.2V
Power	52μW	8.5μW/1078μW	16.4μW/22.9μW	695pW	380pW/28.1μW
Max. Data Rate	100kbps	1k/200kbps	10k/200kbps	91bps	5bps/250kbps
Energy/Bit	0.52nJ/bit	8.5/5.39nJ/bit	1.64/0.11nJ/bit	140pJ/b	80/112.25pJ/b
BER	@-72dBm 10^{-3}	10^{-6}	10^{-5}	10^{-5}	10^{-5}