

A 260 μ W Infrared Gesture Recognition System-on-Chip for Smart Devices

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Abstract

This paper presents a low-power infrared motion detection system suitable for smart devices such as wearables. The SoC incorporates instrumentation chopper amplifiers (ICA), LPFs, ADCs, and a DSP. The low-noise ICAs amplify very low frequency μ V-level thermopile outputs with 2.0 NEF and provide programmable gain modes. To reduce standby power the ICA uses lower current when the system is in idle mode. Wakeup can be triggered by detection of a simple gesture. For the LPF, source degeneration by pseudo-resistors and g_m division techniques are used for both improved linearity and 30Hz bandwidth. The DSP employs a motion history image technique to achieve low-power detection. The system consumes 260 μ W in active mode and 46 μ W in idle mode while processing 16 \times 4 infrared data at 30fps. A complete system demonstration is shown.

Introduction

Recent demand for natural human-computer interfaces such as gesture recognition has increased, particularly for compact wearable devices. Cameras are currently the most common platform for gesture sensing, but they are highly sensitive to environmental light conditions. Extended range capacitive sensing [1] and ultrasonic techniques [2] have been explored but they consume significant energy due to their excitation source. In contrast, an infrared sensing system, in which a thermopile array directly converts incoming infrared radiation energy into electrical energy, is an appealing low-power choice since the sensor array itself is passive. It can be fabricated in CMOS technology and generates voltages linearly proportional to the temperature difference between an object and the background environment [3, 4]. However, array sensitivity is just a few μ V/ $^{\circ}$ C and its time constant is several ms. To achieve ultra-low power gesture recognition, we propose an SoC including a low-noise instrumentation chopper amplifier for low frequency signals, a low-power LPF for filtering out-band noise including the chopper frequency and its harmonics, an ADC, and a motion history image based [5] low-power DSP.

Proposed Gesture Recognition SoC

This paper targets a gesture sensing system using a thermopile array (Figs. 1 and 2). A hand emits infrared radiation with wavelength representing its temperature; this forms an image incident upon a 16 \times 4 thermopile array. Each thermopile signal connects to an AFE path that consists of an ICA and LPF. The four row ADCs digitize the amplified/filtered signals using time-division multiplexing and the DSP then analyzes the waveform to detect gestures.

Fig. 3 shows the proposed ICA. Since the gesture signals are significantly impacted by 1/f noise, they are chopped to remove this 1/f noise and then sent through two amplifiers. Overall gain needs to be up to 80dB for a power-efficient high dynamic range system. C_1/C_2 (15pF/150fF) and C_3/C_4 ($C_4=20$ fF) set the gains for the Low-noise Amplifier (LNA) and Programmable-gain Amplifier (PGA), respectively. C_3 is programmable (200fF–3pF) for system flexibility. OTA_1 and OTA_2 are implemented with inverter-based cascode amplifiers to maximize g_m and gain at a given current. The common-mode feedback (CMFB) amplifiers consume a fraction of the power using ratioed transistor sizes. As in typical noise-limited designs, the first amplifier stage consumes the majority of the total power (up to 2.5 μ A current) to achieve sub- μ V noise while the PGA consumes just 90nA, constrained by the chopper bandwidth. Transistor sizes are chosen for optimal noise efficiency factor (NEF) and chopper frequency is 1kHz. The ICA high-pass corner is set by $(R_3C_3)^{-1}$ in the DC servo loop. R_1 and R_2 paths set the input common mode voltages and cancels the offsets. Fast-settling switches (FS₁₋₃) are selectively turned on to reduce settling time when ICA settings are changed, decreasing the corresponding resistance by 100 \times in simulation.

The ICA outputs show ripple at the 1kHz chopping frequency and

its harmonics. These are removed with the proposed Gm-C LPF in Fig. 4. The two biquads are connected in series to form a 4th order filter. Since the gesture information resides in a low frequency range, the LPF bandwidth is set to 30Hz to achieve high SNR. C_{LPF} is a capacitor array and is set to 8.9pF to approximately match AFE and thermopile pixel size. Considering $f_{LPF3dB}=g_m/(2\pi C_{LPF})$, g_m in the nS range is required. To achieve this bias current must be extremely low, leading to potentially poor linearity. Thus, source degeneration and g_m division techniques [6] are used in the LPF. The Gm-stage input current is divided by the series-parallel current mirror to effectively obtain $g_m/32$. To enhance linearity, input pair sources are degenerated by pseudo-resistors whose gates are controlled by inputs. Simulation results show the resulting g_m is linear within ± 100 mV input range (defined by full width at half-maximum). The CMFB amplifier replicates voltages in the main Gm stage and sets the common mode output voltage. LPF outputs in each row are time-multiplexed via a 16:1 analog multiplexer and connected to a differential 8b SAR ADC (Fig. 5). The ADC sampling rate is 1kS/s.

Fig. 6 describes the overall structure of the proposed motion recognition DSP. There are three separate memories to store frame data. The first memory contains the motion history image (MHI), which is the difference between the current and previous frames (Fig. 7). The second and third memories are used to store two continuous frames once motion is detected. Detection modules use data from the three memories to analyze the gesture. Fig. 8 shows the top level design for the proposed gesture detection algorithm. Motion is detected by counting the number of pixels having significant change in value (i.e., ADC output code) between the current and previous frame. If there is no motion for a period of time the processor goes into an idle mode with only a simpler motion detecting circuit enabled to save power.

When motion is detected, a sweeping algorithm uses two motion history image frames to analyze the motion. In this process each row and column of the MHI frames are first summed. The type of movement (diagonal, up-down, or left-right) is then discerned based on the number of peaks found in the row- and column-wise sums. In a diagonal sweep both row and column sums will exhibit clear peaks (i.e., four total peaks detected) whereas in up-down or left-right sweeps only two peaks are observed due to constant behavior in either the horizontal or vertical direction. This is shown in Fig. 7, which illustrates the principle of detection for sweeping gestures. Up-down or left-right direction can be determined based on the relative positions of negative to positive peaks, as seen in Fig. 7. This approach allows the DSP to accurately identify specific gestures.

Measured Results

The proposed gesture recognition SoC is implemented in 65nm CMOS. The ICA input noise density is 31nV/ \sqrt Hz in active mode and 130nV/ \sqrt Hz in idle mode (Fig. 9), and chopping successfully suppresses 1/f noise. LPF bandwidth is adjustable between 10–150Hz by C_{LPF} changes (Fig. 10). Fig. 11 shows the LPF noise spectrum and HD3 is 48.9dB at $In_{LPF}=0.1$ Vpp. Fig. 12 shows ADC performance. The system is demonstrated with an external 16 \times 4 thermopile and lens, and Fig. 13 shows detection of a hand sweeping across the field of view. Fig. 15 summarizes measured results and compares with recent works. This work represents the first SoC for gesture sensing applications using a thermopile array. Its size (8.1mm², Fig. 14) and power (260 μ W and 46 μ W) are suitable for emerging smart devices.

References

- [1] Yingzhe Hu, ISSCC 2014.
- [2] R. Przybyla, ISSCC 2011.
- [3] M. Hirota, SPIE 2003.
- [4] H. Kawanishi, ISSCC 2008.
- [5] C. Hsieh, ICSPS 2010.
- [6] A. Arnaud, JSSC 2006.
- [7] Qinwen Fan, JSSC 2011.
- [8] Yen-Po Chen, VLSIC 2014.
- [9] P. Bruschi, JSSC 2007.
- [10] S.-Y. Lee, TBCAS 2009.

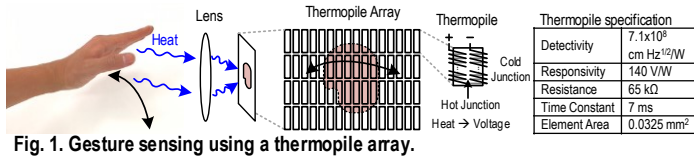


Fig. 1. Gesture sensing using a thermopile array.

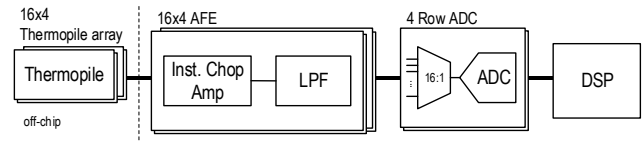


Fig. 2. Block diagram of the proposed gesture sensing system.

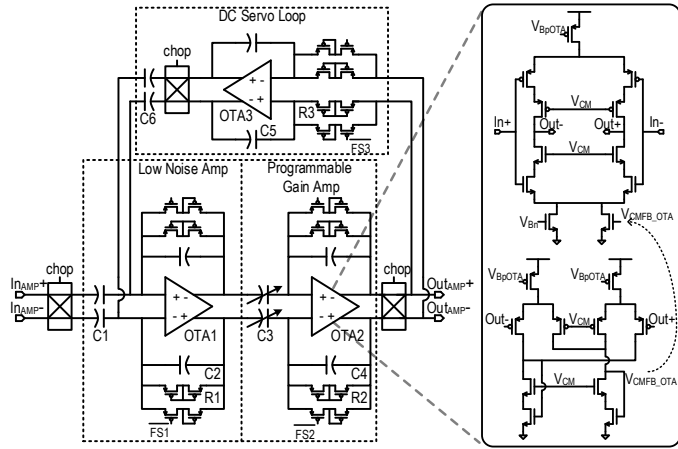


Fig. 3. Proposed low-noise, programmable-gain Instrumentation Chopper Amplifier.

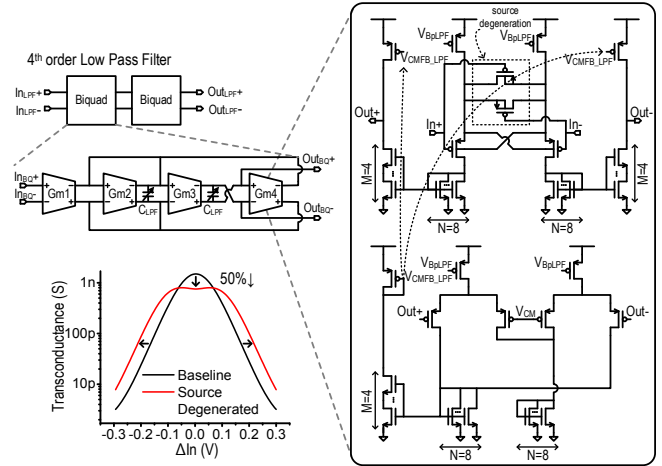


Fig. 4. Proposed 30Hz Gm-C Low Pass Filter.

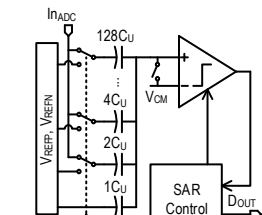


Fig. 5. 8b ADC Implementation.

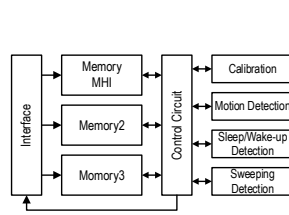


Fig. 6. Gesture detection processor block diagram.

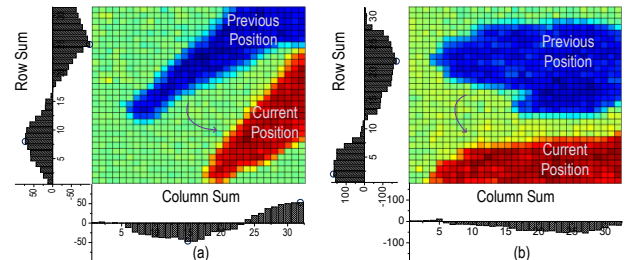


Fig. 7. Motion history image and row- and column-wise sums for a sweep detection (a) diagonal (b) up-to-down (simulated).

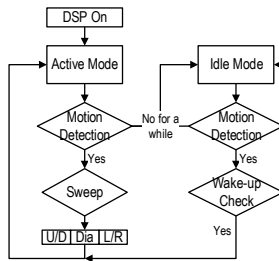


Fig. 8. DSP Detection algorithms.

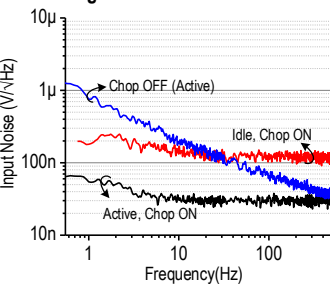


Fig. 9. Measured ICA input referred noise.

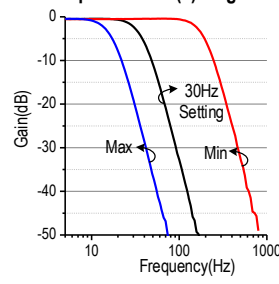


Fig. 10. Measured LPF frequency response across different C_{LPF} .

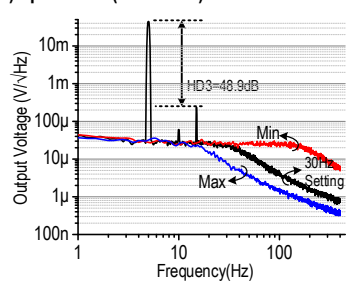


Fig. 11. Measured LPF output noise with different C_{LPF} (0.56-8.9pF).

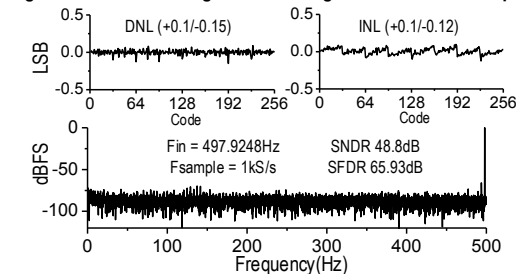


Fig. 12. Measured ADC DNL, INL, FFT results.

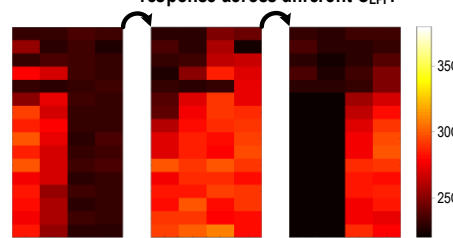


Fig. 13. Motion snapshot (Left to Right sweep)

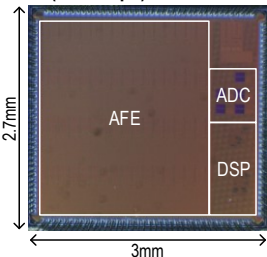


Fig. 14. Die Photo

Instrumentation Chopper Amplifier	This work		[7]	[8]	Low Pass Filter	This work	[9]	[10]	ADC	This Work	System	This Work
	Idle	Active										
Noise (RTI) (nV/√Hz)	130	31	60	59	Cut off Frequency Range (Hz)	10-150	1.5-15	250	Resolution (bit)	8	Technology	CMOS 65nm
Gain (dB)	57.2-78.3		40	41.8-59.2*	THD (%) @ In_{LPF} (Vpp)	0.55 @0.1	1 @1	0.4 @0.1	SNDR (dB)	48.8	FPS	30
Chopping Frequency (kHz)	1		5	4.8, 12**	HD3 (dB) @ In_{LPF} =0.1Vpp	45.5	N/A	48.9	Max INL (LSB)	0.12	Active Power (μW)	260
Current (μA)	0.277	2.655	1.8	0.266	Current (μA)	0.14	550	0.45	Power (μW)	0.06	Idle Power (μW)	46
CMRR (dB)	>130		134	89	Gain (dB)	-0.5	0	-10.5	Sampling rate (kS/s)	1	Active Power/ch (μW/ch)	4.06
PSRR (dB)	>130		120	92	Integrated Noise (RTI) (μVrms)	154***	320	340	DSP		Idle Power/ch (μW/ch)	0.72
NEF	2.7	2.0	3.3	1.4	Order	4	2	5	Power (μW)	5	*open loop gain	
Area (mm ²)	0.04	0.1	0.25		Area (mm ²)	0.04	0.34	0.13	Clock Frequency (kHz)	4	**multi chopper n=3	
VDD (V)	1.4	1	1		VDD (V)	1.4	3.3	1	VDD (V)	0.7	***measured at 30Hz BW setting	

Fig. 15. Performance summary and comparison with prior works.