A 1.02nW PMOS-Only, Trim-Free Current Reference with 282ppm/°C from -40°C to 120°C and 1.6% within-Wafer Inaccuracy

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***Abstract*— A 1.02nW current reference is designed with only PMOS transistors, thereby providing inherently low process variation and enabling trim-free operation. Thirty-two measured chips from 5 corner wafers in 180nm CMOS technology show an untrimmed within-wafer spread (σ/μ) of 1.6% and across-corner wafer-to-wafer spread of ±4.7%. The measured average temperature coefficient is 282ppm/°C from −40°C to 120°C while generating a 35nA reference current. Total untrimmed uncertainty due to variations of process, voltage, and temperature is about 8.8%.**

I. Introduction

Current references are fundamental elements in IoT devices used to set the operating conditions of analog/mixed-signal blocks. IoT devices demand low-power, nano-ampere range current references that operate reliably under a wide range of environmental conditions (i.e. temperature and supply voltage). Conventional beta-multiplier current references require very large polysilicon resistors or resistor-like MOSFET [1] to generate a nA-reference current, incurring substantial area overhead. Sub-threshold current reference [2] using both NMOS and PMOS suffers from process variation and limited temperature range due to inaccurate leakage models at high temperature, particularly for Nwell leakage. This leads to high post-fabrication calibration costs to tighten the distribution of the generated reference current. Also, non-volatile memory is required to store the trimming information, adding fabrication and area costs.

This paper proposes a low-power PMOS-only current reference regulating 35nA output with only 1.02nW power consumption in 180nm CMOS technology. An average temperature coefficient of 282ppm/°C is achieved across a wide temperature range (−40°C to 120°C). By using only PMOS transistors, the reference has inherently low process variation. The untrimmed within-wafer σ/μ is 1.6%, and the untrimmed difference across split-wafers is only ±4.3%. The total uncertainty across process, voltage, and temperature (PVT) variations without trimming is 8.8%, making it well-suited to low-cost, ultra-low-power IoT systems.

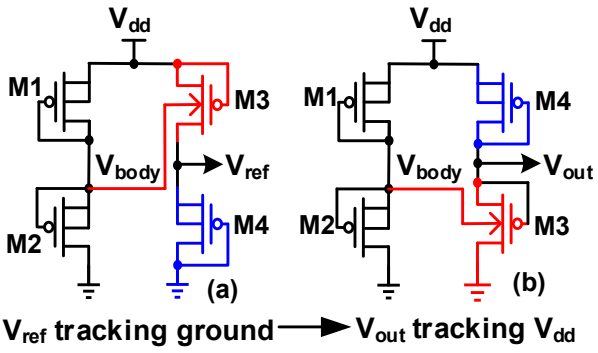

Fig. 1. Voltage generation circuits for ground tracking (a) [3] or V_{dd} tracking (b) by swapping M3 and M4.

II. Current Reference Design

The proposed current reference is based on a V_{th}-based voltage reference design that we previously proposed [3]. In this voltage reference, shown in Fig. 1(a), an off-state M2 and diode M1 provide the required body bias for M3 to generate considerable amount of supply-insensitive sub-threshold current flowing through the bottom PMOS diode M4. With proper sizing of the four PMOS transistors M1/M2/M3/M4, the first-order temperature dependency of the generated reference voltage V_{ref} can be cancelled out. V_{ref} is insensitive to V_{dd} while tracking the ground voltage.

By swapping the positions of M3 and M4 as shown in Fig. 1(b), the generated V_{out} can instead track V_{dd}, maintaining a constant V_{dd}-V_{out}. As shown in Fig. 2, we use this V_{out} to control the gate voltage of a PMOS M5. As shown in Fig. 3, both V_{out} and V_{body} track V_{dd} and therefore V_{dd}-V_{out} is kept constant when V_{dd} is higher than 1.4V. Since V_{dd}-V_{out} is constant, $|V_{gs5}|$ of M5 is supply insensitive (Fig. 3) and I_{ref} (M5 drain current) has very weak sensitivity to V_{dd}.

Current reference I_{ref} has to be insensitive to both power supply and temperature. Proper sizing of M1/M2/M3/M4 is necessary to compensate for the temperature coefficient of I_{ref}. The current equations of M1/M2 and M3/M4 are expressed as (1) and (2), respectively, below:

$$I_L = u_p C_{ox} \frac{W_1}{L_1} nV_T^2 \, exp\left(\frac{(V_{dd}-V_{body})/x - V_{th1}}{mV_T}\right) = u_p C_{ox} \frac{W_2}{L_2} nV_T^2 \, exp\left(\frac{0-V_{th2}}{mV_T}\right) \quad (1)$$

$$I_R = u_p C_{ox} \frac{W_4}{L_4} nV_T^2 \, exp\left(\frac{(V_{dd}-V_{out})/y - V_{th4}}{mV_T}\right) = u_p C_{ox} \frac{W_3}{L_3} nV_T^2 \, exp\left(\frac{0-V_{th3}}{mV_T}\right) \quad (2)$$

By solving (1) and (2), V_{gs5} can be expressed as (3):

$$|V_{gs5}| = y\gamma\left(\sqrt{2\phi_b - |V_{gs5}| + xmV_T \ln\frac{W_2L_1}{W_1L_2}} - \sqrt{2\phi_b}\right) + ymV_T \ln\frac{W_3L_4}{W_4L_3} \quad (3)$$

in which x and y are the stage number of M1 and M4, respectively. By properly selecting values for x and y, $|V_{gs5}|$ can be biased close to the zero temperature coefficient (ZTC) voltage of M5's saturation drain current. This minimizes the temperature coefficient of I_{ref} in first order.

$$I_{ref} = u_p C_{ox} \frac{W_5}{L_5} (|V_{gs5}| - V_{th5})^2 \quad (4)$$

Equation (4) describes I_{ref} in the saturation region. Because PMOS mobility μ_p is complementary to temperature and determines the temperature dependence of drain current in saturation region, $|V_{gs5}|$ must be slightly proportional to temperature for second order compensation. In equation (3) if $W_3L_4 > W_4L_3$, the temperature dependence of the right term is positive; otherwise it is negative. A similar trend holds for the left term containing W_2L_1/W_1L_2 in the square root. Therefore, sizing PMOS transistors M1/M2/M3/M4 allows tuning of the temperature dependence of $|V_{gs5}|$ to a slightly proportional value (PTAT) that minimizes the overall temperature coefficient of I_{ref}.

The proposed design has 4 PMOS widths and lengths for a total of 8 parameters which need to be determined. Therefore, it's too hard to decide the transistor size using hand calculation. A global optimization flow is proposed to find the optimum sizes to compensate temperature sensitivity and power consumption, as shown in Fig. 4.

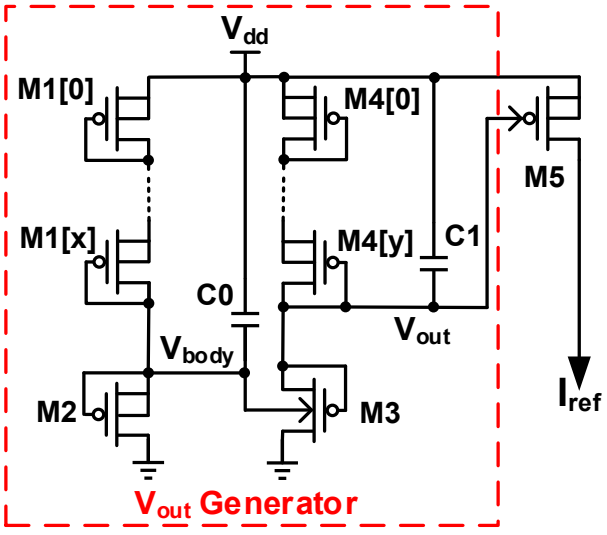

Fig. 2. Schematic of the proposed design with stacked M1s and M4s. C0 and C1 are added to weaken the impact of high-frequency power supply noise.

Fig. 5 shows the simulated waveform of V_{out}, V_{body}, and V_{gs5} with temperature ranging from -40˚C to 120˚C. $|V_{gs5}|$ is close to the ZTC voltage with a slightly positive temperature correlation for second-order compensation of saturation output reference current.

Global process variation is suppressed due to the exclusive use of PMOS transistors. And local mismatch is minimized by upsizing all transistors (>10μm^2) in this design. Two 1.78pF MIM capacitors C0 and C1 are added at nodes V_{body} and V_{out}, respectively, in order to weaken the impact of high-frequency power supply noise as shown in Fig. 2.

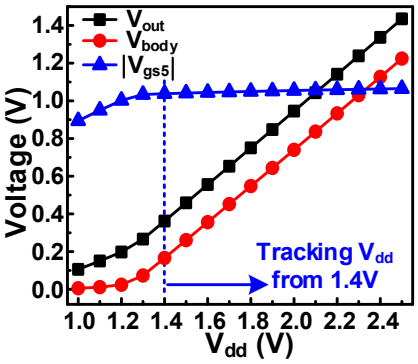

Fig. 3. Simulated V_{out} , V_{body} and $|V_{gs5}|$ tracking V_{dd} change at $V_{dd} > 1.4V$.

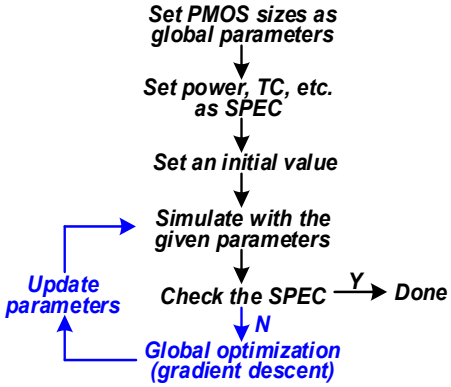

Fig. 4. Design flow of global optimization.

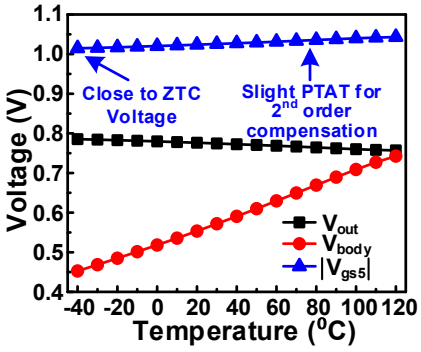

Fig. 5. Simulated V_{out}, V_{body} and $|V_{gs5}|$ across temperature.

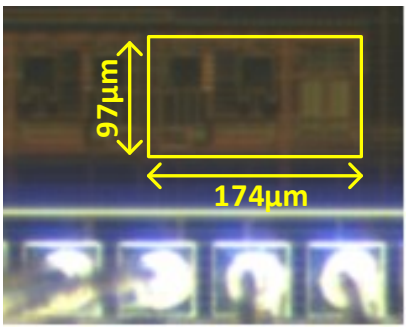

Fig. 6. Die Photo in 180nm CMOS technology.

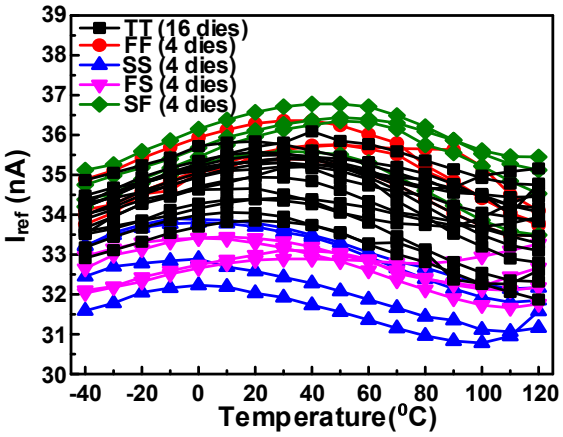

Fig. 7. Measured I_{ref} across temperature for 5 wafers in 5 different corners.

III. Measurement Results

The current reference is validated with a 180nm CMOS test chip. Fig. 6 shows the die photo. The area of the proposed circuit is 16878µm^2 (97µm x 174µm).

Measurements include 32 chips from 5 wafers, including one at TT corner (16 dies) and four corner wafers (4 dies for each of FF, SS, SF, and FS). Fig. 7 shows measured I_{ref} across temperature without trimming for all 32 chips.

Fig. 8(a) illustrates the temperature coefficient distribution of the 16 chips at TT corner. The average temperature coefficient is 282ppm/˚C without trimming. The average I_{ref} at room temperature for 16 chips is 35.02nA with 0.594nA standard deviation (Fig. 8(b)), which is 1.6% σ/µ for within-wafer variation.

Fig. 9 shows the measured average I_{ref} at each temperature point for different corners. With higher PMOS threshold voltage (TT, SS, FS), second order temperature compensation is observed at ~100˚C, extending the working temperature range.

The average temperature coefficient at TT, SS, and FS corners are all below 300ppm/˚C; while FF and SF corners have slightly worse untrimmed temperature coefficient (Fig. 10(a)). The average I_{ref} at room temperature has ±4.7% difference across the corner wafers (Fig. 10(b)).

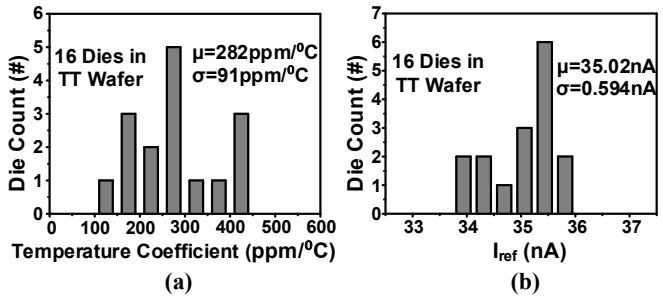

Fig. 8. Measured distribution of temperature coefficient (a) and I_{ref} (b) of 16 dies in TT wafer.

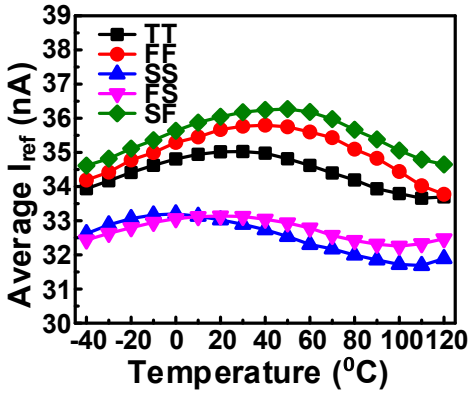

Fig. 9. Measured average Iref across temperature for 5 corner wafers.

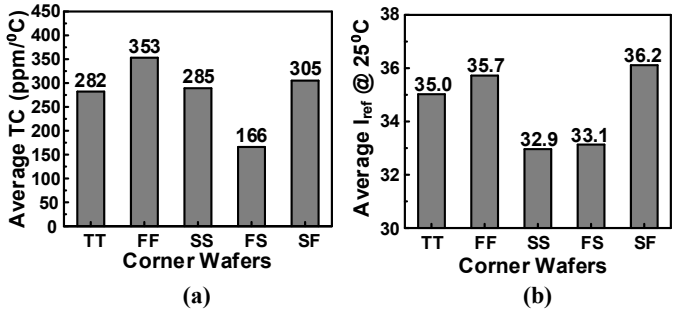

Fig. 10. Measured average temperature coefficient (a) and Iref (b) in each corner wafer.

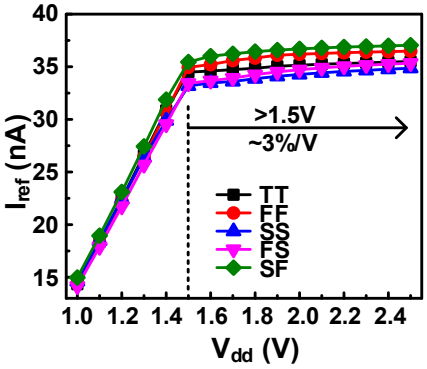

Fig. 11. Measured line sensitivity for 5 corner wafers.

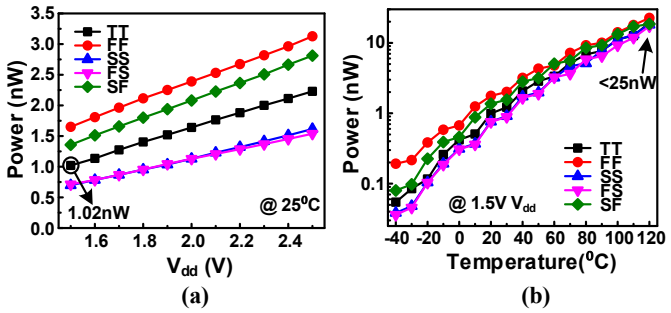

Fig. 12. Measured power consumption across V_{dd} (a) and temperature (b) for 5 corner wafers.

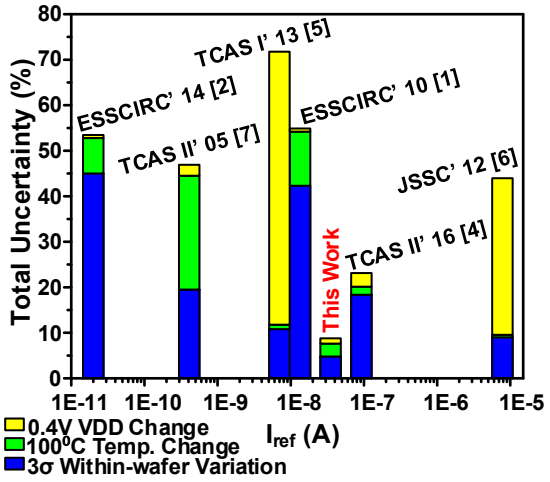

Fig. 13. Accumulated uncertainty comparison with other works.

Table I. Comparison Table to related works.

	This Work	[1]	[4]	[5]	[6]
Technology (nm)	180	350	180	350	180
V_{dd} (V)	> 1.5	> 1.3	> 1.25	5	> 1
I_{REF} (nA)	35	9.95	92.3	9	7810
Power (nW)	1.02	88.5	670	4171	1400
Temperature Range (°C)	-40 ~ 120	-20 ~ 80	-40 ~ 85	0 ~ 80	0 ~ 100
TC (ppm/°C)	282 (146 ~ 428)	1190	177	57	24.9
Line Regulation (%/V)	3	0.046	7.5	150	86 [1]
Within-wafer Variation (σ/μ)	1.6%	14.1%	6.1%	3.6%	3% [2]
Wafer-to-wafer Difference	± 4.3% [3]	N/A	N/A	N/A	N/A
Trimming	No	No	N/A	N/A	No
Chip Area (mm)	0.017	0.12	0.0013	0.0081	0.023
Samples	32 from 5 corner wafers	15 from 1 wafer	10 from 1 wafer	3 from 1 wafer	10 from 1 wafer

[1] Value w/o BGR, extracted from Fig. 10(a)
[2] σ is estimated according to ± 4.5% I_{ref} difference
[3] Difference among corner wafers

Measured line sensitivity is approximately 3% for Vdd above 1.5V (Fig. 11). Fig. 12(a) shows the measured power across Vdd at room temperature. At 1.5V, the proposed circuit consumes 1.02nW in TT corner at room temperature. In the worst corner (FF), power remains below 1.7nW at 1.5V. Furthermore, even at 120˚C, power consumption is below 25nW across all corners (Fig. 12(b)), which is sufficiently low for many IoT applications.

Fig. 13 shows accumulated uncertainties due to PVT variations of state-of-the-art current references. As to the proposed reference, the spread (3σ/μ) of untrimmed reference current due to within-wafer process variation is ~4.8%. The reference current also sees 2.8% and 1.2% variations, due to 100˚C temperature change and 0.4V supply voltage change, respectively. Therefore, the total PVT-induced uncertainty is ~8.8% for this work, which is the smallest among relevant works. Table I summarizes measured results of the proposed current reference and compares them with previous works.

IV. Conclusion

This paper presents a 1.02nW current reference using only PMOS transistors, which can provide inherently low process variation and enable trim-free operation. According to measurement results of 32 chips from 5 corner wafers in 180nm CMOS, the untrimmed within-wafer σ/μ is 1.6% and across-corner wafer-to-wafer difference is ±4.7%. The output reference current is 35nA with an average temperature coefficient of 282ppm/°C from −40°C to 120°C. Total untrimmed uncertainty among process variation, voltage, and temperature is ~8.8%.

References

[1] T. Hirose, Y. Osaki, N. Kuroki and M. Numa, "A Nano-Ampere Current Reference Circuit and its Temperature Dependence Control by using Temperature Characteristics of Carrier Mobilities," IEEE European Solid-State Circuits Conference 2010, pp. 114-117.

[2] M. Choi, I. Lee, T. Jang, D. Blaauw, and D. Sylvester, "A 23pW, 780ppm/°C Resistor-less Current Reference Using Subthreshold MOSFETs," IEEE European Solid-State Circuits Conference 2014, pp. 119-122.

[3] Q. Dong, K. Yang, D. Blaauw, and D. Sylvester, "A 114-pW PMOS-Only, Trim-Free Voltage Reference with 0.26% within-Wafer Inaccuracy for nW Systems," IEEE Symposium on VLSI Circuits 2016, pp. 98-99.

[4] S. S. Chouhan, and K. Halonen, "A 0.67-μW 177-ppm/◦C All-MOS Current Reference Circuit in a 0.18-μm CMOS Technology, IEEE Transaction on Circuits and Systems II, vol. 63, no. 8, pp. 723-727, Aug. 2016.

[5] H. Kayahan, O. Ceylan, M. Yazici, S. Zihir, and Y. Gurbuz, "Wide Range, Process and Temperature Compensated Voltage Controlled Current Source," IEEE Transaction on Circuits and Systems I, vol. 60, no. 5, pp. 1345-1353, May 2013.

[6] J. Lee, and S. Cho, "A 1.4-μW 24.9-ppm/°C Current Reference With Process-Insensitive Temperature Compensation in 0.18-μm CMOS," IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2527-2533, Oct. 2012.

[7] E. Camacho-Galeano, C. Galup-Montoro, and M. Schneider, "A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology," IEEE Transaction on Circuits and Systems II, vol. 52, no. 2, pp. 61-65, Feb. 200