24.3 A 36.8 2b-TOPS/W Self-Calibrating GPS Accelerator Implemented Using Analog Calculation in 65nm LP CMOS

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Many signal processing applications involve manipulating a large amount of data to generate a relatively narrow numerical result, such as, "does a particular object X exist in a picture?", "which of several possible words was spoken in a sentence?", or, "how strongly do these two patterns correlate?". These applications take in noisy inputs with relatively low quantization, such as 8-bits/color for video, or 8-bit audio samples, or 1b-to-2b digitized baseband signals. However, a sufficiently large amount of data allows noise rejection, and an accurate answer can be computed. This large-data-to-narrow-result property makes these applications a good fit for analog calculation, which also has limited resolution and inherent noise, but can offer higher energy efficiency than digital implementations.

A GPS acquisition engine is implemented, which is a prime example of a large-data-to-narrow-result application. In GPS, the goal is to discover the precise timing of a CDMA signal from a baseband signal originally received below the noise floor; this is achieved by comparing hundreds of thousands of 2b numbers in order to generate a single correlation result. The generated correlation result reflects the likelihood with which the target signal was broadcast at a particular time offset relative to the received signal. By searching thousands of possible time offsets the speed-of-light delay to the broadcasting satellite can be measured accurately. While tracking already acquired satellites is a relatively energy efficient process, the initial search and synchronization (*i.e.*, signal acquisition) requires a very large number of calculations (10-to-350 billion MAC instructions per civilian satellite, and up to 35 trillion per military satellite) making it both energy intensive (19-to-665mJ) and time consuming (10-to-350ms). Due to inference, multipath, and obstructions, satellites are frequently lost and the acquisition process often must run continuously in the background, creating the need for low power, high performance GPS acquisition accelerators.

The accelerator implemented in this paper uses analog computation to acquire a GPS satellite with the performance and scalability of a digital implementation and the energy efficiency of an analog implementation. Calculations are performed by converting digitally stored inputs into currents that are summed on differential wires spanning the entire matched filter. In addition, we take advantage of the fact that the correlation result has a very narrow dynamic range (typically between 48.5-to-51.5% of the total possible range), which allows us to use strong amplification of the current difference to produce high resolution (0.5% per LSB) without amplifier saturation. As a result, the matched filter achieves an efficiency of 36.8 TOPS/W, which is approximately 67× higher efficiency than previous high-performance accelerators, while maintaining similar performance.

To search for correct alignment, GPS receivers use a parallel matched-filter topology (Fig. 24.3.1). This process involves two sets of data: the original pattern (*i.e.*, spreading code) broadcast by the satellite and the data received from the antenna. To perform a time-domain search one of these datasets is loaded into the correlation cells and kept in place, while the other is shifted past. At each shift, a correlation is performed by element-wise multiplying the two datasets with each other and then summing the results. The RF signal is quantized at 1 or 2 bits since there is little SNR gain beyond 2 bits [1]. Due to low quantization the multiplication can be implemented using a small number of gates, hence the main challenges include efficient dataset storage/shifting and efficient addition. For example, adding 4096 2b numbers in an all-digital implementation requires at least 8168 full adders in a 15-stage tree that spans the entire storage array, creating routing and interconnect challenges.

Figure 24.3.2 depicts the floorplan with 4096 cells arranged into four banks, a 3b ADC, one fully differential amplifier, one common mode (CM) amplifier, and one sample-and-hold circuit. Each cell contains 4b of storage for RF data (2b for in-phase data and 2b for quadrature data), a 1b shifter to save and move the search pattern, and three current sources that each steer current to either the positive or negative current sum line. These three current sources can represent the four values from the 2b multiply of the RF data and search pattern (PPP=3, PPN=1, PNN=–1, NNN=–3). Since the cells are identical and connect only to adjacent cells and the two current sum lines, they are implemented as a tiled design, enabling a compact floorplan.

To perform one calculation, either the 2b in-phase or 2b quadrature data is selected in each cell and then digitally multiplied with the 1b pattern. The result is decoded and sent to the three current sources that steer current to one or both of the current sum wires. Two opamps are responsible for canceling these currents and holding the two current sum lines at a fixed voltage (Fig. 24.3.3). The CM opamp sets the common mode of CURRENT_SUM_POS/NEG while the equalizing opamp equalizes the two wires and develops a measurement voltage via feedback resistors. The CM opamp is responsible for efficiently canceling the majority of the current from the cells, allowing the equalizing opamp to be designed for generating large measurement voltages across the feedback resistors at a high bandwidth. A sample and hold is inserted between the equalizing opamp output and the ADC to provide a pipeline stage, improving performance.

The entire matched-filter can be calibrated via the ADC, which is a 3b flash with digitally controlled offsets. In calibration mode the bank is made to generate sample inputs to the analog computation chain to calibrate the ADC. The ADC offsets are then adjusted for each bit until they trigger at the appropriate level. The sample inputs from the bank are generated by using the override muxes (Fig. 24.3.2) to force the differential current sources to a known state that simulates various degrees of correlation. This strategy calibrates for ADC mismatch, opamp mismatch, and global variation in the current sources without the need for post-silicon trimming. The procedure is controlled by a RISC core located on chip, and can be run periodically to account for changing temperature and aging conditions.

All bias voltages and currents are generated from a single off-chip analog voltage supply. To simplify the design, the ADC will clip the extreme values that occur in the event of a strong signal, a case that will still be easily distinguished from noise. Loading of data into the matched filter is performed in parallel with computation. To save area, each bit of RF data is stored in a single latch (instead of a FF) and the latches are addressed using a crosshairs scheme. The storage operates as a simple buffer, so one element is loaded at a time by pulsing a single row and a single column select. Since the majority of control signals are driven vertically across the bank, the cells were custom designed to minimize vertical pitch and reduce wiring parasitics.

The matched filter was implemented in a 65nm LP CMOS process. Figure 24.3.4 shows the measured analog output overlaid on an ideal simulated digital output for a single-pass case and an eight-pass case, the latter including a correlation event. The correlation event is obtained by summing the magnitude of the eight passes through the matched filter, which increases gain and decreases noise. The analog computation shows very little deviation (typically at most one LSB) from the expected ideal output in both cases. Figure 24.3.4 also shows how clipping impacts the measured output compared to the ideal output, where the signal is still strong and detectable.

Additional noise is introduced by the analog circuit chain and differential current sources when performing the analog computation. To determine this extra noise did not have any impact on probability of detection, consecutive measurements of the filter output were taken and matched to a statistical model to isolate analog and current source noise from any quantization noise (Fig. 24.3.5). Variation in the differential current sources is the dominant source of noise in the analog computation – contributing 2.5× more noise than the analog chain, but still remains 10× lower than the noise inherent to the signal at the output of the matched filter, thus it does not impact correlation performance.

Figure 24.3.6 shows comparisons to prior work. The matched filter achieves 340-to-27000× higher performance than previous analog approaches while significantly reducing silicon area and obtaining a 67× gain in energy efficiency compared to an all-digital implementation [1]. The matched filter can be tiled to proportionally increase performance. Figure 24.3.7 shows the die micrograph (65nm LP CMOS).

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References:
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[2] Yamasaki, T., et al. "A low-power and compact CDMA matched filter based on switched-current technology", *IEEE J. Solid-State Circuits,* Vol. 40, No. 4, pp. 926-932, April 2005.
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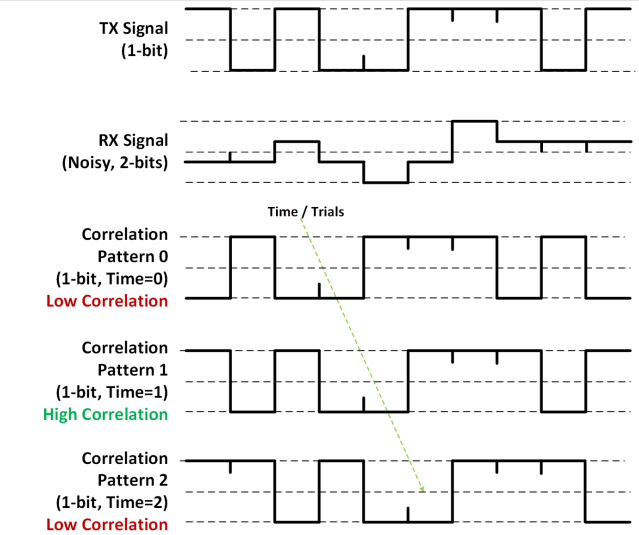

Figure 24.3.1: Example scenario. TX time can be recovered through correlation (Time=1 shows high correlation).

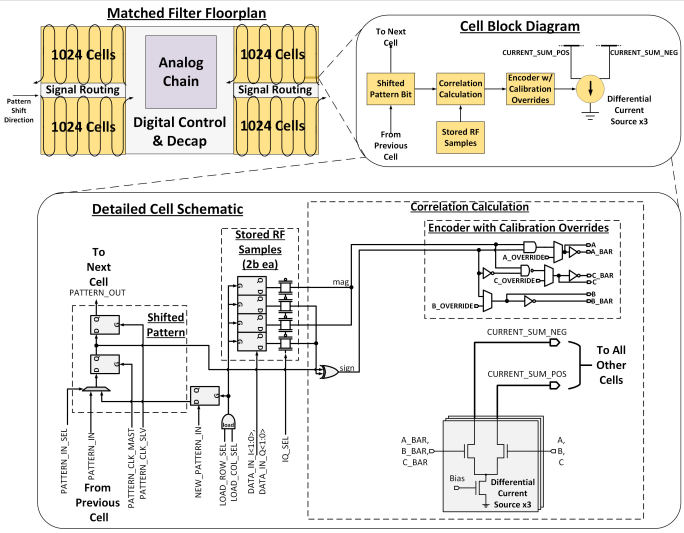

Figure 24.3.2: Matched filter floorplan, cell block diagram, and detailed cell schematic.

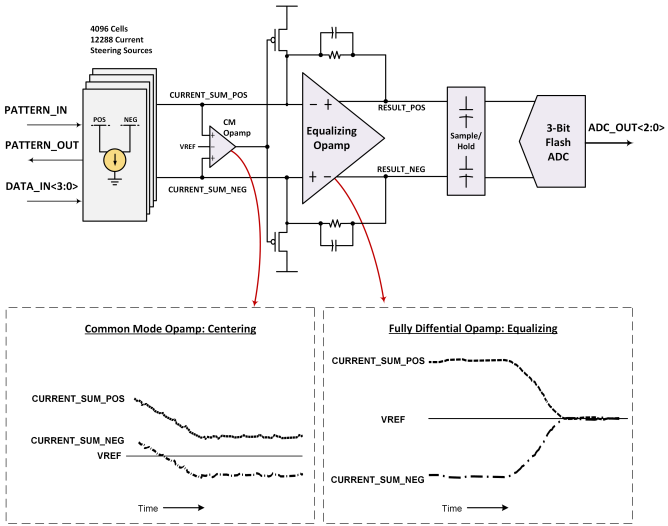

Figure 24.3.3: Block diagram of the analog chain. The S/H provides additional performance by enabling pipelining.

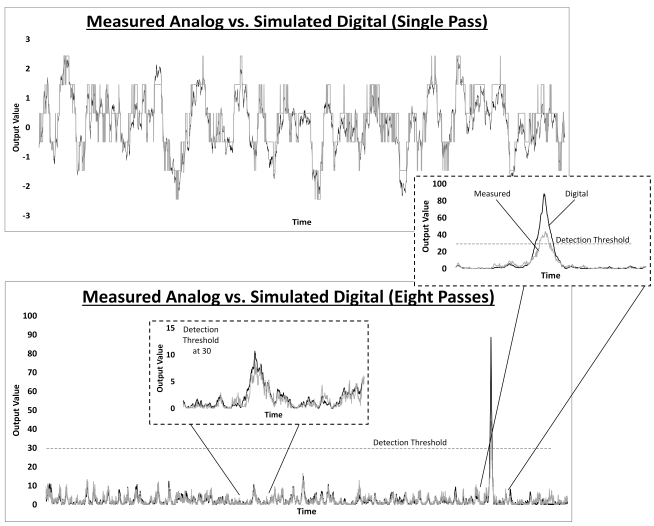

Figure 24.3.4: Measured output of the matched filter at 170 MHz, 25°C. Detection threshold heuristically chosen.

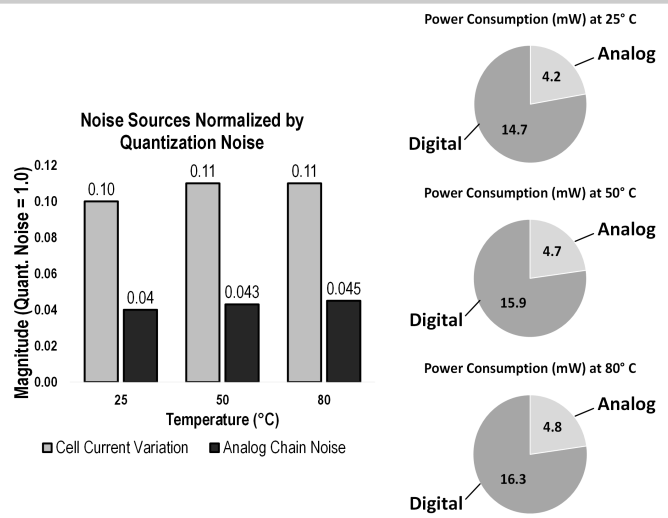

Figure 24.3.5: Noise from analog computation is negligible (10× lower) compared to noise inherent to the signal due to quantization.

	This Work	[1]	[2]	[3]
Technology	65 nm	180 nm	350 nm	130 nm
V_{DD} (V)	1.20 (Analog) 1.15 (Digital)	1.8	2.0	1.0
Clock Frequency (MHz)	170	20.46	8	0.2
Power (mW)	18.9	1,900	2	0.0000004
TOPS	**0.70***	**1.05**	**2.05E-3**	**2.56E-5**
TOPS/W	**36.8**	**0.55**	**1.05**	**64.0**
Vector Length	4,096*	51,150	256	128
Quantization	2-bit	2-bit	Analog	Analog
Area (mm^2)	0.325	88.0	0.54	0.13
Topology	Digital storage/ switched current	All digital	Analog storage/ switched current	Analog storage/ switched capacitor

*The design could be tiled to proportionally scale these metrics.

Figure 24.3.6: Comparison to prior works.

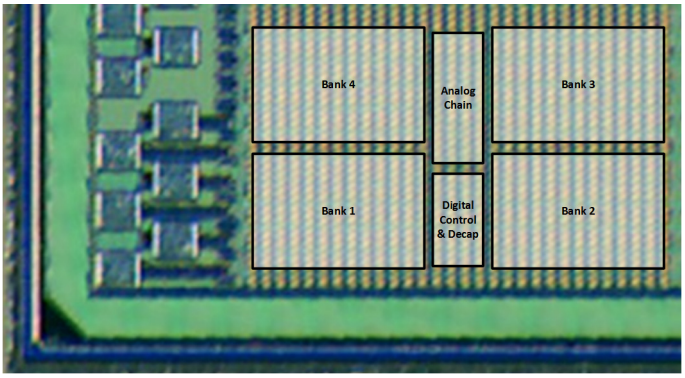

Figure 24.3.7: Die micrograph.

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