22.6 A Fully Integrated Counter-Flow Energy Reservoir for 70%-Efficient Peak-Power Delivery in Ultra-Low-Power Systems

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Recent advances in circuits have enabled significant reduction in the size of wireless systems such as implantable biomedical devices. As a consequence, the battery integrated in these systems has also shrunk, resulting in high internal resistances (~10kΩ). However, the peak-current requirement of power-hungry components such as radios remains in the mW range, and hence cannot be directly supplied from the battery. Therefore, duty-cycled architectures such as pulsed-based radios have been proposed that transmit a short burst (~1µs) of high power (~10mW) supplied by an internal energy storage capacitor [1-3]. The capacitor is then recharged using a current limiter to protect the battery from excessive droop. This paradigm raises two challenges: 1) to supply sufficient energy, very large capacitance (>50nF) is often needed (200mV droop, for 10mW and 5µs), leading to large die area or bulky off-chip discrete components; 2) only a small fraction (~5%) of energy stored in the capacitor is actually delivered to the high power components since the capacitor can only be discharged by a few 100s of mV while maintaining proper circuit operation (Fig. 22.6.1).

To extract more energy from the capacitor and reduce its size, a DC-DC up-converter can be used [4] to more fully deplete the stored energy while maintaining the required supply voltage. However, such a high-output-power DC-DC converter either requires an off-chip discrete inductor or a large on-chip flying capacitor array with similar or even larger total capacitance as the storage capacitor. Neither approach is therefore suitable to small form-factor sensors. In this paper, we propose a fully integrated energy reservoir unit that dynamically reconfigures a storage capacitor array using a so-called "countercurrent" flow (in short, counter flow) approach. This efficiently integrates the storage capacitor and DC-DC converter into one circuit, thereby maximizing area efficiency. It achieves efficient delivery (65%) of the stored energy to the load, and allows an up to 12× reduction in area compared to a simple capacitor. The design supplies up to 13.6mW output power. We demonstrate the proposed concept with a pulsed radio, showing an 11.5× increase in pulse length compared with using a single storage capacitor of the same size.

The key challenge in the reconfigurable energy reservoir is to deliver charge with minimum charge sharing loss (i.e., minimum voltage drop across switches) and to extract a very high percentage of the total charge (i.e., minimum remaining voltage on capacitors). To accomplish this, we use an approach inspired by a biological phenomenon called counter-flow, where oxygen and blood flow in opposite directions in fish gills, creating a slowly declining oxygen gradient for maximum gas exchange. Initially, all capacitors in the energy reservoir are fully charged. Energy is then extracted in two phases: First, a voltage gradient is created across two sets of capacitors in a "split" phase (Fig. 22.6.2). Second, the two sets of capacitors are stacked together in reverse direction (serially connecting the capacitors with largest voltages to those with smallest, etc.). As the load draws charge from the capacitor array and the voltage reduces, the two capacitor sets are repeatedly shifted in opposite directions in the "recombine" phase, increasing the voltage by the slope of the gradient with each shift. Since this shift operation simply increases the load voltage V_{supply} and does not cause any charge sharing within the capacitor array, charge sharing loss is avoided, resulting in highly efficient energy delivery. By repeatedly shifting, the vast majority of stored charge can be extracted, maximizing the total delivered charge. The successive split and recombine phases are controlled by a clocked comparator that automatically advances the array to the next configuration when V_{supply} drops below V_{min}, which is the minimum voltage required for proper circuit operation.

Figure 22.6.3 shows details of the capacitor reconfiguration process. Initially, all capacitors are fully charged (to VBAT = 4V in our implementation). In each step of the split phase, capacitors are split in half, stacking the capacitor with the highest voltage with the lowest, and second highest to the second lowest. This results in capacitor arrays with a fine-grained voltage gradient. To start with, the full 16C capacitors are discharged to V_{min}. In step 1, 4 unit capacitors (4C) are placed in series with another 4C, forming a "stack deck", and connect in parallel with 8C (the "main deck") to boost V_{supply} through charge sharing. As the load continues to pull down V_{supply}, 8C with V_{min} and 8C with ½ V_{min} are obtained (initial state in step 2). Step 2 stacks 4C at V_{min} and 4C at ½ V_{min} and charge shares with the 4C main deck at V_{min}. Steps 3 and 4 perform similar reconfiguration, resulting in a "trapezoid-shape" voltage gradient from 1/8 V_{min} to V_{min} with a step size of 1/8 V_{min}, which will be used in the subsequent recombine phase. To limit voltage overshoot ($V_{supply} > V_{max}$), timespreading is used where the switches are enabled sequentially, resulting in lower overshoot voltage at the cost of slightly higher charge sharing loss.

The recombine phase delivers energy based on counter flow. To start, the two "trapezoid-voltage-shaped" capacitor arrays are stacked in reverse directions, where capacitors with low voltages are connected in series with capacitors with high voltages. As the load drains charge from the reservoir, the capacitors with low voltage are drained by a much higher fraction because both serial capacitors experience the same voltage drop. To maintain high V_{supply} (=9/8 V_{min} here), the two trapezoid arrays are shifted in opposite directions, discarding the two capacitors that are already drained at the shortest edges of the trapezoids. This "shift and restore" step is repeated each time V_{supply} drops below V_{min}, ending with all capacitors discharged to half their original voltage. A second round of recombine phase (not shown in Fig. 22.6.3) is performed using "folded trapezoids" where pairs of capacitors with equal voltage are stacked and shifted, extracting 40% of the residual energy remaining after the first round.

Figure 22.6.4 shows the top-level architecture of the design, consisting of the counter-flow energy reservoir, a feedback loop for delivery modulation, a feedback loop for charging modulation, and a configuration controller. When the energy reservoir is in delivery mode, the load is enabled and V_{supply} is monitored using the "fast voltage divider", which combines a resistive and capacitive voltage divider for fast response time. When V_{supply} drops below V_{min}, comparator C1 triggers a pulse C_pulse. The configuration controller is an unconditional pulse-based state machine, which proceeds through pre-programmed states on each rising edge of C_pulse and generates the reconfiguration control signals. In charging mode, the reservoir energy is restored by reversing the steps of the recombine phase, which reduces the voltage difference seen by the current limiter to achieve much lower charging loss (~3× lower) than directly charging all capacitors. The charging state is again monitored by a clocked comparator. The comparators and clock generation operate at 1.2V to reduce power. A pulse-skipping module skips clock cycles immediately after C_pulse triggers a configuration change, allowing time for the energy reservoir to restore V_{supply}, avoiding false C_pulse edges.

A test chip was fabricated in 0.18µm CMOS. The V_{supply} waveform is captured (Fig. 22.6.5) for a load power of 1.4mW, showing 8× longer high-current delivery time compared to the conventional method. Voltage overshoot is limited to 90mV. The measured power breakdown shows that comparator and control overhead is 5.5%. The energy reservoir maintains >62% single-shot energy delivery efficiency (Fig. 22.6.6) across 45µW to 8mW load power, and extracts 17.5nJ from a 3.15nF on-chip storage capacitor before recharging, marking up to 12× improvement over the conventional method with 4% supply droop (equivalent to a 12× capacitor size reduction). By reversing the steps in the recombine phase during charging, the end-to-end efficiency improves from 45% to 70%. Integration with a radio demonstrates 11.5× longer continuous RF transmission. Figure 22.6.7 shows a die photo and summary table.

References:

[1] A. Shirane, et al., "A 5.8GHz RF-Powered Transceiver with A 113µw 32-QAM Transmitter Employing the IF-Based Quadrature Backscattering Technique", *ISSCC*, pp. 248-249, Feb. 2015.

[2] Y. Shi, et al., "A 10mm³ Syringe-Implantable Near-Field Radio System on Glass Substrate", *ISSCC*, pp. 448-449, Feb. 2016.

[3] M. H. Ghaed, et al., "Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor", *IEEE TCAS*, pp. 3152-3162, Aug. 2013.

[4] J. Yang, et al., "A 2.5-V, 160-µJ-Output Piezoelectric Energy Harvester and Power Management IC for Batteryless Wireless Switch (BWS) Applications", *IEEE VLSI Circuits Symp.,* pp.282-283, June 2015.

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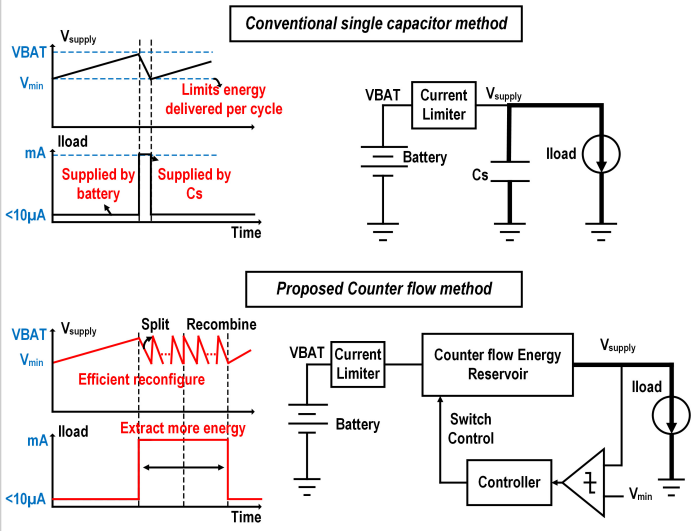


Figure 22.6.1: Concept of the proposed counter-flow energy reservoir.

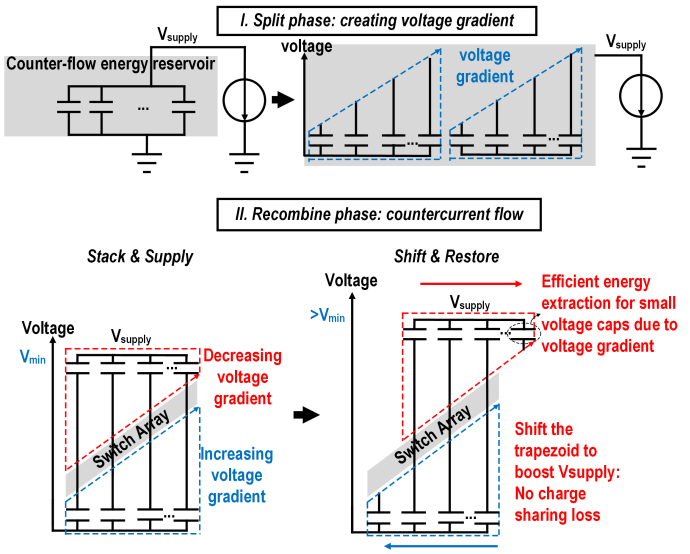


Figure 22.6.2: Concept of the proposed capacitor-configuration method.

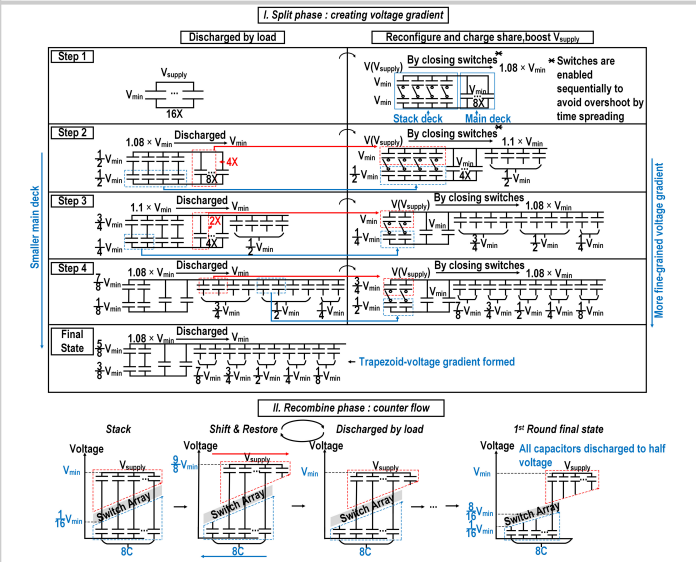


Figure 22.6.3: Capacitor configuration steps.

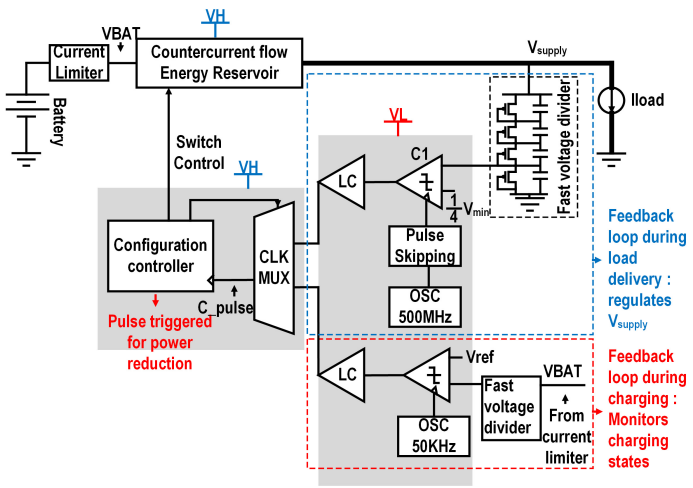


Figure 22.6.4: Top-level architecture of the implemented counter-flow energy reservoir.

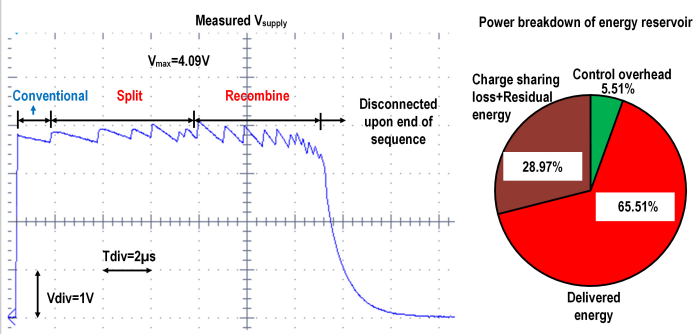


Figure 22.6.5: Measured output supply voltage waveform and power breakdown.

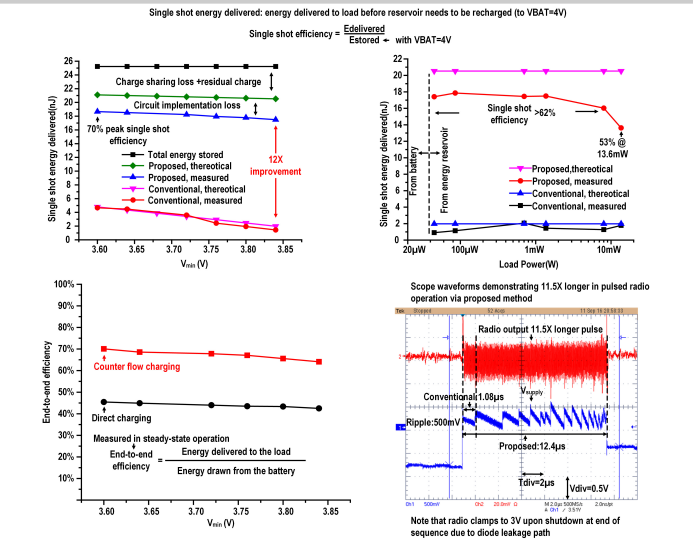
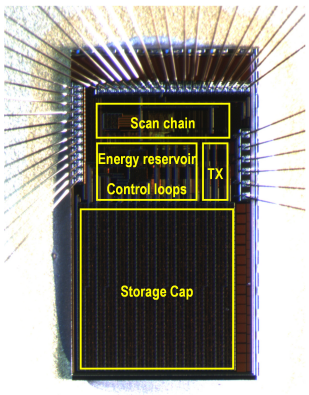
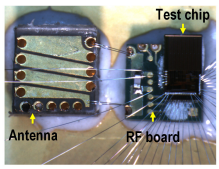


Figure 22.6.6: Measured energy delivery in single-shot and continuous operation and captured waveform with integrated radio.

Die Photo



Integration with radio



Chip characteristics summary

Technology	0.18µm CMOS
Chip area	3.8mm^2
Fully integrated	Yes
Capacitor size	3.15nF
Output power range	45µW – 13.6mW
Control overhead	5.5%
Single shot energy delivered	18.7nJ @ 10% V_{supply} drop

Figure 22.6.7: Die micrograph of test chip, and integrated system and summary table.

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