A 1.7nW PLL-Assisted Current Injected 32KHz Crystal Oscillator for IoT

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Abstract

This paper presents a PLL-assisted crystal oscillator using a current switching phase detector (PD) with intrinsic 90° phase offset for IoT applications. The PLL provides accurate pulse injection timing into the XO, sustaining its oscillation at only 100mV amplitude and ensuring robustness operation across PVT. This technique achieves high energy injection efficiency and avoids the use of power hungry amplifiers. Measured power is 1.7nW at room temperature and operation is demonstrated from -20 – 80°C and across 3 corner wafers.

Introduction

Crystal oscillators (XOs) are commonly used in low-power IoT devices to provide an accurate timing reference. IoT devices are typically highly duty-cycled, and hence sleep power often dominates the total power budget. XO circuits often must be awake even when the system sleeps (e.g., for synchronization, wakeup, etc.) and therefore ultra-low power is a critical design constraint [1]. Recent progress in Ultra Low Power (ULP) XOs suffers from the use of high-power amplifiers [2] or low injection efficiency [4], resulting a high power consumption. Reference [5] achieves the minimum reported power consumption (1.5nW) but trades off startup time (> 30s) for low power consumption and requires significant calibration. To minimize power while also avoiding long start-up time and calibration, we propose an XO circuit that uses a 90° phase aligned PLL to ensure accurate timing of pulse injection into the crystal. Measurements in 55nm deeply depleted channel (DDC) technology shows 1.7nW power consumption at room temperature and robust operation at SS and FF corner die.

PLL Working Principle

The most common XO oscillator uses an inverter to sustain the oscillation. However, this so-called Pierce oscillator requires a constant bias current, increasing power consumption (27nW) [6]. To eliminate this constant current, a pulse injection scheme was first proposed in [2], which only injects current pulses at the peaks and trough of the XO waveform. By injecting only at these extremes, the voltage across the driving transistors is minimized which maximizes the injection efficiency and reduces power consumption (5.58nW) [3]. However, this approach uses a high power amplifier and delay cells to generate the injection timing, which limits its power reduction and robustness across temperature and process variation. Reference [4] also adopts pulse injection but implements a logic-based design, which eliminates the need of high power components. However, as a result it compromises injection accuracy and suffers from lower injection efficiency. Reference [5] uses a conventional Pierce oscillator structure instead but tunes the pull up/down strength carefully so that the inverter driver is at the boundary of being able the sustain oscillation. However, this results in a long start-up time (>30s) due to low driving strength and may require recalibration across temperature.

In this work, we propose a pulse injected XO that uses a PLL with current switching PD to avoid the need for a high power amplifier and delay cells while guaranteeing accurate injection timing across process corners and temperature. The circuit sustains the XO oscillation at 100mV while the PLL operates at 400mV with a total power consumption of 1.7nW. Fig 1 shows a conceptual schematic where OSC_IN is connected to the output of the crystal. The shaded area shows the phase detector (PD) circuit which consists of two transistors (M_1, M_2) and two switches (SW_1, SW_2). The two transistors act as current sources that depend on the amplitude of OSC_IN, and the two switches are alternatively turned on when the output of the VCO, (VCO_OUT and VCO_OUTB) switches. Only when the charge injected by SW_1 equals the charge extracted by SW_2 does the VCO control voltage, V_{CTRL}, remain stable. As shown in Fig. 2, when the edges of VCO_OUT are aligned with the exact peaks and troughs of the XO waveform, is the waveform of OSC_IN while SW_1 is enabled the mirror image of the waveform of OSC_IN while SW_2 is enabled. This condition results in equal charge injection (Q_{INJ}) and extraction (Q_{EXT}) at V_{CTRL} and achieves 90° phase offset locking. The proposed PD removes the need for an amplifier to transform OSC_IN to a square wave [2], and maintains an accurate lock even with an XO oscillation amplitude of 100mV. VCO_OUT is used to generate the current injection pulses to sustain the XO oscillation (Fig. 3) using pulse generators. It also serves directly as XO output and removes the need for further level conversion.

In the proposed PD, mismatch between the two current sources can affect the accuracy of the injection timing. To address this, a second feedback path is implemented, as shown in Fig 1 in red. When the PLL is locked, any mismatch between M_1 and M_2 will again result in unequal charge injection / extraction at node V_{FB} causing it to move up or down in voltage, automatically adjusting the conductance of M_1 and M_2 to match through body biasing. Since the bandwidth of the feedback loop is very low it does not affect regular PLL locking.

Architecture of Whole Circuit

Fig. 4 shows the overall architecture of the proposed circuit. VCO_OUT and VCO_OUTB are connected to a pulse generator shown in Fig. 5. Pulses are generated after the edges of the VCO. The pulses turn on the pulse-injection driver for a short time (1μS, simulation), during which the driver injects or extracts charges to/from XO capacitors. In this way, the energy loss of crystal is replenished with high energy efficiency.

The XO oscillator has two working phases: start-up phase and normal phase. The start-up circuit is composed of a conventional phase frequency detector (PFD) and a charge pump, as shown in Fig. 6. During start-up, the pulse generator and the pulse-injection driver are disabled and an inverter is used to drive the crystal. V_{CTRL} is connected to the conventional charge pump output (Fig. 6) instead of the PD to ensure the VCO locks to the correct frequency. This is necessary because the proposed PD has a limited frequency capture range. If the initial voltage of V_{CTRL} is not initially set correctly by the PFD, the VCO may be locked to 1/3, 1/5, etc. of the XO frequency. After start-up, the inverter driver and start-up circuit are disabled and the core PLL-assisted driving circuit sustains oscillation. The V_{CTRL} waveform during the two phases is shown in Fig. 12 (simulation). The proposed circuit uses two power domains: VDDM (0.4V) is used for the main PLL and start-up circuit while a lower VDDL (0.1V) supplies the drivers that sets the XO oscillation amplitude.

Measurement Results

Fig. 11 shows the die photo of the test chip in 55nm DDC technology. Table 1 shows the measured power consumption for TT, FF and SS corner wafers, demonstrating robust and power efficient operation across process variation. Fig. 7(a) and (b) shows the power across a range of VDDM and VDDL voltages, respectively. In Fig. 7(a), VDDM varies from 0.4V to 0.8V without disturbing the XO oscillation. Driving power can be reduced by lowering VDDL as shown in Fig. 7(b). Fig. 7(c) reports the power across temperature. Total power increases by 8× from 20^0C to 80^0C due to increased sub-threshold current. Fig. 8(a) shows the frequency variation across different VDDLs with a maximum variation of only 4 ppm. Fig. 8(b) shows the sensitivity of frequency to temperature which is nearly equal to the XO innate temperature dependence. Fig. 9 shows the Allan Deviation and Fig. 10 shows the measured waveform of VCO_OUT and OSC_IN. Table 2 is the comparison table showing relevant other work. This work achieves more than 2x power reduction compared to other works except [5]. However, the start-up time of this work is less than 10ms, which is 3000 times smaller than that of [5]. The proposed approach does not require calibration and shows robust operation across process corners.

Acknowledgement

We thank Masaru Kawaminami and Akihido Harada in Fujitsu Semiconductor for design kit support and chip fabrication.

References

[1] Y.Lee, JSSC, 2013
[2] D. Yoon, ISSCC, 2012
[3] D. Yoon, JSSC, 2016
[4] K. Hsiao, ISSCC, 2014
[5] A. Shrivastava, JSSC, 2016
[6] W. Thommen, ESSCIRC, 1999

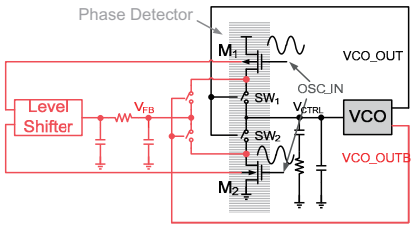


Fig. 1.Conceptual schematic of the PLL

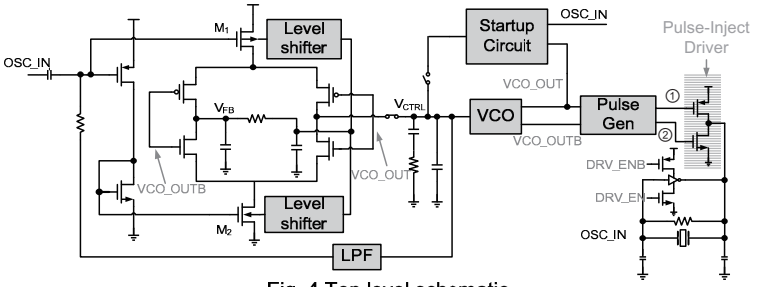


Fig. 4.Top level schematic

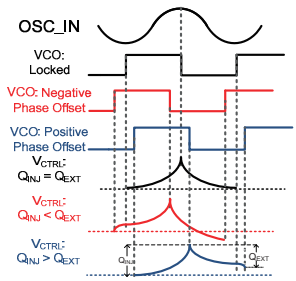


Fig. 2. Different phase offset between VCO_OUT & OSC_IN

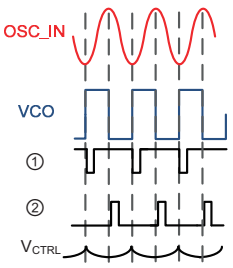


Fig. 3. Waveform of XO and VCO when locked

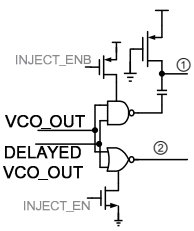


Fig. 5. Pulse generation circuit

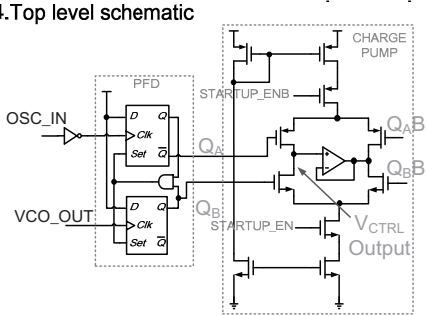
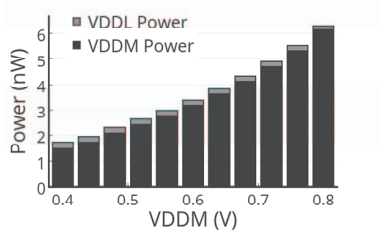
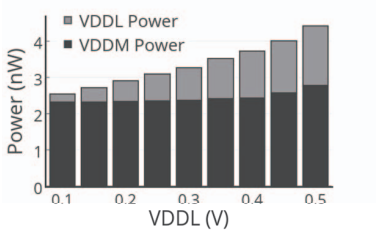


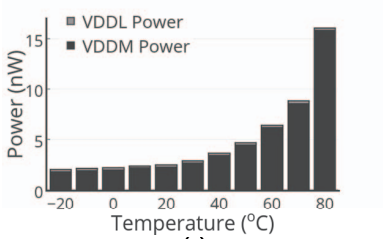
Fig. 6. Startup Circuit



(a) VDDL=0.1V

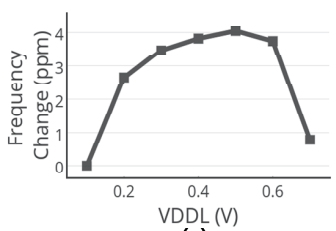


(b) VDDM=0.5V

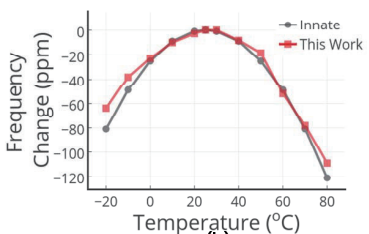


(c)

Fig. 7. Measured power dependence of (a) VDDM (b) VDDL (c) Temperature



(a)



(b)

Fig. 8. Measured frequency dependence of (a) VDDL (b) Temperature

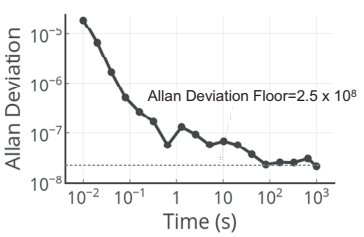


Fig. 9. Allan Deviation

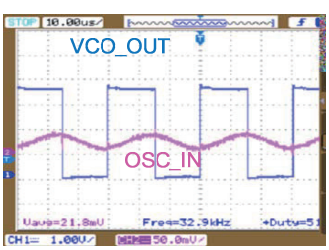


Fig. 10. Tested waveform

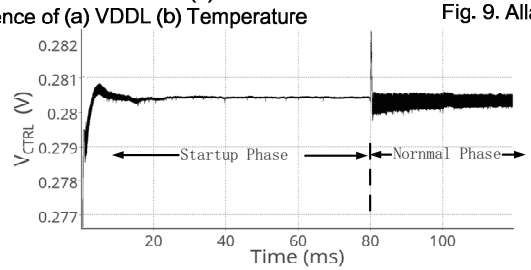


Fig. 12. Simulated V_{CTRL}

Corner	Power (nW)
TT	1.7
FF	3.3
SS	2.1

Table 1. Measured power consumption across split-wafer corner die

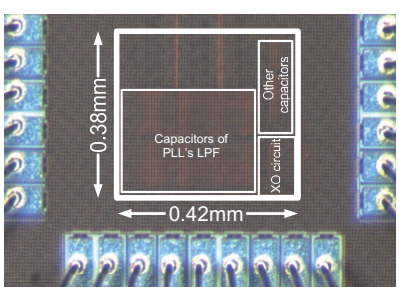


Fig. 11. Die photo

	This work	[2]	[4]	[5]	[6]
Frequency (KHz)	32.768	32.768	32.768	32.768	32.768
Technology	55nm	180nm	28nm	180nm	2μm
Area (mm^2)	0.16	0.3	0.03	0.0625	N/A
Power at Room Temp(nW)	1.7	5.58	5	1.5	27
V_{DD} (V)	VDDL:0.1~0.5 VDDM:0.4~0.8	0.94 ~1.82	0.15 ~ 0.5	0.3 ~ 0.9	0.71
Tested Temperature(°C)	-20~80	-20~80	-20~80	0 ~ 80	N/A
Temperature stability	109.1 ppm	133 ppm	48.8 ppm	150 ppm	N/A
Line sensitivity	6.7ppm/V	30.3 ppm/V	85 ppm/V	7 ppm/V	N/A
Allan Deviation (ppb)	2.5	~ 1	< 1	7	N/A
Startup Time(s)	0.008	N/A	N/A	31	N/A

[4] reported power consumption of 1.85nW at -20 °C as confirmed by author. Based on graph [17.7.4], power at room temperature is ~5nW.

Table 2. Comparison Table