27.8 A Static Contention-Free Single-Phase-Clocked 24T Flip-Flop in 45nm for Low-Power Applications

Yejoong Kim, Wanyeong Jung, Inhee Lee, Qing Dong, Michael Henry, Dennis Sylvester, David Blaauw

University of Michigan, Ann Arbor, MI

Near-threshold computing (NTC) is an attractive solution to stagnating energy efficiencies in digital integrated circuits, arising from slowed voltage scaling in nanometer CMOS [1-2]. The design of sequential elements for NTC, as well as in voltage-scaled systems operating at both near-threshold and super-threshold, has not been extensively studied. However, it is well known that sequential elements have a strong sensitivity to process variations in NTC [2], which can have a significant impact on system yield and power consumption. In order to achieve reliable energy-efficient operation across a wide operating voltage range, a flip-flop should have the following attributes: 1) static operation, since dynamic nodes are highly susceptible to PVT variations at low voltage; 2) contention-free transitions, since ratioed logic has poor robustness across the wide range of device I_{ON}/I_{OFF} ratios incurred with voltage scaling; 3) single-phase clocking, which avoids toggling of internal clock inverters and the corresponding power penalty; 4) minimum or no area penalty compared to conventional flip-flops.

While many flip-flops have been proposed, no prior design meets all these requirements for an energy-efficient, highly voltage-scalable sequential element. Fig. 27.8.1 highlights shortcomings in several common flip-flops. The widely-used conventional 24T TGFF exhibits high power consumption due to a large number of clocked nodes (i.e., it is not single-phase clocked). The ACFF [3] uses single-phase clocking operation and has fewer devices than the TGFF but experiences current contention in the slave latch. This contention can be suppressed at the expense of additional devices (area). The TGPL [4] is based on pulsed operation and achieves high performance at full V_{DD} but has poor robustness at low V_{DD} due to increased process-variation sensitivity. The TSPC [5] employs single-phase clock operation and uses only 11 devices. However, its dynamic operation degrades robustness, especially at low V_{DD}. In addition, Fig. 27.8.1 illustrates a non-negligible glitch at node *QN* in the TSPC whenever CK goes high while D remains 0. This arises since precharged *net2* begins to discharge *QN* before M5/M6 can pull *net2* low, resulting in unnecessary power consumption or even a system malfunction.

This work presents a new flip-flop, referred to as static single-phase contention-free flip-flop (S^2CFF) that meets the requirements above: it is static, completely contention-free, and uses single-phase clocking. It has the same device count as a TGFF, with only a 7% layout size increase that corresponds to a one poly-pitch increase in 45nm technology, where fixed poly-pitch is enforced. Fig. 27.8.2 shows the S^2CFF schematic and describes its operation. For CK=0, *net1* holds $\overline{D}$ value, *net2* precharges through M8, and the slave latch (M17~M22) stores the previous data. If D=0, the high *net1* starts discharging *net2* at the positive edge of CK. Then, discharged *net2* turns off M3, completely isolating the circuit from changes in D. Also, the low *net2* charges *QN* through M13, updating the data in the slave latch. Note that *net1* is held high by M5, while M9/M10 keep *net2* low during the high CK phase. If D=1, the positive edge of CK does not generate any dynamic transitions at *net1* and *net2*. During CK=1 phase, *net1* is kept low by M7/M10, and M6 holds *net2* high. If the previous Q value is the same as the current D input (i.e., *QN*=0), there is also no transition at *QN*. Otherwise, *QN* discharges through M14~M16. Signal *net1b* is also used to control M15; without this sub-circuit, *QN* will glitch when CK rises with D staying low in consecutive cycles, similar to the TSPC. M15 eliminates this glitch by cutting off the discharge path (M14~M16) depending on *net1*'s value. Note also that there is no contention throughout the operation, all internal nodes are fully static, and only one clock phase (CK) is used.

An additional benefit of the S^2CFF topology is that it simplifies the "hold-time path" compared to a regular TGFF (Fig. 27.8.3). As described in [6], the worst-case hold time in a TGFF is when D changes from 1 to 0 just after the CK edge, and it is dictated by mismatch among the clock/data inverters (I1, I3, I4). Due to clock inversion in $PATH_{CK}$, the NMOS in I2 turns off earlier than its PMOS, while the PMOS in I5 turns on before its NMOS, weakening the pull-down strength at node *MN*. Hence, a TGFF shows severe hold-time degradation at low V_{DD} where mismatch is accentuated. On the contrary, the worst-case hold time in the S^2CFF occurs when D changes from 0 to 1 just after the CK edge. The high *net1* starts discharging *net2*, and the discharged *net2* turns off M3, isolating the D input. If D becomes 1 before *net2* shuts off M3, and thus discharges *net1*, a hold failure may result. Only the discharging speed of *net2* through $PATH_{CK}$ dictates the hold time. As a result, the hold time of the S^2CFF is much less prone to variability compared to the TGFF, which involves the time difference of several gate delays. Fig. 27.8.3 shows a substantial reduction (3.4×) in hold time at the 3σ value at 0.32V for S^2CFF (from Monte Carlo simulations). This suggests a large potential benefit for NTC, since small hold-time variation reduces buffer-insertion overhead, reducing power and improving system yield.

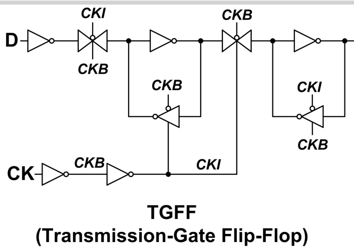
The S^2CFF is characterized in a 45nm SOI test chip that also includes TGFF, ACFF, and TGPL for comparison. 50 dies are measured. On-chip testing circuits are shown in Fig. 27.8.4, where the setup/hold-time measurement circuit is based on the structure in [7]. In the power measurement circuit, the activity ratio is controlled using the 20b initial pattern. To mimic a realistic scenario, the test chip has one clock buffer driving 10 DUTs. The current flowing into 'CLKBUF + 10 DUTs' is measured and then divided by 10. The C-Q delay measurement circuit incorporates a new flip-flop ring, where a short pulse at the EN input triggers the oscillation of DUT Ring with a period that is proportional to T_{CQ} with an offset value; this offset can be measured using Reference Ring. With a large N (= number of unit cells in a ring) value, local mismatch is effectively cancelled out making it possible to obtain accurate C-Q delays. This test chip uses 100 unit cells per ring (N=100). The DUT Ring also gives insight on DUT yield, since oscillation stops unless all 100 DUTs in the ring are functional.

Figure 27.8.5 shows measured total power and energy. The S^2CFF does not require internal clock inverters, enabling a clock power (defined as total power at 0% activity ratio with D=0) reduction of 41% at 1V/1GHz compared to TGFF. Assuming that flip-flops in a typical system have 20% activity ratio, the S^2CFF provides 39% and 38% improvement in total sequential power at 1V/1GHz and 0.4V/200MHz, respectively. Active energy consumption is also reduced by 32% and 34% (1.0V and 0.4V, respectively). The measured ACFF total power increases rapidly as activity rises due to contention in the slave latch. The TGPL has a delay element, which leads to higher total power consumption, even at 0% activity ratio. Fig. 27.8.6 shows measured C-Q delays and leakage power. The S^2CFF shows modest improvement over the TGFF across V_{DD}. Missing points in the plot indicate that ACFF fails to have 100% yield at 0.4V due to contention. The TGPL fails at $V_{DD} \leq 0.6V$, mainly due to hold-time failures. This illustrates the importance of static and contention-free operation at low V_{DD}, since only the TGFF and S^2CFF show 100% yield across the wide V_{DD} range. The S^2CFF has 35% lower leakage power than the TGFF at 1.0V. The provided comparison table includes other recently proposed flip-flops, showing that the S^2CFF is the only flip-flop with static, contention-free, single-phase clock operation with minimum area penalty (one poly-pitch) and same device count as TGFF. The S^2CFF has 15.5% faster 'setup time + C-Q delay' at 1.0V vs. the TGFF, as shown in the table. Fig. 27.8.7 includes the die photo of the test chip.

Acknowledgment:
Funding support of DARPA (agreement HR0011-13-2-0006) and US Army Research Laboratory is gratefully acknowledged.

References:
[1] B. Zhai, *et al.*, "Energy Efficient Near-Threshold Chip Multi-Processing," *IEEE International Symp. Low-Power Electronics and Design*, pp. 32-37, 2007.
[2] S. Jain, *et al.*, "A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 66-67, 2012.
[3] C.-K. Teh, et *al.*, "A 77% Energy-Saving 22-Transistor Single-Phase Clocking D-Flip-Flop with Adaptive-Coupling Configuration in 40nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 338-339, 2011.
[4] S. D. Naffziger, *et al.*, "The Implementation of the Itanium 2 Microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448-1460, 2002.
[5] J. Yuan, *et al.*, "High-Speed CMOS Circuit Technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62-70, 1989.
[6] C.-H. Chen, *et al.*, "Minimum Supply Voltage for Sequential Logic Circuits in a 22nm Technology," *IEEE International Symp. Low-Power Electronics and Design*, pp. 181-186, 2013.
[7] B. Giridhar, *et al.*, "Pulse Amplification Based Dynamic Synchronizers with Metastability Measurement using Capacitance De-rating," *IEEE Custom Integrated Circuits Conf.,* 2013.

 978-1-4799-0920-9/14/$31.00 ©2014 IEEE



	TGFF	ACFF[3]	TGPL[4]	TSPC[5]
Static Operation	YES	YES	NO*	NO
Single -Phase Clock	NO	YES	YES	YES
Contention -Free	YES	NO	YES	YES
Device Count	24	22 or more	24 or more	11

* Pulsed operation

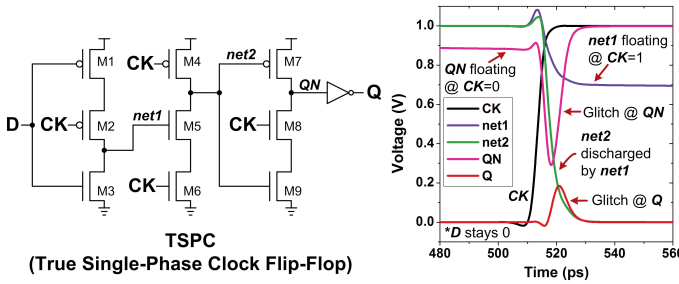


Figure 27.8.1: Conventional flip-flops and TSPC waveforms.

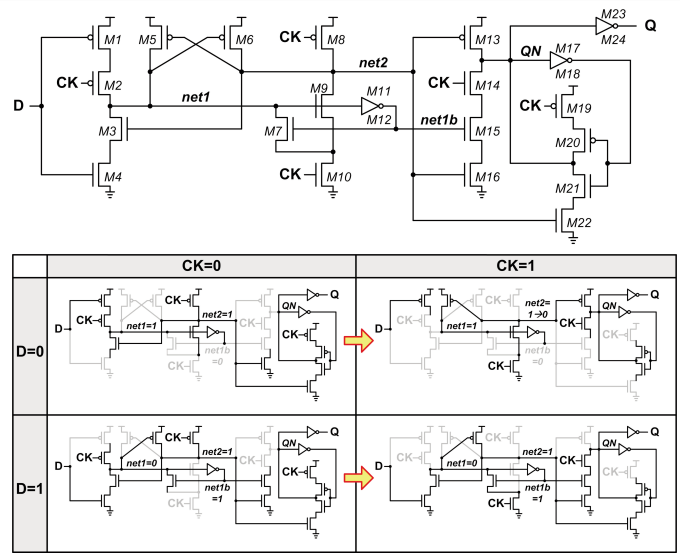


Figure 27.8.2: Schematic of S²CFF and its operation.

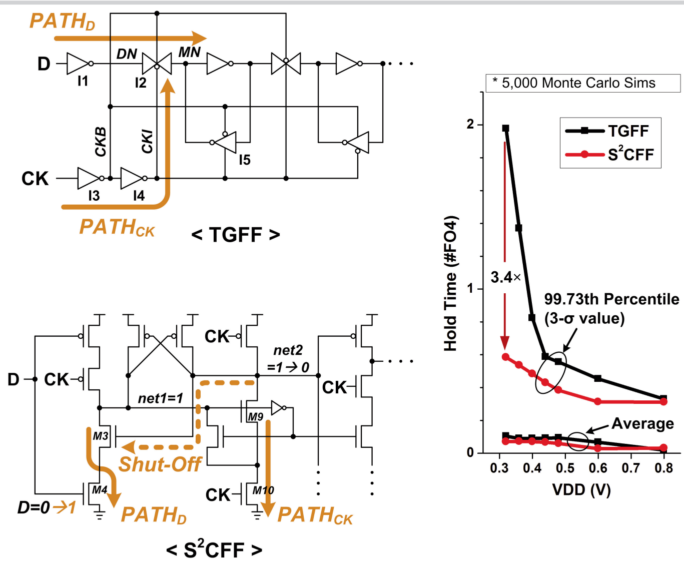


Figure 27.8.3: Hold-time paths and simulated hold-time variation.

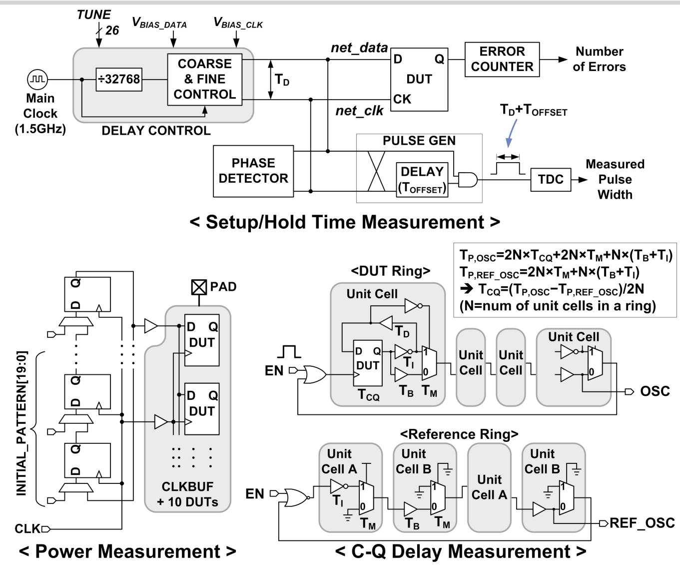


Figure 27.8.4: Testing circuits.

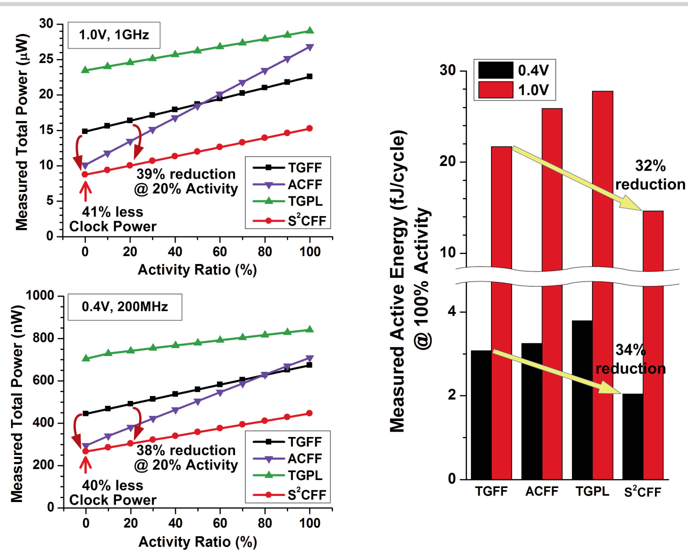
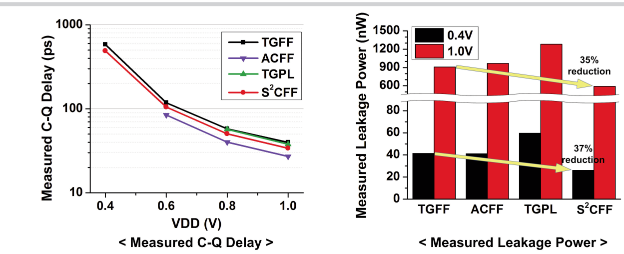


Figure 27.8.5: Measured power and energy comparisons.



	S²CFF (This Work)	TGFF Standard Cell Lib.	ACFF Teh, ISSCC'11	TGPL Naffziger, JSSC'02	CSP³L* Consoli, ISSCC'12	DMFF* Nomura, ISSCC'08	CPSA* Ueda, ISSCC'06	CCFF* Kong, JSSC'01	HLFF* Partovi, ISSCC'96
Type	Static	Static	Static	Pulsed	Pulsed	Pulsed	Static	Pulsed	Pulsed
Contention-Free	Yes	Yes	Partially	Yes	Yes	No	No	No	No
Single Phase Clock	Yes	No 1)	Yes	Yes	No 1)	No 1)	Yes	Yes	No 1)
Number of Transistors	24	24	22 2)	28 3)	42 4)	24 5)	28	35	20
Normalized Layout Size	1.07	1.00	1.13	1.40					
Measured C-Q Delay @ 1.0V	33.9ps	39.8ps	27.1ps	37.9ps					
Measured Setup Time @ 1.0V	34.0ps	40.6ps	77.8ps	8.5ps					
Measured Hold Time @ 1.0V	-25.7ps	-31.4ps	-66.1ps	1.28ps					
Measured Total Power @ 1.0V, 1GHz, 20% Activity	10.02µW	16.36µW	13.45µW	24.57µW					
Measured Leakage @ 1.0V	592nW	909nW	967nW	1283nW					

1) Inverted clock signal is used in the circuit (the circuit includes a clock inverter)
2) It becomes 26 if ACE (Adaptive-Coupling Element) is added to the slave latch for low-voltage robustness
3) Delay element has 5 inverters to generate a pulse
4) 16 transistors (pulse generator) can be shared among multiple flip-flops.
5) Assuming 3 inverters are used for delay generation

* CSP³L, DMFF, CPSA, CCFF, HLFF are not implemented in this test chip.

Figure 27.8.6: Measured C-Q delay, leakage, and comparison table.

27

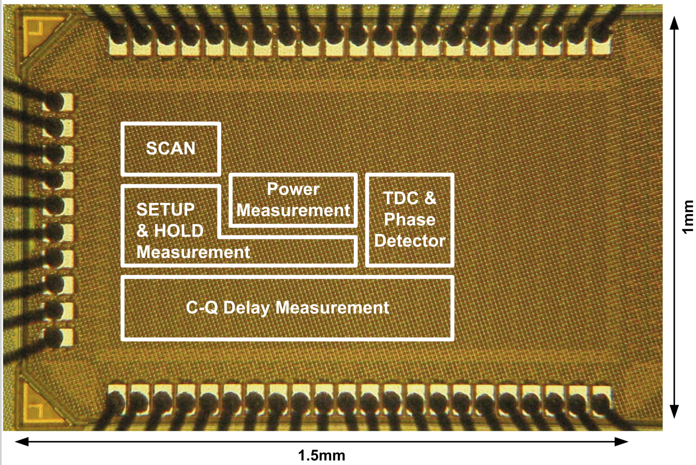


Figure 27.8.7: Die photograph of the 45nm SOI test chip.