A Dual-Slope Capacitance-to-Digital Converter Integrated in an Implantable Pressure-Sensing System

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Abstract—A dual-slope capacitance-to-digital converter for pressure-sensing is presented and demonstrated in a complete microsystem. The design uses base capacitance subtraction with a configurable capacitor bank to narrow down input capacitance range and reduce conversion time. An energy-efficient iterative charge subtraction method is proposed, employing a current mirror that leverages the 3.6 V battery supply available in the system. We also propose dual-precision comparators to reduce comparator power while maintaining high accuracy during slope conversion, further improving energy efficiency. The converter occupies 0.105 mm^2 in 180 nm CMOS and achieves 44.2 dB SNR at 6.4 ms conversion time and 110 nW of power, corresponding to 5.3 pJ/conv-step FoM. The converter is integrated with a pressure transducer, battery, processor, power management unit, and radio to form a complete 1.4 mm $\times$ 2.8 mm $\times$ 1.6 mm pressure sensor system aimed at implantable devices. The multi-layer system is implemented in 180 nm CMOS. The system was tested for resolution in a pressure chamber with an external 3.6 V supply and serial communication bus, and the measured resolution of 0.77 mmHg was recorded. We also demonstrated the wireless readout of the pressure data on the stack system operating completely wirelessly using an integrated battery.

Index Terms—Capacitance-to-digital converter, capacitive-sensor interface, integrating converter, pressure-sensing system, wireless sensor node.

I. INTRODUCTION

IMPLANTABLE systems are increasingly in demand for emerging biomedical applications, and yet they face stringent power budgets because battery capacity is limited due to their small volume [1], [2]. These systems collect and analyze sensor data, which is often measured in the form of capacitance. Capacitive sensor interfaces are widely used because of their inherent energy benefit; i.e., they do not draw static current, unlike resistive sensors. However, a capacitive-sensor interfacing circuit could dominate system power, and hence an energy-efficient capacitance-to-digital converter (CDC)
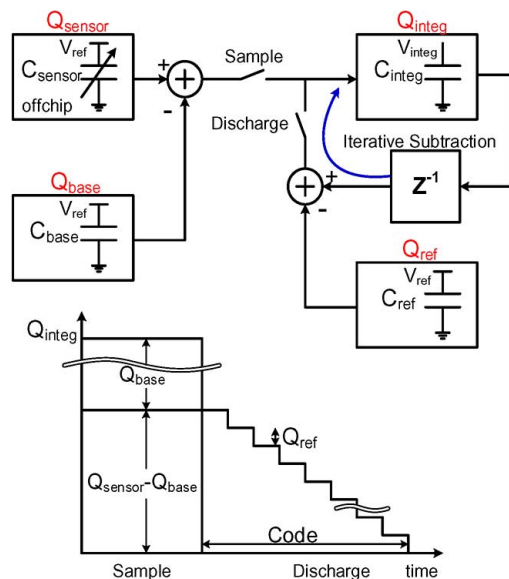
Fig. 1. Simplified block diagram of the proposed CDC and an associated waveform.

is required. Capacitive sensors, along with a corresponding CDC, are used in diverse applications such as pressure-sensing [3], humidity-sensing [4], proximity-sensing [5], and microphones [6].

Pressure-sensing is a key technique used in implantable devices with applicability to glaucoma treatment [2], [7], blood pressure monitoring [8], and tumor diagnosis, among others. These systems typically use a MEMS capacitive sensorand they require a moderate-resolution (9–10b), low-power CDC. Dual-slope converters are well known for their simplicity, accuracy, and low power consumption [9], [10]. However, their nominal base capacitance is often quite large compared to the capacitance changes due to pressure variations. The need to charge and discharge the large base capacitance in dual-slope CDCs (DS-CDC) makes it difficult to achieve sufficient resolution with high energy efficiency.

To address this challenge, we employ iterative charge subtraction/accumulation using a configurable capacitor bank to cancel base capacitance, and to zoom in and amplify the variable input region [4], [5]. This reduces the conversion time and energy for the DS-CDC (Fig. 1). The design also uses dual-precision comparators to achieve the high-resolution of a fine comparator with the low power consumption of a coarse comparator. It does this by enabling the fine comparator only in the final

Fig. 2.   Circuit diagram of the dual slope CDC.

stages of conversion. The CDC has a low power consumption of 110 nW, which makes it compatible with ultra-small batteries that often suffer from low peak current capacity. We demonstrate CDC operation that is integrated with a complete pressure-sensing system using a MEMS pressure sensor, processor, memory, battery, and radio.

The remainder of the paper is structured as follows. Section II describes the proposed topology of the DS-CDC with a detailed description and analysis. Section III describes the implementation of the pressure-sensing system with the proposed CDC. Section IV presents CDC measurement results and demonstrates system operation, while Section V concludes the work.

II. CAPACITANCE-TO-DIGITAL CONVERTER ANALYSIS AND IMPLEMENTATION

A. Dual-Slope Operation

Fig. 1 shows a simplified block diagram of the proposed DS-CDC. The sampled charge difference between C_{sensor} and C_{base} is transferred to C_{integ}, and the transferred charge is removed by iterative subtraction using C_{ref}. The CDC circuit consists of a current mirror, charge subtraction/accumulation devices, and two comparators (shown in Fig. 2), followed by a ripple carry counter and digital control logic.

Fig. 3 shows the waveforms in the DS-CDC. During the reset state, all of the OTAs are disabled, and the RST switch is closed to set the voltage of C_{integ} to V_{ref_c}. In the next sampling state, the OTA$_1$ and OTA$_2$ are enabled. While $\Phi_{s1} = 1$, the charge is removed from C_{sensor} and C_{base} by shorting both nodes of the capacitors to ground. With $\Phi_{s2} = 1$, the top plate nodes of these capacitors are set to V_{ref_a} due to the feedback of the OTA and the device gated by Φ_{s2}. Since $\Phi_{s1} = 0$ in this phase, all current conducted by the source followers is accumulated on C_{sensor} or C_{base}. The OTAs drive the source followers to track V_{ref_a} with little error, and a current mirror above the source followers flips the direction of current from C_{sensor}. As a result, the amount of transferred charge Q_{add} added to C_{integ} (4 pF) for each Φ_s cycle is:

$$Q_{add} = (C_{sensor} - C_{base}) \times V_{ref\_a} \qquad (1)$$

Fig. 3.   CDC waveforms.

The full sampling operation consists of $4\Phi_s$ cycles, during which $4Q_{add}$ is transferred, thus providing $4\times$ charge amplification.

In the following discharge state, OTA$_3$ and one of the two comparators is turned ON. Similarly, the amount of charge that is subtracted from C_{integ} for each Φ_c cycle (denoted Q_{sub}), and the value of V_{integ} at the end of nth cycle of the discharge stage are given by:

$$Q_{sub} = C_{ref} \times V_{ref\_a} \qquad (2)$$

$$V_{integ}(n) = V_{ref\_c} + \frac{4Q_{add} - n \cdot Q_{sub}}{C_{integ}} \qquad (3)$$

C_{ref} (18 fF) is composed of two MIM capacitors in series. The discharge state ends when V_{integ} becomes smaller than V_{ref_c}; the total number of required cycles is recorded by a ripple carry counter as the digital code.

$$Code = 4Q_{add}/Q_{sub} = 4(C_{sensor} - C_{base})/C_{ref} \qquad (4)$$

In the proposed CDC, C_{sensor} is an off-chip sensor capacitor, and C_{base} is a programmable on-chip MIM capacitor bank composed of capacitors and NMOS switches, allowing for adjustment of the capacitance measurement range. V_{ref_a} is 300 mV

Fig. 4. Block diagram of the CDC with power domain.

Fig. 5. Capacitive feedback of an OTA (switches not shown).

Fig. 6. Discharge circuit schematic.

and each C_{base} has a 4 pF linear range, and thus the maximum $4Q_{add}$ difference is 4.8 pC between the smallest and largest inputs from (1). ΔV_{integ} and ΔCode are 1.2 V and 890 from (3) and (4), respectively, and the LSB voltage is 1.35 mV. Although C_{sense} and C_{base} can be larger than C_{integ} since both C_{sense} and C_{base} are simultaneously clocked, V_{integ} is not saturated as long as $4 \cdot (C_{sense} - C_{\text{base}}) < C_{\text{integ}}$. The sensor capacitance changes due to an environment signal such as pressure. Because environmental signals change fairly slowly, a slow speed is typically acceptable for CDCs. Clocks Φ_{s1}/Φ_{s2} and Φ_{d1}/Φ_{d2} are non-overlapping 125 kHz clock pairs. To save power, 0.6 V is used for non-overlapping clock generation and digital control logic. When the 0.6 V signals pass on to the 1.2 V domain, level converters are used to shift up the voltage domain (Fig. 4).

B. Energy-Efficient Charge Subtraction

The OTAs are responsible for a significant portion of the CDC's total energy consumption, and so its bandwidth should be appropriately chosen to optimize energy. Unity gain bandwidth (ω_u) of an OTA is generally $g_{m,OTA}/C_L$ for a single-stage design where $g_{m,OTA}$ is the transconductance of the OTA input transistor pair and C_L is the OTA output load capacitance. The unity gain bandwidth is unchanged even when the OTA forms a negative feedback loop ($\omega_{u,cl} = \omega_u$). Its transfer function is $A_{0,cl}/(1 + s/\omega_{p,cl})$ [11], where $A_{0,cl}$ and $\omega_{p,cl}$ are the DC gain and the dominant pole of the loop, respectively. Assuming the DC OTA gain is much larger than the inverse of the feedback factor ($A_0 \gg 1/\beta$), $A_{0,cl}$ and $\omega_{p,cl}$ are approximated as $1/\beta$ and $\beta g_{m,OTA}/C_L$. The settling time constant of the first order system is the inverse of $\omega_{p,cl}$:

$$\tau = \frac{C_L}{\beta g_{m,OTA}} \qquad (5)$$

When the feedback is capacitive, as shown in Fig. 5, C_L becomes equal to $C_3 + C_1 C_2/(C_1+C_2)$ and $1/\beta$ is $(C_1+C_2)/C_2$. Assuming $C_3 \ll C_1, C_2$, the settling time constant becomes:
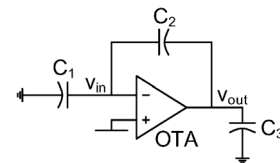
$$\tau \cong \frac{C_1}{g_{m,OTA}} \qquad (6)$$
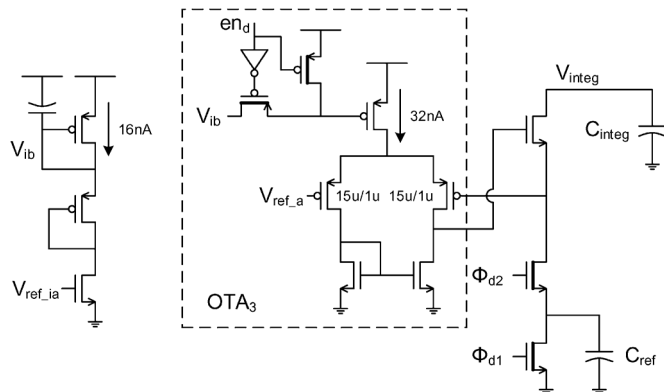
From this we see that τ is not related to the feedback capacitor (C_2), and only depends on the input capacitor (C_1).

The proposed DS-CDC opens the sensor capacitor path while only connecting the C_{ref} path during the discharge state as shown in Fig. 2 and Fig. 6. The corresponding τ is $C_{\text{ref}}/g_{m,OTA}$. C_{ref} is equivalent to the LSB of the DS-CDC. Hence C_{ref} is much smaller than C_{sensor}, allowing for significantly lower OTA tail current for a fixed sampling rate. In the proposed method, the OTA's feedback loop is modified to include a source follower, which isolates the discharge path from C_{integ} as well as C_{sensor}. The OTAs in the proposed design use a single-stage design. The OTA bias current (Fig. 6 left) is generated by a voltage reference described later. Although the OTAs use a 1.2 V supply, the current mirror uses 3.6 V, which is available in the complete microsystem described later (battery voltage); this increases V_{integ} range while keeping power low. Although the proposed CDC has an energy benefit, mismatch in the current mirror and injection at the switches can result in offsets and gain errors. These need to be calibrated for each C_{base} to obtain a complete, calibrated code over the entire range of the CDC. The power supply rejection is also limited in the proposed design and the CDC may require a supply regulator.

C. Noise Analysis and Dual Comparators

The CDC resolution is determined by the circuit noise, which is composed of sampling state noise and discharge state noise.

The sampling noise comes from the switched-capacitor integrators. In a typical implementation, as shown in Fig. 5, the input-referred noise is represented by $\overline{v_{n,c1}^2} = 7kT/3C_1$ and the output noise is described as $\overline{v_{n,o}^2} = 7kT/3C_1 \cdot C_1^2/C_2^2$. Here the OTA transconductance is assumed to be much lower than the switch transconductance [11]. Although the OTA output noise power spectrum density is proportional to $1/g_{m,OTA}$, the OTA bandwidth is proportional to $g_{m,OTA}$, and hence the
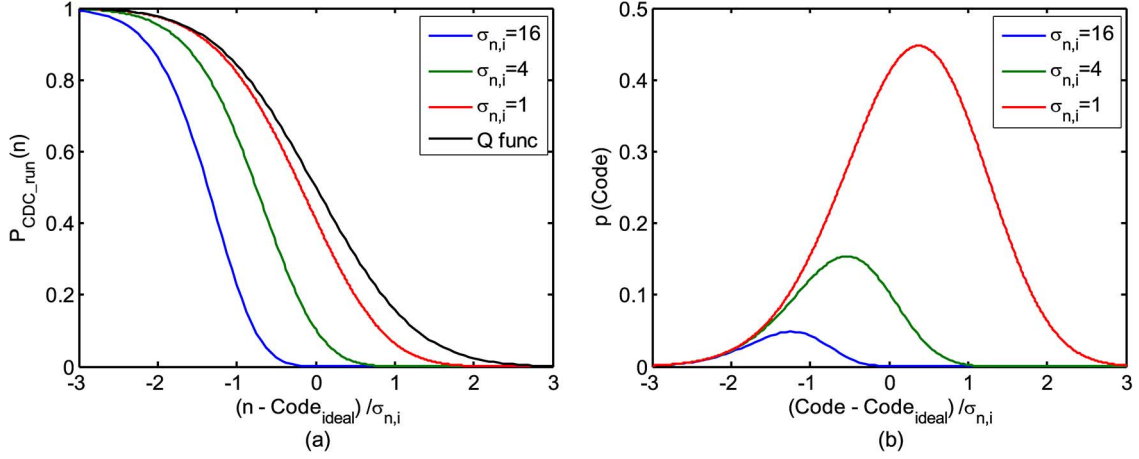
Fig. 7. Clocked comparator schematic.

sampled noise of the switched capacitor integrator is independent of $g_{m,OTA}$. This equation also applies for the proposed CDC. The noise from the sensor capacitor on the integration capacitor using the proposed OTA feedback is represented by:

$$\overline{v_{n,\mathrm{OTA,sensor}}^2} = \frac{7kTC_{\mathrm{sensor}}}{3C_{\mathrm{integ}}^2} \qquad (7)$$

In the worst-case condition where the largest C_{sensor} is used (30.7 pF), the noise is 136 μVrms. The current mirror noise can be suppressed by proper transistor sizing (large length). Similarly, the noise from C_{base} on C_{integ} ($v_{n,\mathrm{OTA,base}}$) is 115 μVrms (with 22 pF C_{base}). The noise from C_{ref} on C_{integ} ($v_{n,OTA,ref}$) is 3.2 μVrms; this is negligible and hardly affects the discharge noise.

The CDC uses clocked comparators (Fig. 7). The comparator precharges both out_c nodes and X_c nodes to 1 with $\Phi_c = 0$. When $\Phi_c = 1$, the comparator discharges those nodes with input dependent speeds and makes a comparison decision using regenerative feedback. The main noise source of the clocked comparator is thermal noise in our simulation; this causes a random decision error and the error probability follows Gaussian statistics [12].

In the proposed DS-CDC, the probability of obtaining a 1 as a function of the comparator input x can be written in the form of the Q function [13]:

$$P_1(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}\cdot\sigma_{n,i}} e^{-\frac{x^2}{2\sigma_{n,i}^2}}\, dx = Q\left(\frac{x}{\sigma_{n,i}}\right) \qquad (8)$$

where x is the comparator input normalized to LSB, and $\sigma_{n,i}$ is the input-referred comparator noise normalized to LSB. The discharge process of the CDC involves discrete and sequential events. Initially, the counter value is 0, and it counts every comparison until the comparator flips. The first flip of the comparator directly indicates the end of the conversion, while continuing iterations of the CDC imply the comparator has not yet flipped, and all previous results were 1's. The probability that the CDC is still performing a conversion at the nth cycle (P_{CDCrun}) is the cumulative product of $P_1(x)$:

$$P_{CDCrun}(n) = \prod_{i=0}^{n} P_1(i - Code_{\mathrm{ideal}}) = \prod_{i=0}^{n} Q\left(\frac{i - Code_{\mathrm{ideal}}}{\sigma_{n,i}}\right) \qquad (9)$$

where $Code_{\mathrm{ideal}} = 4(C_{\mathrm{sensor}} - C_{\mathrm{base}})/C_{ref}$. From (9), the probability density function of the code (final iteration cycle of the CDC conversion) is:

$$p(Code) = P_{\mathrm{CDCrun}}(Code-1) - P_{\mathrm{CDCrun}}(Code)$$
$$= \left(1 - Q\left(\frac{Code - Code_{\mathrm{ideal}}}{\sigma_{n,i}}\right)\right)\cdot\prod_{i=0}^{n-1} Q\left(\frac{i - Code_{\mathrm{ideal}}}{\sigma_{n,i}}\right). \qquad (10)$$

Equations (9) and (10) can be numerically solved, and they are shown with example values in Fig. 8. From (10), the expectation value and variation of $Code$ are calculated as:

$$\overline{Code_{\mathrm{comp}}} = E[Code] = \sum Code \cdot p(Code) \qquad (11)$$

$$\sigma_{Code_{\mathrm{comp}}}^2 = Var[Code] = \sum Code^2 \cdot p(code) - \overline{Code_{\mathrm{comp}}^2} \qquad (12)$$

Fig. 9 shows calculated $\overline{Code_{\mathrm{comp}}}$ and $\sigma_{Code_{\mathrm{comp}}}$ with respect to $\sigma_{n,i}$. When $\sigma_{n,i} \ll 1$ (ideal comparator), $\sigma_{Code_{\mathrm{comp}}}$ converges to $0.289 (\cong 1\sqrt{12})$ representing quantization noise, and $\overline{Code_{\mathrm{comp}}}$ converges to $Code_{\mathrm{ideal}} + 0.5$ as expected since comparator flip probability is 0.5 at $Code = Code_{\mathrm{ideal}}$. When $\sigma_{n,i} \gg 1$, $\overline{Code_{\mathrm{comp}}}$ and $\sigma_{Code_{\mathrm{comp}}}$ converge to linear expressions.

Comparator energy consumption is reduced by adopting a dual comparator scheme, composed of a coarse comparator and a fine comparator, without impacting the CDC accuracy (Fig. 2 and Fig. 10). For the energy reduction, the lower power coarse comparator is used for the most discharge cycles. After the flip of the coarse comparator, the fine comparator makes the final decision that $V_{\mathrm{integ}} < V_{\mathrm{ref\_c}}$ and determines overall accuracy. To accomplish this, the coarse comparator requires a higher reference voltage ($V_{\mathrm{ref\_cc}}$) than the fine comparator ($V_{\mathrm{ref\_c}}$) as shown in Fig. 10. The difference can be generated by two different voltage references. The coarse comparator design (720 μV rms input-referred noise, 7.4 fJ/comparison, simulated) is constrained by minimum size transistors. The fine comparator (100 μVrms noise, 450 fJ/comparison, simulated) is designed for $\sigma_{n,i} = 0.1$ with $10\times$ larger transistors and output capacitors to balance energy and noise. The converted comparison-output noises ($V_{\mathrm{LSB}} \cdot \sigma_{Code_{\mathrm{comp}}}$, $V_{\mathrm{LSB}} = C_{\mathrm{ref}}/C_{\mathrm{integ}}.V_{\mathrm{ref\_a}}$) are 780 μVrms (coarse comparator) and 402 μVrms (fine comparator, dominated by quantization noise). The reference voltages $V_{\mathrm{ref\_a}}$ and $V_{\mathrm{ref\_ia}}$ (300 mV for OTAs) as well as $V_{\mathrm{ref\_c}}$ and $V_{\mathrm{ref\_cc}}$ (600 mV for comparators) are generated using ultra-low power (60 pW) voltage references. $V_{\mathrm{ref\_a}}$ ($V_{\mathrm{ref\_ia}}$) is approximately equal to the threshold voltage difference of two different-type transistors (Fig. 11(a)), and the higher reference voltages ($V_{\mathrm{ref\_c}}$ and $V_{\mathrm{ref\_cc}}$) are generated by stacking the two references (Fig. 11(b)) [14]. The references have <2 mV resolution programmability by trimming $tcon$ and $bcon$. Each reference voltage is connected to a decoupling capacitor (4 pF). The trimming methodology consists of two steps: We initially use a large voltage difference between the two references and measure the resolution, which is determined by the fine comparator. Then, we incrementally lower the threshold voltage difference until resolution starts to degrade and select the last voltage difference where resolution was

Fig. 8. (a) Probability that the CDC is still performing a conversion at the *n*th cycle. (b) Probability density function of the code.

Fig. 9. (a) Comparison output noise. (b) Comparison output offset calculated from the comparator flip probability.

still maintained. This methodology ensures fine-comparator resolution with minimum power consumption. In simulation, a 2–4 mV comparator offset difference is sufficient to achieve the resolution of the fine comparator and results in an average usage of the fine comparator of three cycles per conversion. In the test-chip implementation it was not possible to measure the minimum necessary comparator offset difference due to a step size limitation in the testing harness.

The total noise power is calculated by adding the OTA noises and the comparator noise:

$$\overline{v_n^2} = 4\overline{v_{n,\text{OTA,sensor}}^2} + 4\overline{v_{n,\text{OTA,base}}^2} + \overline{v_{n,\text{comp}}^2} \qquad (13)$$

where $\overline{v_{n,\text{comp}}^2} = V_{\text{LSB}}^2 \cdot \sigma_{Code_{\text{comp}}}^2$. Based on the design values, $v_{n,rms}$ is calculated to 537 μVrms; this corresponds to 7.2 fF resolution. Quadruple sampling was chosen to balance the sampling noise and the discharge noise.

III. SYSTEM INTEGRATION

The proposed CDC was integrated in a complete pressure sensing system constructed from stacked IC layers to demonstrate CDC operation in an ultra-low power sensor platform [1]. Fig. 12 shows a system-level block diagram.

The system is powered by a custom 2 μAh thin-film battery with 3.6 V output, which is down-converted to 1.2 V and 0.6 V by a switched-capacitor-based power management unit (PMU)
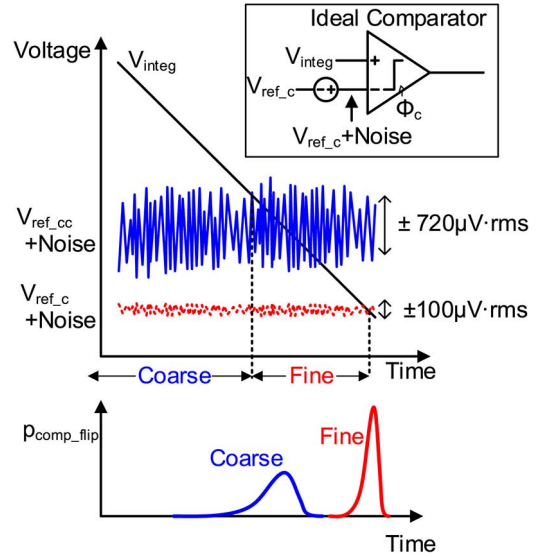
Fig. 10. Dual comparators operating concept.

in the control layer. The DS-CDC uses all three power domains: 0.6 V for digital control logic and non-overlapping clock generator, 1.2 V for most analog blocks, and 3.6 V for the current mirror. The system also includes an ARM Cortex-M0 processor and 3 kB low-power retentive (always powered on) memory
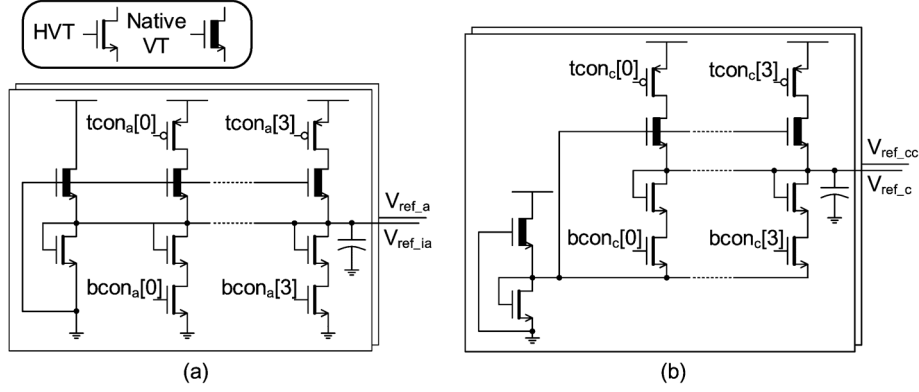
Fig. 11. 60 pW reference voltage generator for (a) the OTAs and (b) the comparators.
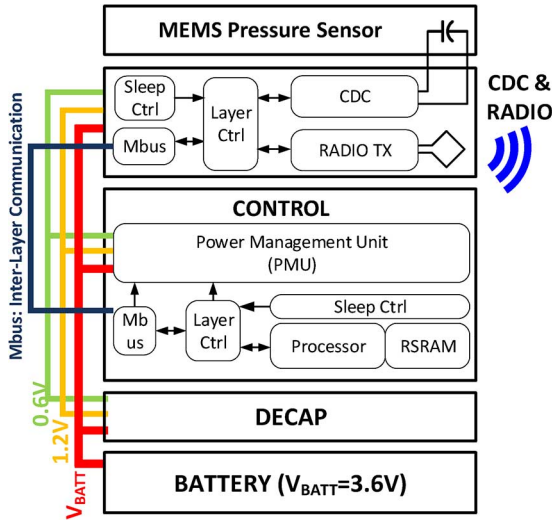
Fig. 12. System-level block diagram of the implantable pressure monitoring sensor with the proposed CDC.

Fig. 13. (a) Physical structure diagram and (b) picture without encapsulation of the proposed implantable sensing system.

in the control layer, which controls overall system operation. An on-off keying (OOK) near-field radio [2] with an on-chip coil is located on the top IC layer to enable users to collect the measured pressure data. The proposed CDC is also located on the top IC layer. The processor on the control layer communicates with the radio and CDC via an inter-layer communication (ILC) bus. A layer dedicated to providing decoupling capacitance (decap layer) is also included to ensure the supply voltages remain stable.

The entire electronics stack is placed on a MEMS pressure sensor whose two top electrodes are connected to the CDC with bondwires, as shown in Fig. 13. The sensing diaphragm of the MEMS pressure sensor faces the bottom of the stack so that it can be exposed to the ambient pressure when the upper part of the sensing system is sealed. The entire stack measures 1.4 mm × 2.8 mm × 1.6 mm, allowing minimally invasive implantation, potentially with a syringe. Fig. 14 shows die micrographs for each of the implemented IC layers.

IV. MEASUREMENT RESULTS

The CDC is implemented in 180 nm CMOS, and has an active area of 0.105 mm^2. To test CDC linearity, the bottom voltage

of C_{sensor} is swept and $C_{\text{sensor}} \cdot (V_{\text{ref\_a}} - V_{\text{sens\_bot}})/V_{\text{ref\_a}}$ is regarded as effective capacitance ($C_{\text{eff\_sensor}}$). While this test does not include the effect of the OTA loading changes, it is capable of verifying the whole range continuously. Fig. 15 shows the measurement result. By changing the C_{base} configuration from 0 to 8, which corresponds to 0 pF to 22 pF, the CDC covers $C_{\text{eff\_sensor}}$ ranging from 5 pF to 31 pF. A linearity error plot shown in Fig. 16 combines results from 9 different ranges calibrated by 2 points in each range. Maximum error is found to be 16.5 fF. The ranges are configured to overlap with an adjacent C_{base} value to avoid missing codes. For a given C_{base},
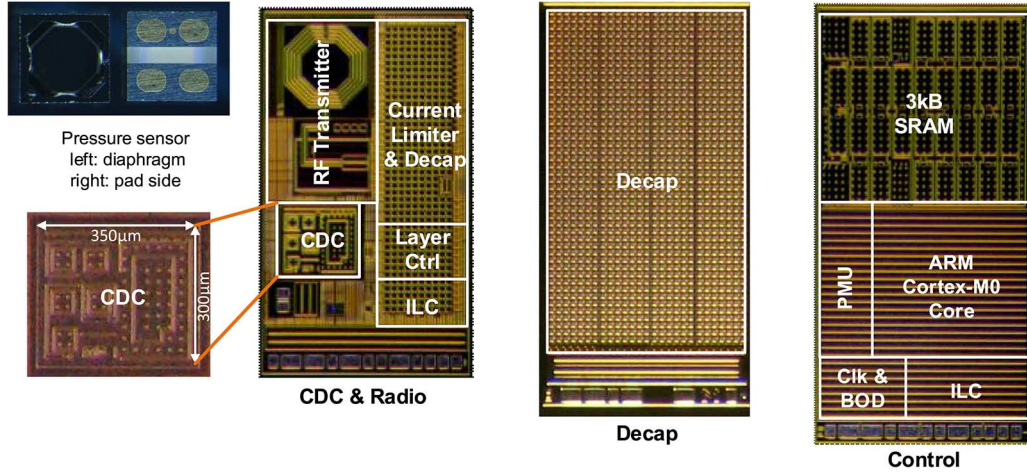
Fig. 14. Implemented IC layers and MEMS pressure sensor.
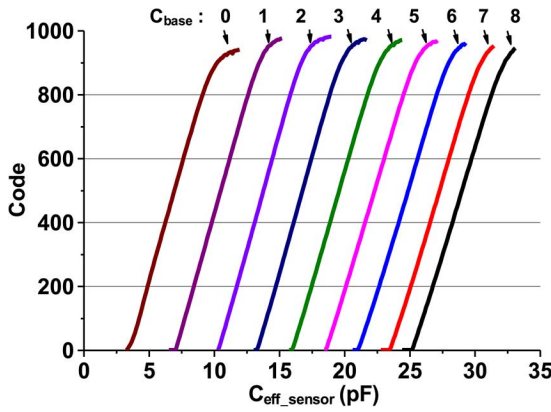
Fig. 15. Code versus effective sensor capacitor ($C_{\mathrm{eff\_sensor}}$) using voltage sweep with various C_{base} values.
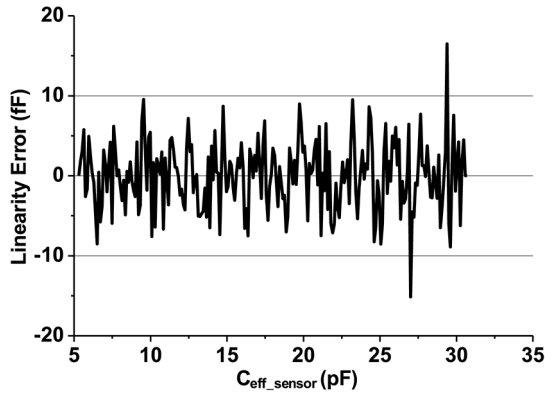
Fig. 16. Linearity error of the proposed DS-CDC with 9 different C_{base}.

Fig. 17. Power breakdown of the CDC.
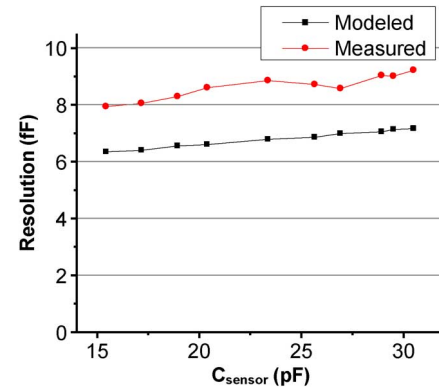
Fig. 18. Modeled and measured capacitance resolution.

a 4 pF range is measured with a linearity that is less than the maximum error.

Power and resolution are measured at the worst-case maximum input capacitance condition. Total CDC power is 112 nW, consuming 95 nW from 1.2 V, 17 nW from 0.6 V, and 0 nW from 3.6 V, and the power breakdown is shown in Fig. 17. This makes it suitable for miniature sensor node systems that often have batteries with low peak current capabilities [15]. Power from the 1.2 V supply is reduced by

13% when using the proposed dual-comparator method rather than using the fine comparator only. Power savings are limited by the parasitic capacitance on the clock network. The CDC SNR is defined as $20 \log \left(\frac{Capacitance\ Subrange/2\sqrt{2}}{Capacitance\ Resolution} \right)$ and the figure of merit (FoM) is $\frac{(Power \times Meas.Time)}{2^{(SNR-1.76)/6.02}}$. Here, $2\sqrt{2}$ is the crest-factor [16] for DC-input CDC to compare with sinusoidal-input ADCs. This SNR definition imagines that a sinusoidal continuous capacitance is given as an input with an amplitude of $Capacitance\ Subrange/2$, and the signal rms is regarded as $Capacitance\ Subrange/2\sqrt{2}$. The measured capacitance resolution is 8.7 fF, resulting in 5.3 pJ/conv·step FoM. Fig. 18 shows the measured resolution and the modeled resolution with different C_{sensor}. The measured capacitance

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH RECENTLY PUBLISHED CDCs

	This Work	[4]	[5]	[9]	[10]	[19]	[20]	[21]	[22]	[23]
Technology(μm)	0.18	0.16	0.35	0.35	0.35	0.13	0.32	0.18	0.18	0.04
Method	Dual Slope	ΣΔ	ΣΔ	PWM	PWM	Freq	PWM	SAR	ΣΔ	IDCD[4]
Input Range(pF)	5.3-30.7	0.54-1.06	8.4-11.6	1-6.8	0.8-1.2	6.0-6.3	0.5-0.76	2.5-75.3	0-24	0.7-10000
Meas. Time(ms)	6.4	0.8	0.02	7.6	0.05	1	0.033	4	0.23	0.019[5]
Power	110 nW	10.3 μW	14.9 mW	210 μW	15.8 mW	270 nW	84 μW	160 nW	33.7 μW	1.84 μW[5]
SNR[1](dB)	44.2[3]	68.4	84.8	83	45.7	29.4	40.9	55.4[3]	94.7	49.7[5]
FoM[2](pJ/c·s)	5.3[3]	3.8	21	140	5000	11	98	1.3[3]	0.18	0.14[5]

[1] $\text{SNR} = 20 \log \left(\frac{Capacitance\ Range/2\sqrt{2}}{Capacitance\ Resolution} \right)$.

[2] $\text{FoM} = \frac{Power \times Meas.Time}{2^{(SNR-1.76)/6.02}}$.

[3] Calculated with one subrange.

[4] Iterative delay-chain discharge.

[5] Measured with 11.3 pF.
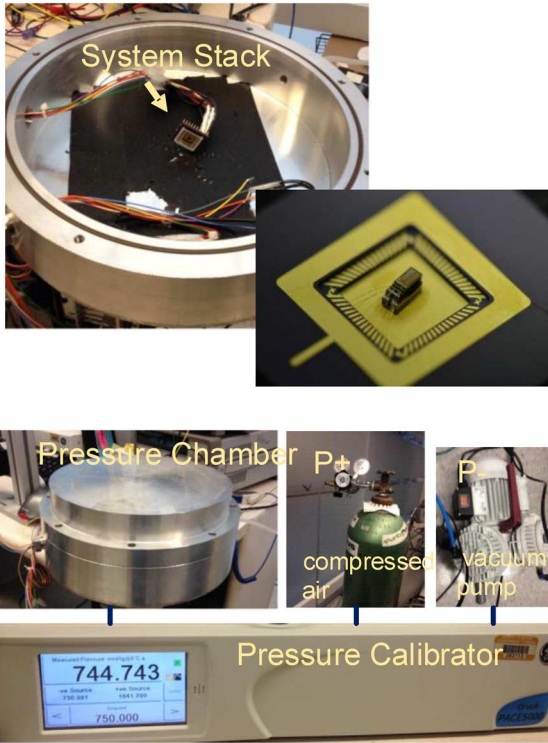
Fig. 19. Pressure measurement set-up for the CDC integrated in an implantable pressure sensing system.

Fig. 20. Pressure measurement result with $C_{\text{base}} = 4$ and 32 OSR, taken using the complete pressure-sensing system in a pressure chamber.

measurement results achieving a linear output response with $R^2 = 0.9995$. The chamber pressure was swept from 740 to 840 mmHg, which is a sufficient range for various body pressure diagnoses, including intra-ocular, intra-cranial, and intra-abdominal pressures [17]. The MEMS pressure sensor used in this experiment has high linearity in this region [18], and the corresponding capacitance range is overlaid in Fig. 20. During this test, C_{base} was set to 4, and $Code$ is the total count. The measured power sensitivity of the system was 0.4 mmHg/mV for 3.6 V and 4.0 V supplies without calibration. During the system measurement, the PMU generated relatively large fluctuations on the power supply nodes and the processor was also running introducing possible additional noise. Given the sensitivity of the CDC to supply variation, the CDC was operated with an over-sampling rate (OSR) of 32 and achieved a resolution of 0.77 mmHg with 200 ms conversion time. The long-term CDC supply sensitivity can bead dressed with two-pressure-point calibration as its linearity is preserved across voltage. Since a pressure sweep during calibration represents the most time-consuming and expensive process, multiple readings can be taken at different supply voltages for each pressure and then stored in a look-up table. In operation, a low sample rate ADC would read the supply voltage to index

resolution is within 20% of the estimated resolution from (13), providing reasonable matching between theory and experiment. Table I summarizes CDC performance and compares with the previously reported CDCs.

The proposed CDC is integrated in a pressure-sensing system as described in Section III and tested as a pressure sensor. Fig. 19 shows the test set-up for pressure measurement. The sensing system is wirebonded to a PGA socket and it was placed in an aluminum pressure chamber. The pressure inside the chamber was controlled by a pressure calibrator where compressed air and vacuum are supplied externally. Using the bonded wires, an external 3.6 V supply overrode the battery, and the ILC bus read the CDC data. Fig. 20 shows the pressure
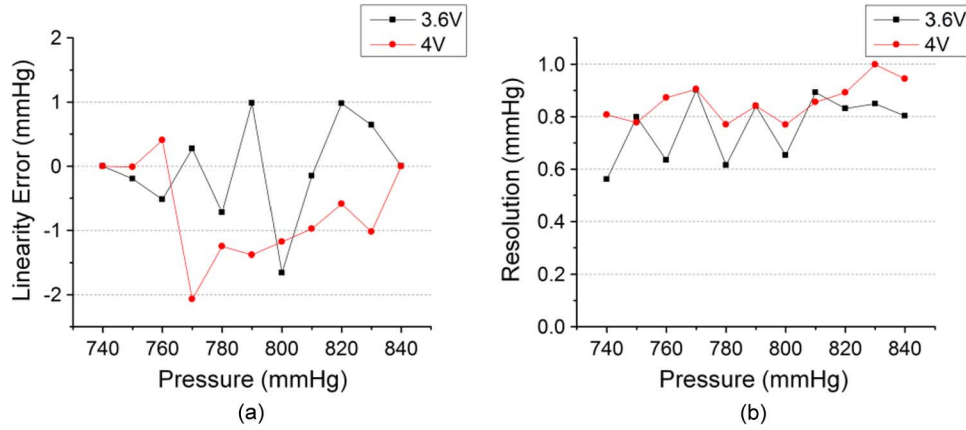
Fig. 21. Pressure sensing system measurement. (a) Linearity error with two-pressure-point correction. (b) RMS resolution for 3.6 V and 4.0 V operation.
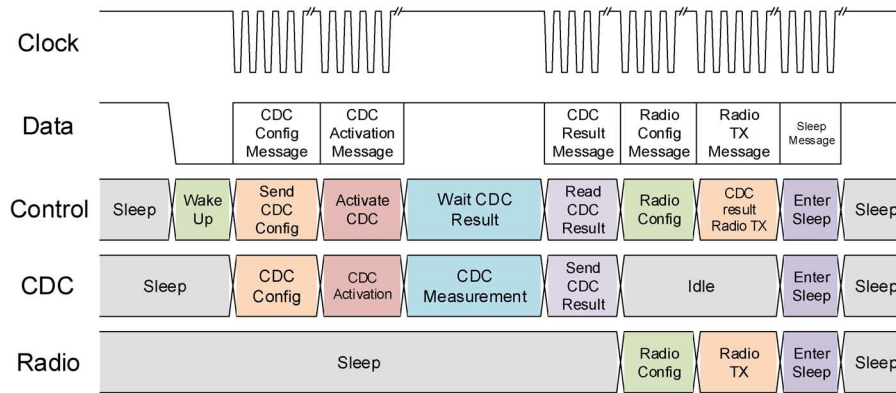

Fig. 22. Operation sequence of the implantable pressure-sensing system.

into the look-up-table. Using this manner of two-pressure-point correction, the linearity error and resolution become less than 2 mmHg and 1 mmHg, respectively, for 3.6 V and 4.0 V supply across 740 to 840 mmHg as shown in Fig. 21 with fairly small added testing time and cost beyond a single-Vdd dual-pressure calibration. However, since a low sampling rate ADC was not available in our system at the time of testing, the system level performance and power overhead of this supply voltage calibration was not quantified.

Fig. 22 shows an example operation scenario of the sensing system. The sensor system typically spends most of its time in a low-power sleep mode (<8 nW) to save power. Then it periodically wakes up and enters active mode (~ 50 μW) for measurement operation. As the system wakes up, it first initializes the CDC and then initiates pressure measurement. Upon completion, the digital pressure value is stored to memory and can be accessed for later radio transmission. In this example, the data is immediately transmitted through the radio after each pressure measurement. The system then returns to sleep mode. Each pressure measurement cycle consumes 6.5 μJ, and so the 2 μAh battery corresponds to 17.7 days of operation capacity (assuming the pressure is recorded every 10 minutes). Fig. 23 shows measured waveforms of the ILC wires and battery current. The ILC activity indicates the processor in the control layer is interacting with the CDC and the radio on the top IC layer. As the system wakes from the low power sleep
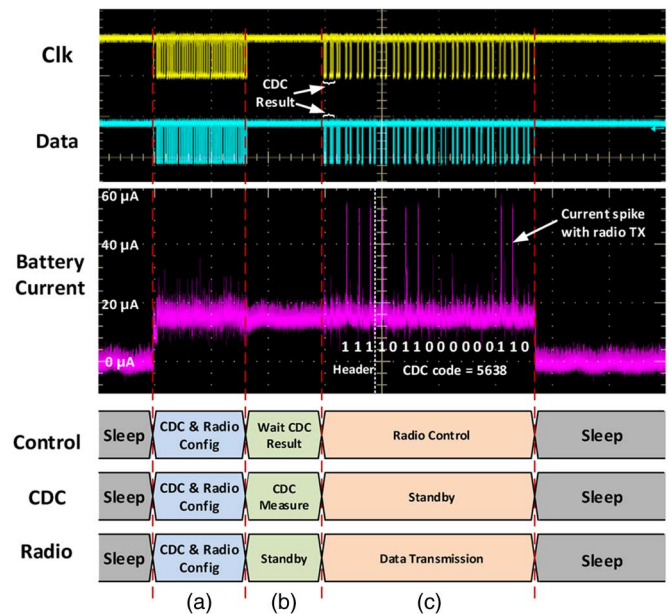
Fig. 23. Measured waveforms for the sensing system operation.

mode, the current consumption jumps to ~ 20 μA. The ILC activity in part (a) indicates that the CDC is configured, and pressure measurement is activated. During the CDC activation

in part (b), no ILC activity is required until the result is sent back to the memory in the early part of (c). In the remainder of part (c), the processor controls the radio to send out pulses; whenever the radio transmits a pulse, a battery current spike can be clearly observed. After the radio transmission, the current consumption drops to <8 nA as the system enters sleep mode to save power.

V. Conclusions

This paper proposed an energy-efficient DS-CDC suitable for implantable pressure sensing systems. Pressure sensors often have large base capacitance, while their variation is small. The CDC removes this base capacitance using a configurable capacitor bank that zooms in on the capacitance variation and reduces conversion time and energy. The CDC uses three different supply voltages (0.6, 1.2, 3.6 V) that are available in the system to optimize energy. By isolating the reference capacitance from the relatively large neighboring sensor capacitor, the OTA bias current can be reduced to 32 nA. Dual-precision comparators are used in conjunction to achieve the high resolution of the fine comparator and low energy of the coarse comparator. The proposed CDC achieves 8.7 fF resolution, 5.3 pJ/conv·step FoM, which is in reasonable agreement with the theoretical noise analysis for the circuit. In addition, we demonstrated a complete 1.4 mm $\times$ 2.8 mm $\times$ 1.6 mm pressure sensor system with a MEMS pressure sensor, processor, memory, PMU, battery, ILC, and radio. This system was tested in a pressure chamber with an external 3.6 V supply and OSR of 32 and achieved 0.77 mmHg resolution with good linearity ($R^2 = 0.9995$).

Acknowledgment

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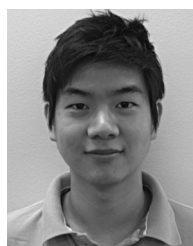
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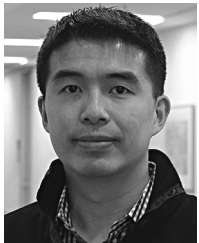Dr. Lee has received a Samsung Scholarship and an Intel Ph.D. fellowship.
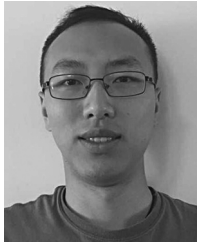
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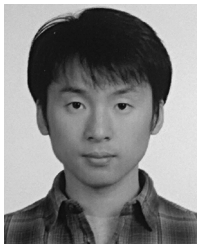
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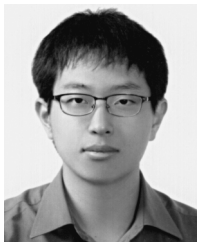
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