19.6 A 2.5nJ Duty-Cycled Bridge-to-Digital Converter Integrated in a 13mm³ Pressure-Sensing System

Sechang Oh[1], Yao Shi[1], Gyouho Kim[1,2], Yejoong Kim[1,2], Taewook Kang[1], Seokhyeon Jeong[1,2], Dennis Sylvester[1], David Blaauw[1]

[1]University of Michigan, Ann Arbor, MI; [2]CubeWorks, Ann Arbor, MI

Small form-factor piezoresistive MEMS sensors, often configured in a Wheatstone bridge, are widely used to measure physical signals such as pressure [1-3], temperature [4], force [1], and gas concentration. A common method to realize a digital output from the bridge involves biasing the bridge with a DC voltage source and using a low-noise amplifier followed by an ADC. While a bridge measurement can achieve high resolution and linearity, it is very power hungry [3] because the bridge resistance is low (typically 1-10kΩ). Both the high power and high instantaneous current make it unsuitable as a sensing interface in miniaturized microsystems with battery capacities of <10μAh and ~15kΩ internal resistance [5]. Duty cycled excitation was proposed in [1] to reduce power in moderate dynamic range (DR) applications, lowering bridge excitation energy by up to 125× compared to static biasing. However, the excitation energy consumption (~250nJ) is still much larger than the interface circuit conversion energy, and therefore limits overall sensor energy efficiency. To address this challenge, we propose an energy-efficient highly duty-cycled excitation bridge-sensor readout circuit for small battery-operated systems. Due to high battery resistances, the excitation voltage (V_{EX}) is sourced from an on-chip decoupling capacitance that drops ~100mV during excitation and then slowly recharges from the battery. To avoid accuracy degradation from this voltage fluctuation, the design samples not only the inputs ($V_{IN+/-}$) but also V_{EX}, from which it generates a DAC reference voltage (V_{DAC}). We also propose an offset calibration and input-range matching method. We demonstrate operation of the bridge-to-digital converter (BDC) integrated with a complete and fully functional pressure-sensing system, including a processor, battery, power management unit, RF transmitter, and optical receiver.

Figure 19.6.1 shows the structure of the bridge-sensor interface circuit. The BDC provides V_{EX} to the bridge and senses $V_{IN+/-}$ and V_{EX} with a sampling circuit, followed by V_{DAC} generation, SAR ADC, and an FSM. An RC-relaxation oscillator generates an internal 17.2kHz clock and the FSM is controlled by a bus controller, which connects to other chips in the microsystem. A sampling pulse generator applies a short pulse (SPL) to sampling switches for V_{EX}, the V_{EX} sampling capacitor (C_{EXS}), and input sampling capacitors (C_S). The value of C_S and SPL pulse width are determined by the input resolution requirement. We target 200μV $V_{IN+/-}$ resolution at 3.6V V_{EX}. C_S is set to 4pF so that kT/C noise is <50μV and SPL width is set to 170ns to satisfy >10b accuracy with the RC settling of $V_{IN+/-}$. The bridge is exposed to the supply voltage for only 170ns within the 1ms total conversion time, enabling bridge power consumption to be 6000× less than conventional DC biasing.

Figure 19.6.2 shows the detailed implementation of V_{EX} and V_{DAC} generation circuits. Since V_{EX} is at ground for most of the conversion time and its large V_{SD} and V_{GD} voltage incurs significant GIDL current, these circuits use GIDL reduction devices G1 and G2. SPL is generated by an inverter delay chain, which is 4b-programmable from 60 to 240ns. Once propagation reaches a selected stage, the remainder of the delay chain is gated to reduce energy consumption. Since battery internal resistance is high, it cannot directly supply the bridge excitation current. Instead, sampling current is provided from a 0.48mm² 1.2nF on-chip decoupling capacitor (C_{DECAP}) made up of M1-M4 MOM and MIM. V_H drop is ~100mV during sampling and it is then slowly restored by the battery during subsequent conversion phases. To avoid negative impact of this supply voltage fluctuation effect during ADC conversion, it is necessary to dynamically adjust the conversion to the reduced V_{EX} at the end of excitation. To achieve this, a DAC reference voltage (V_{DAC_REF}) is internally generated by sampling V_{EX} with C_{EXS} (4pF) when SPL=1. Then, V_{DAC_REF} is multiplied by 10/11 to provide >200mV V_{DS} to ensure transistors are in saturation within the amplifier that generates the final regulated output V_{DAC}. Simulated amplifier PSRR is –56dB. The amplifier is designed for 30kHz bandwidth and 60μV integrated noise and draws 160nA. By sampling the excitation voltage in this way, the BDC is also insensitive to supply variation, which is important for sensor nodes operating on small batteries and hence often unstable supplies. The BDC timing diagram is shown in the bottom left of Fig. 19.6.2. After ST_SPL pulses, PREP_VDAC is on and acts to multiply V_{DAC_REF} by 10/11. V_{DAC} settles during the on period of PREP_VDAC, after which the bit-cycle phase is entered.

Figure 19.6.3 shows the proposed SAR ADC with input range matching and offset calibration features. In conventional SAR ADCs, the input voltage is sampled to a binary DAC array. However, in such an implementation such an approach would require $V_{IN+/-}$ to drive >12pF for linearity in the target process technology, increasing the sampling time constant and V_{EX} energy by 3×. Targeting a 4pF sampling capacitor instead (as determined by kT/C constraints), C_S is separated from the DAC [6] as shown. Bridge sensor resistance changes at most a few % at full-scale input. To match the input range of the bridge an additional MSB DAC is used. To accommodate an input range from ±50 to 100mV the MSB DAC is implemented with 31b unary capacitors with selection switches. The MSB DAC uses a split-DAC structure to reduce both total DAC capacitance and V_{DAC} amplifier current, which is proportional to the total DAC capacitance load for the same bandwidth constraint as the DAC settling constraint.

During the sampling phase, the DAC purges all its charges while the input is sampled on C_S. To avoid the power consumption of a common-mode reference voltage generation, the DAC uses only V_{DAC} and ground. At the beginning of the bit-cycling phase, the DAC top plate (V_X) connects to the left plate of C_S (V_Y). C_S charge is conserved during the bit-cycling phases, and V_Y change is directly coupled to the comparator input. The comparator operates at 1.2V (V_{1P2}) to reduce power while the DAC operates at 3.3V (V_{DAC}). The comparator is a conventional two-stage clocked comparator with 400fF internal loading capacitor to enhance noise performance. During the transition the common-mode voltage is shifted to the correct range (0V < V_Z < 1.2V) by adjusting the M code of the MSB DAC. The BDC can optionally run offset calibration. It operates with shorted inputs (SHRT=1) and B_{OS}=512 during the calibration, and its output is set as B_{OS} in normal operation. The remainder of the conversion process is identical to a conventional SAR ADC. In order to accommodate multiple applications that require different resolution, the BDC conversion can be oversampled with an oversampling rate (OSR) of 1 to 256. This approach repeats the entire conversion process OSR times and accumulates the output codes.

The proposed BDC was integrated in a stacked sensor node system (Fig. 19.6.5, left) composed of a MEMS pressure sensor, battery, and 6 IC layers: radio, decap, processor, energy harvester, photovoltaic cells, and power management unit. The system is powered by two 8μAh thin-film batteries with 3.6-to-4.1V output voltage, which is downconverted to 1.2V and 0.6V by the switched-capacitor power management unit. The system includes 8kB SRAM and an ARM Cortex-M0 processor, which controls BDC operation. The MEMS pressure sensor is on top of the entire stack with a pressure-sensitive top diaphragm. The four electrodes are directly wirebonded to the proposed BDC chip.

The BDC was implemented in 0.18μm CMOS technology with an area of 1.7mm². The BDC output was measured with different MSEL (# of C_M selected) and input voltages (Fig. 19.6.4, top left). MSEL changes the slope and input range from 45 to 110mV. Measured SNR is 46 to 51dB across MSEL from 12 to 31 (Fig. 19.6.4, bottom left). BDC line sensitivity is measured at 3.6, 3.8, and 4.0V V_H (Fig. 19.6.4, top right). The codes shift 0.07code/mV. Total BDC conversion energy is 2.5nJ and Fig. 19.6.4 (bottom right) provides its breakdown from measurement. Testing the BDC with the pressure sensor is shown in the top right of Fig. 19.6.5. With OSR of 4 it achieves 1.1mmHg resolution at 4ms conversion time. The complete sensor system was tested and is fully functional, as shown by system operation in Fig. 19.6.5 (bottom right). The system periodically wakes up from a sleep mode and enters an active mode by releasing power gates and isolation gates, turning on its RC clock, and executing the BDC. Measured data is saved to SRAM and can be transmitted out by radio when needed. Figure 19.5.6 summarizes the BDC and overall system performance from measurement, and also compares it with previous related BDC work.

References:
[1] R. Grezaud, et al., "A Robust and Versatile, –40°C to +180°C, 8Sps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications," IEEE Symp. VLSI Circuits, pp. C310-C311, June 2017.
[2] T. T. Nguyen, et al., "An Energy-Efficient Implantable Transponder for Biomedical Piezo-Resistance Pressure Sensors," IEEE Sens. J., vol. 14, no. 6, pp. 1836-1843, June 2014.
[3] H. Jiang, et al., "An Energy-Efficient 3.7nV/√Hz Bridge-Readout IC with a Stable Bridge Offset Compensation Scheme," ISSCC, pp. 172-173, Feb. 2017.
[4] S. Pan, et al., "A CMOS Temperature Sensor with a 49fJK2 Resolution FoM," IEEE Symp. VLSI Circuits, pp. C82-C83, June 2017.
[5] S. Oh, et al., "A Dual-Slope Capacitance-to-Digital Converter Integrated in an Implantable Pressure-Sensing System," IEEE JSSC, vol. 50, no. 7, pp. 1581-1591, July 2015.
[6] S. Jeong, et al., "A 12nW Always-on Acoustic Sensing and Object Recognition Microsystem Using Frequency-Domain Feature Extraction and SVM Classification," ISSCC, pp. 362-363, Feb. 2017.
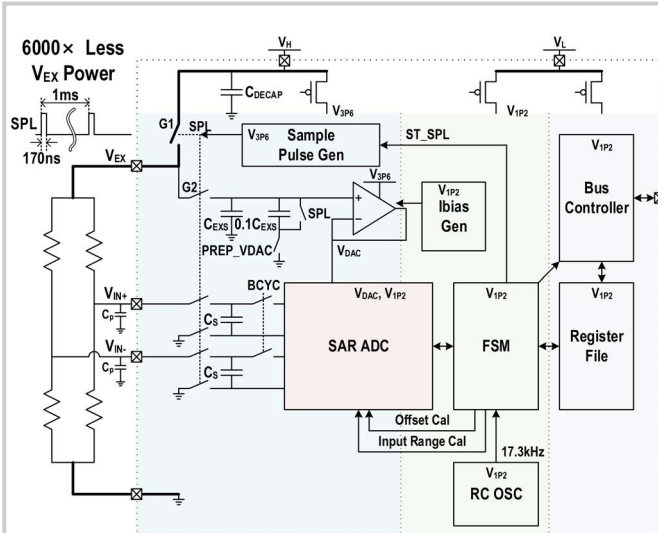
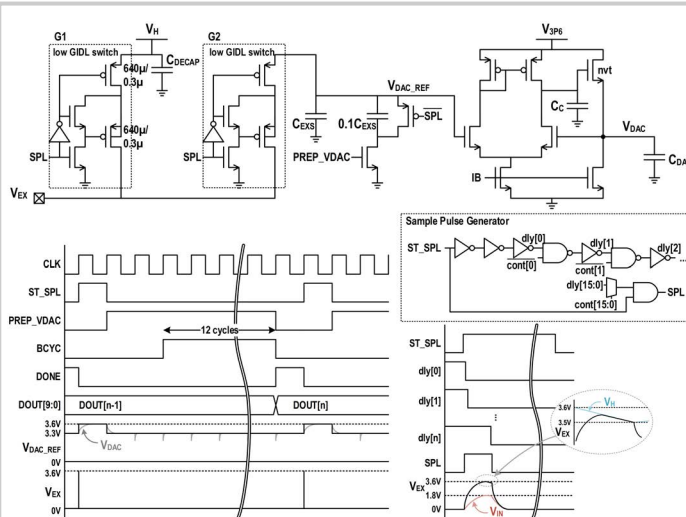Figure 19.6.1: Structure of the bridge-sensor interface circuit.

Figure 19.6.2: Detailed implementation of V_{EX} and V_{DAC} generation and BDC timing diagram.
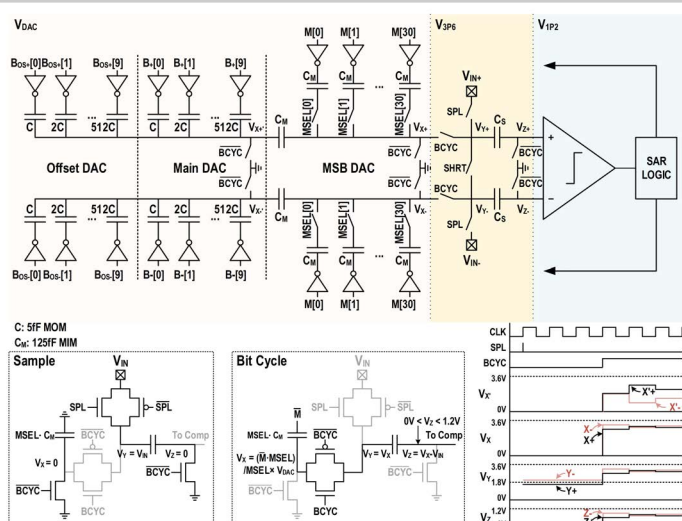

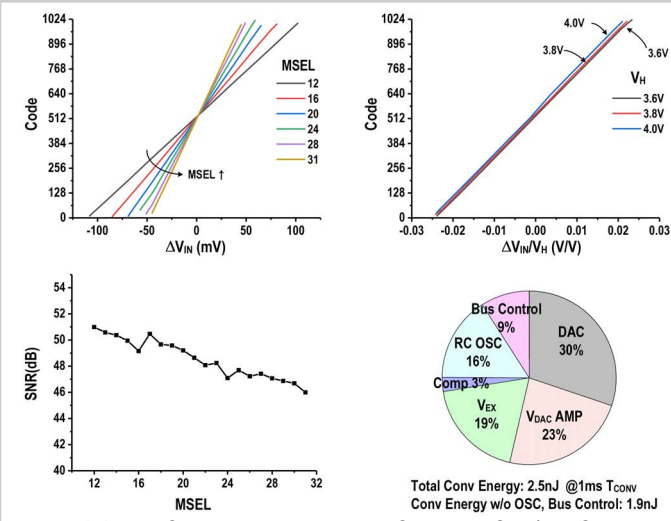Figure 19.6.3: Implementation of 10b ADC with range matching and offset calibration.

Figure 19.6.4: BDC Measurement results of Code vs. MSEL (# of C_M selected) and V_{IN} (top left), Code vs. V_H and V_{IN} (top right), SNR vs. MSEL (bottom left), and conversion energy breakdown (bottom right).
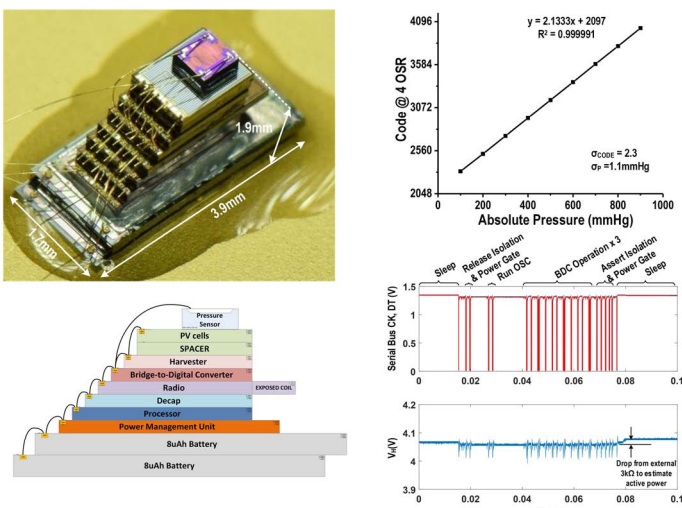

Figure 19.6.5: The proposed 3D stacked pressure-sensing system and the measurement results.

	This Work	This Work OSR=4	VLSI 2017 [1]	Sens J 2014[2]	ISSCC 2017[3]
Technology (nm)	180		180	90	180
Supply Voltage (V)	1.2, 3.6		1.8	1	1.8
Supply Current (µA)	0.65 @1.2V, 0.52 @3.6V		140	52	1200 @1.8V, 1500 @5V
Bridge Voltage (V)	3.6		1.8	1	5
Bridge Resistance (kΩ)	6		1	12	3.3
Conv. Time(µs)	1000	4000	1000	96	500
Energy/Conv exclude Bridge (nJ/Conv)	2	8	61	1.88	1080
Energy/Conv include Bridge (nJ/Conv)	2.5	10	246	5	4870
+/-Input Range(mV)	68		16	12.8	10
SNR (dB)	49.2	54.2	59.0	44.1	95.5
FOMW[1] (pJ/c.s.)	10.6	23.9	337.9	38.3	100.0
FOMS[2] (dB)	132.2	131.2	122.1	124.1	145.6

$$^{1}FOMW = \frac{E_{CONV\_INC\_BRIDGE}}{2^{(SNR-1.76)/6.02}}$$

$$^{2}FOMS = SNR(dB) + 10\log\left(\frac{1}{2E_{CONV\_INC\_BRIDGE}}\right)$$

Figure 19.6.6: Performance summary and comparison.

19

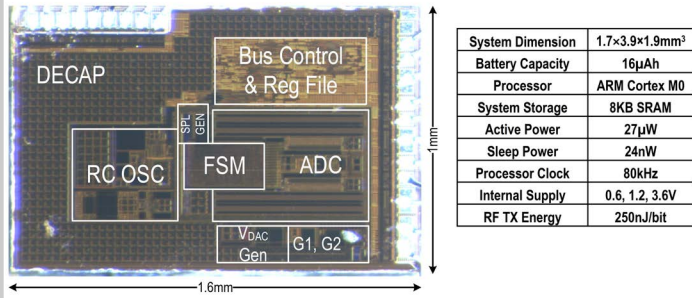| System Dimension	1.7×3.9×1.9mm³
Battery Capacity	16µAh
Processor	ARM Cortex M0
System Storage	8KB SRAM
Active Power	27µW
Sleep Power	24nW
Processor Clock	80kHz
Internal Supply	0.6, 1.2, 3.6V
RF TX Energy	250nJ/bit

Figure 19.6.7: BDC die micrograph and system specification.