A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation

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Abstract

A key challenge in the design of on-chip wake-up timers for compact wireless sensor nodes is to achieve high timing accuracy over temperature and supply voltage variation within an ultra-low power budget. We propose a gate-leakage-based frequency-locked timer with first- and second-order cancellation achieving 260 ppm/°C from −5 to 95°C. The timer consumes 224 pW at 90 Hz output frequency with 0.93%/V supply voltage dependence in the 1.1-3.3 V range.

Introduction

Wake-up timers are a critical component of wireless sensor nodes (WSNs) for the Internet of Things. Since they are on even when the sensor node is in sleep mode, they must consume extremely low power. In addition, they should ensure high timing accuracy for synchronization between devices and general timekeeping while remaining compact, leading to a highly constrained design space. An RC oscillator [1] or frequency-locked oscillator [2] based on temperature-compensated resistors achieves frequency stability across temperature of <50ppm/°C. However, these approaches consume ~100 nW or more, which far exceeds the power budget of state-of-the-art ultra-low power sensors. Extending these approaches to sub-nW requires extremely large resistors, unacceptably increasing the area and cost. Recently, a switch-resistor based timer achieved a high effective resistance without increasing resistor size and obtained a temperature coefficient (TC) of 13.8 ppm/°C [3]. However, the approach requires large capacitors, and power consumption remains relatively high at 4.7 nW. An alternative to resistor-based timers is gate-leakage-based timers; several such timers have been proposed [4-5], providing sub-nW power consumption in compact silicon area. However, gate leakage exhibits significant first- and second-order temperature dependence, complicating temperature compensation, and it is also sensitive to the gate voltage. As a result, previous gate leakage timers have TCs in excess of several hundred ppm/°C and line sensitivities (LS) >150%/V. The gate leakage timer in [5] achieves 31 ppm/°C but requires 10-point calibration, and its 660 pW power consumption does not include the power of a required auxiliary temperature sensor. Further, its LS is unacceptably high at 420%/V.

This paper proposes a 224-pW gate-leakage-based frequency locked timer with first- and second-order temperature dependency cancellation, yielding a TC of 260 ppm/°C across −5 to 95°C. Supply insensitive reference voltage generators and an on-chip low dropout (LDO) regulator decrease LS to 0.93%/V for 1.1−3.3 V, which marks a 150× improvement compared to previous gate-leakage-based timers.

Proposed Circuit

The proposed design uses a frequency locked oscillator scheme [2,3] in which current I_1, set by the gate leakage of a standard-Vth NMOS N_1, is matched with current I_2, using modulation of the frequency of a switched capacitor C_2 (Fig. 1). The measured temperature dependence of N_1 gate leakage shows both first- and second-order components (Fig. 2). It is essential to cancel both components to achieve a good TC. In the proposed design, we use two tuning mechanisms. We cancel the first-order dependence by varying V_2 in a proportional to temperature (PTAT) fashion using a voltage reference with tunable temperature dependence (Fig. 1, right). This PTAT reference consists of two PMOS diode stacks, each with different threshold voltages and sizes to create a first-order dependence on temperature (Fig. 3b). Switches control the high-Vt PMOS size, which tunes the slope of V_{PTAT} from 0.5 to 0.68%/°C (simulation).

To cancel the second-order dependence, we use a 2T voltage reference, which has intrinsic convex temperature dependence [6] (Fig. 3a). However, the convexity of this reference is fixed and is not easily tuned to cancel the second-order dependence of gate leakage. Hence, we leverage the exponential dependence of gate leakage on voltage to provide this tuning mechanism, as follows: First, we remove first-order dependence by tuning the native NMOS and High-Vt PMOS sizes, resulting in $V_{2T} = V_{2T,0}+\alpha(T-T_0)^2$. We then amplify V_{2T}, and a mux structure selects the output voltage $V_{REF} = V_1 = k_{mux}(V_{2T,0}+ \alpha(T-T_0)^2)$ where k_{mux} varies with the mux selection. Note that this does not change the relative magnitude of the convexity of V_1. However, gate leakage I_1 is exponentially dependent on V_1, resulting in $I_1 \propto \exp(\beta k_{mux} V_{2T,0}) \times \exp(\beta k_{mux} \alpha (T- T_0)^2)$. Hence, by changing k_{mux} (i.e., the mux setting) we can modulate the relative magnitude of the convexity of I_1, which allows us to cancel the second-order temperature dependence of the gate leakage. Fig. 3c shows simulation results of this approach. After both first- and second-order temperature dependencies are canceled, only third- and higher-order terms remain. Finally, the center frequency (0^{th} order) is adjusted by tuning C_2 in Fig. 1.

Two PMOS devices (P_1 and P_2, Fig. 1) implement the current mirror. The devices are high threshold thick-oxide PMOS transistors operating in subthreshold with V_{DS} >5 kT/q, which significantly reduces mismatch between I_1 and I_2. The low power voltage controlled oscillator (VCO) in Fig. 1 provides the timer's output frequency and is composed of stacked high threshold inverters to minimize short circuit current (Fig. 4). The voltage range of V_{CTRL} across temperature, 0.67-0.9 V, is too narrow and situated at too high a voltage to compensate the VCO frequency across temperature. We double the voltage range and shift it lower using switch capacitor C_4, obtaining V_{CTRL}' with range 0.2-0.65 V. Capacitors C_3-C_5 also generate the dominant pole of the frequency lock scheme.

Gate leakage has high voltage sensitivity, leading to strong frequency dependence on supply voltage in previous gate-leakage-based timers. The proposed design addresses this by placing native NMOS transistors in the convex voltage generator and PTAT voltage generator, enabling low line sensitivity (1.3%/V and 2.2%/V, respectively, simulation). An on-chip LDO further reduces supply voltage dependence while consuming only 18 pW (simulation).

Measurements

The proposed gate-leakage-based timer was implemented in 55nm CMOS (MIFS C55DDC) in 0.057 mm^2. Fig. 5 show the measured frequency variation from −5 to 95°C for five typical corner dies. Fig. 5a gives results with no tuning, while Fig. 5b has 2-pt calibration to cancel first-order dependence. Fig. 5c uses the proposed second-order cancelation with 3-pt calibration, yielding measured TCs of 175−343 ppm/°C, which is 5× better than first-order cancelation only. The timer consumes 224 pW at 25°C with 90 Hz output frequency; power increases to 1.2 nW at 95°C (Fig. 8). Line sensitivity is 0.33−1.29%/V across 1.1−3.3 V supply voltage for the five dies (Fig. 6). Fig. 11 compares TC, LS, and energy per cycle to those of previous sub-nW timers and resistor-based timers. The proposed timer is Pareto optimal in terms of TC and LS vs. power among the listed works, enabling a new ultra-low power timer design space. Energy per cycle of 2.49 pJ/cycle is comparable to the best reported among the listed works.

References

[1] D. Griffith *et al*., ISSCC, 2014. [2] M. Choi *et al*., JSSC, Sep. 2016.
[3] T. Jang *et al*., ISSCC, 2016. [4] H. Wang *et al*., JSSC, Jun. 2016.
[5] Y. Lee *et al*., JSSC, Oct. 2013. [6] M. Seok *et al*., JSSC, Oct. 2012.
[7] P. M. Nadeau *et al*., JSSC, Apr. 2016.

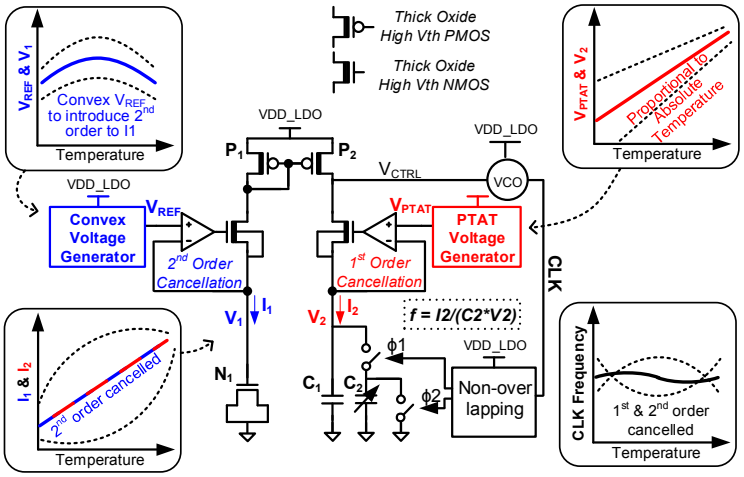

Fig. 1. Proposed gate leakage based frequency locked timer.

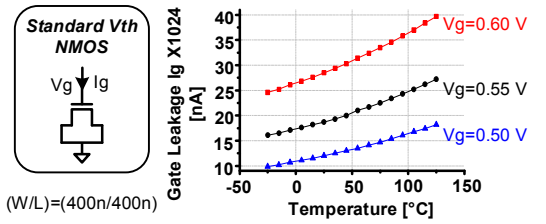

Fig. 2. Measured gate leakage current across temperature in 55nm CMOS.

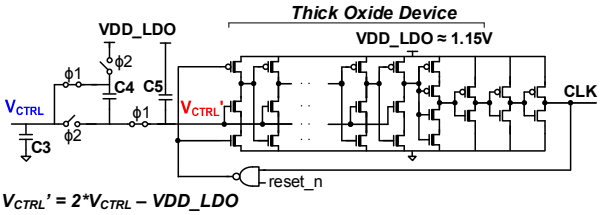

Fig. 4. Diagram of stacked inverter VCO with switch capacitor voltage doubler.

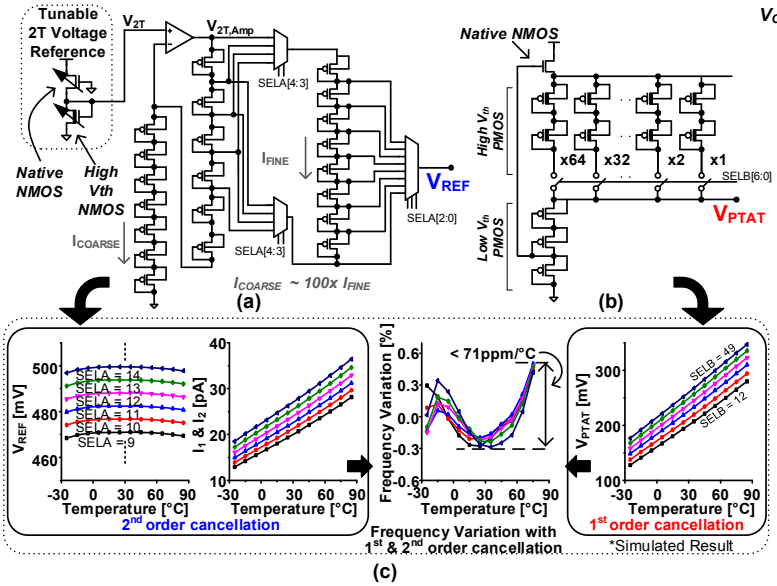

Fig. 3. (a) Proposed convex voltage generator (b) PTAT voltage generator and (c) simulation result of first- and second-order cancellation.

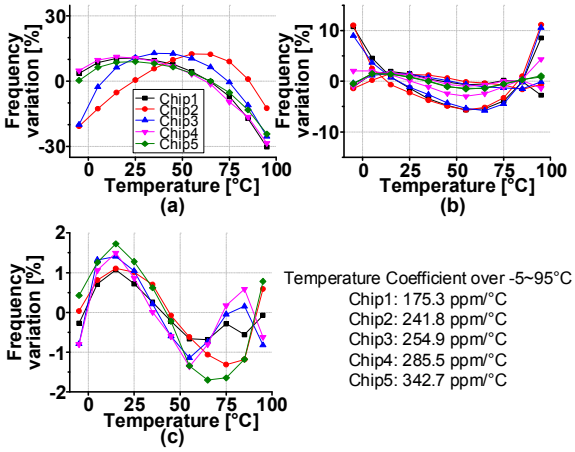

Fig. 5. Measured frequency variation over temperature: (a) without calibration (b) with 2-pt and (c) with 3-pt calibration.

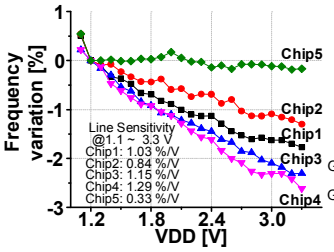

Fig. 6. Measured line sensitivity of output clock frequency.

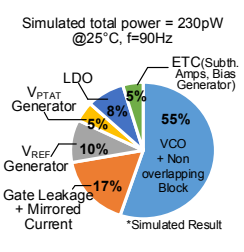

Fig. 7. Simulated power breakdown of timer

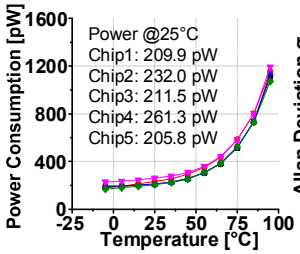

Fig. 8. Measured power consumption

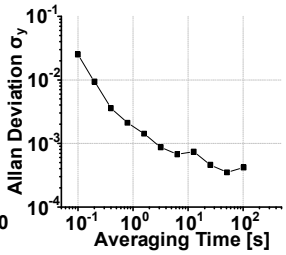

Fig. 9. Measured Allan deviation

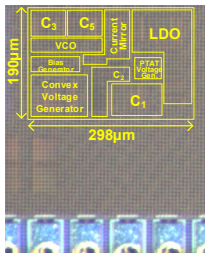

Fig. 10. Die photo.

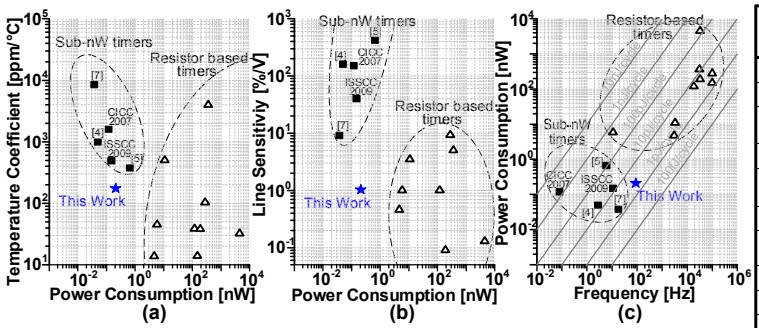

Fig. 11. Comparison scatter plots with previous work (best reported dies): (a) temperature coefficient (b) line sensitivity and (c) energy per cycle

Table1. Comparison table

	This Work	JSSC 2016 [7]	JSSC 2016 [4]	JSSC 2013 [5]	ISSCC 2009 (Y.-S. Lin)	CICC 2007 (Y.-S. Lin)
Process [nm]	55	180	65	130	130	130
Supply Voltage [V]	1.2	1.8 / 0.6	0.5	0.7 & 1.2	0.6	0.45
Power [pW]	206~261 (avg 224[a])	38 / 4.2	30 ~ 50[b] (avg 44[a])	660[c]	150	120
Frequency [Hz]	90	18	2.8	6	11	0.08
Temp. Coeff. [ppm/°C]	175~343 (avg 260[a])	8500 / 21000	990~2200[b] (avg 1260[a])	375 (31[d])	490	1600
Temp. Range [°C]	-5 ~ 95	-30 ~ 60	-40 ~ 60	-20 ~ 60	0 ~ 90	0 ~ 80
Line Sensitivity [%/V]	0.33~1.29 (avg 0.93[a])	9.1 / 240	160	420	40	150
Energy/cycle [pJ/cycle]	2.49	2.1 / 0.23	15.8	110	13.6	1500
Area [mm^2]	0.057	0.18	0.026	0.015	0.02	0.0005
# of reported dies	5	1	5	1	1	1

a. Average over multiple samples
b. Calculated from Fig15.
c. Power consumption without a temperature sensor
d. 10 point calibration with a temperature sensor