5.2 Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications

Kyojin D. Choo, Li Xu, Yejoong Kim, Ji-Hwan Seol, Xiao Wu, Dennis Sylvester, David Blaauw

University of Michigan, Ann Arbor, MI

As IoT is increasingly integrated into our everyday life, the demand for different sensor modalities, especially imaging, is rising. IoT imagers are often compact and have small form-factor batteries and thus must be designed with both low power (improving battery life) and high image quality (maximizing utility). Previously reported sensors [1,2], along with this work, adopt motion-detection (MD) triggering of full-array capture where MD is performed on a heavily subsampled frame to enable continuous low-power operation. MD limits energy-hungry full-array captures to cases where activity is detected. To further reduce power consumption, the full-frame capture energy itself needs to be addressed, which is typically dominated by the ADC.

Conventional imagers use a single-slope ADC with 4T pixel structure [1], which provides high fidelity but is inherently energy inefficient. This is particularly the case at higher resolution due to its exponential energy scaling with bit-width or when used in conjunction with sub-sampling. SAR-based ADCs have superior energy efficiency and are used extensively in other application areas. However, to date SAR ADCs have been rarely used in imagers due to their large size and limited accuracy. To achieve both high quality and low power, we propose an energy-efficient, low-noise capacitor array-assisted charge-injection SAR ADC (c-ciSAR) structure. The structure merges an area-efficient charge-injection cell (ci-cell) [3] with a small capacitor array structure to extend its performance to 10b (Fig. 5.2.1). The merged c-ci structure achieves significantly higher ADC energy efficiency compared to a single-slope ADC, with a measured ADC FoM of 14.4μV·nJ (full capture mode) and 90.4μV·nJ (MD mode).

In addition, for MD, we propose an *n*-way side-step mapping of *n* motion pixel rows that re-uses the in-column hardware of the full-adder (FA) in the SAR logic (Fig. 5.2.1). This allows MD without transferring the motion pixel values to external storage for motion frame differencing. Unlike prior in-pixel analog MD [2], which degraded pixel performance by -25dB compared to typical 4T pixels, the MD approach maintains an un-modified conventional 4T pixel structure for high image quality. The complete image sensor is implemented in a 65nm CIS process with VGA active resolution and achieves 70.1μJ/full-array or 167.5pJ/frame/pixel, which is 2.4× lower than recent prior art [1], and consumes 1.7μJ/MD-frame (64.7× lower) in continuous MD mode.

The MD pixels are subsampled every n^{th} column and i^{th} row. For row *r*, an MD pixel at coordinate ($r \bullet i$, $c \bullet n$), where $c = \{0, 1, \ldots\}$, is re-routed sideways to column ($c \bullet n + r$) for data retention and in-column MD computation. As readout progresses vertically across subsampled MD rows, the mapped ADCs shift horizontally, and all MD pixels are mapped to column ADC. Both the storage of the MD pixel values and the differencing of values between MD frames reuse existing hardware of the c-ciSAR, thereby incurring minimal area overhead. The subsample stride *(n, i)* and resulting MD frame size *(h, v)* are configurable with the constraint that $h \bullet v < k$, where *k* is the total number of full active-array columns (640 for VGA). Skipped pixels can be enabled and binned together to minimize blind spots using three methods: floating diffusion (FD) binning on 2 shared Gr-Gb pixels, source-follower (SF) binning across horizontal/vertical direction, and digital binning in the column logic. For our evaluation case, $n = 20$ and $i = 24$, resulting in an MD frame resolution of 20×32 pixels.

The c-ciSAR ADC structure uses a c-ciDAC to create a local reference voltage, which is compared to the pixel voltage (Fig. 5.2.2). The comparator uses a StrongARM structure supplemented with an NMOS-input 5T-OTA placed as a pre-amplifier. Auto-zeroing (DC decoupling) capacitors are applied at both input branches of the pre-amplifier. Three capacitors (8×, 1×, 1×) on the DAC side provide coarse/fine pathways that transfer and sum charge-injection-based voltage changes at PDC (*pull-down coarse)*, PDF (*pull-down fine)* and PUF (*pull-up fine)* at *i_DAC*.

For each ci-cell (Fig. 5.2.2, right), the *Inject bar* signal pulses low to transfer constant charge from output (*Out*) and induces a repeatable change in its voltage. During each injection, the voltage on node *i_cap* rises from its reset value (*Gnd*) to the voltage controlled by node *Bias*, whose value sets the charge-injection amount. The cascode configuration of *M2* and the direction steering switches (*M1* and *M1d*) greatly improve the output impedance of the ci-cell, enabling 10b linearity. We pre-charge the output capacitor (C_{inj}) to a sufficiently high voltage (3.4V in our chip) during auto-zero phase to ensure that *M1* and *M2* operate in saturation mode throughout the ADC sequence. The dummy injection path makes the current draw from the power supply decision-independent, which ensures a constant injection charge even for high impedance power supply regulation. This enables low power overhead supply regulation, which is often needed in battery-operated devices.

Ci-cells are replicated 8 times per path to provide 3b of resolution and are re-activated multiple times to further refine resolution. Each set has a 7b calibration capacitor C_{cal}. There are only two types of ci-cells (up, down), reducing design complexity. Also, the coarse/fine capacitor array reduces the number of ci-cell activations by 4.3× for 10b ADC operation, enabling compact and energy-efficient DAC design.

Figure 5.2.3 shows the c-ciSAR ADC operation for one row. We perform dual-CDS, both in the analog domain. The first is performed during auto-zeroing. The second is performed by a non-binary search with fine ci-cells that match the DAC output (*i_DAC*) voltage to the *i_pixel* voltage. This is followed by coarse and fine searches to quantize the pixel signal value. Unlike a conventional capacitive DAC, the c-ciDAC does not require the fine CDS search code to be remembered and subtracted from the final signal code, simplifying ADC operation.

The signal value quantization first uses a coarse linear search (4b) instead of a binary search, which offers three advantages: 1) smaller and regular changes in DAC voltage allow for the use of a slow, low-power pre-amplifier; 2) the pull-up coarse (PUC) path can be omitted; and 3) noisy PDC operation is avoided at darker light levels where its higher DAC noise (due to its high gain) impacts image quality more significantly (Fig. 5.2.3). This is unlike a binary search, which involves noisy PDC/PUC operations regardless of light level. To further this improvement, the DAC value is shifted lower with PDF operation before entering the coarse linear search to avoid any PDC operations for the dark level.

Next, we perform a 7b fine binary search with a 1b redundant range where the DAC voltage is again offset to the center of the coarse search step to maximize overlap. Unlike a conventional capacitive SAR ADC, a non-binary search can be easily programmed since the sequence of operations is not restricted by the hardware configuration. Another advantage of this flexibility is the option to perform multiple sampling on the fine LSB to reduce noise. We implemented two types of multiple sampling (Fig. 5.2.3): 1) repeat the LSB decision cycle for MS1 times, and/or 2) fire the comparator decisions MS2 times within a cycle and perform majority voting. When the noise level is comparable to the LSB size, using the first approach is both effective and energy efficient.

Figure 5.2.4 shows the MD mode procedure and column logic, which has four unit operations: 1) arbitrary number addition/subtraction, 2) inversion, 3) absolute value, and 4) storage. Using these operations, we store the MD pixels in-column and detect those with significant changes in their code. The controller gathers and accumulates the MD flags (sign-bit of difference result) along with the frame values to determine whether to proceed to full capture and to adjust exposure value. The sensor is designed primarily with thick-oxide transistors to enable a low-power standby mode; column logic circuits use standard thin-oxide devices but are power gated.

Figure 5.2.5 shows captured images from full-array and MD operation, while Fig. 5.2.6 provides a comparison with other recent works with MD capability or SAR ADCs. The energy efficiency of the complete sensor is 37.9μV·nJ (ADC FoM). However, this number is dominated by the fully programmable controller (for flexible testing purposes); a simple hardwired state machine could be used in a more lightweight implementation. Excluding the controller energy consumption and evaluating only the readout energy (pixel, ADC and stream-out), E/frame/pix is 63.6pJ, and the ADC FoM is 14.4μV·nJ. The E/frame/pix in MD mode is 230.5× smaller than that of a single-slope sensor [1]. Also, the sensor can operate with its on-chip PMU, which generates internal voltages from a single external 2.5V battery, enabling integration into an IoT sensor. Figure 5.2.7 provides the chip photograph; the die area is 16.7mm^2.

References:

[1] O. Kumagai, et al., "A 1/4-inch 3.9Mpixel Low-Power Event-Driven Back-Illuminated Stacked CMOS Image Sensor," *ISSCC Dig. Tech. Papers*, pp. 86-87, Feb. 2018.

[2] G. Kim, et al., "A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation," *ISSCC Dig. Tech. Papers*, pp. 480-481, Feb. 2013.

[3] K. Choo, et al., "Area-Efficient 1GS/s 6b SAR ADC with Charge-Injection-Cell-Based DAC," *ISSCC Dig. Tech. Papers,* pp. 460-461, Feb. 2016.

[4] S. Ji, et al., "A 220pJ/Pixel/Frame CMOS Image Sensor with Partial Settling Readout Architecture," *IEEE Symp. VLSI Circuits*, pp. 226-227, June 2016.

 978-1-5386-8531-0/19/$31.00

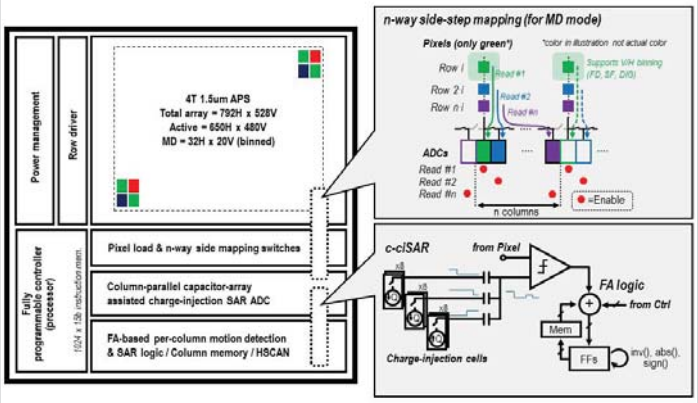


Figure 5.2.1: Overall sensor organization. n-way side-step mapping is used to enable low-power motion detection (MD) operation. Capacitor array-assisted charge-injection SAR ADC (c-ciSAR) is proposed to improve energy efficiency of the overall sensor.

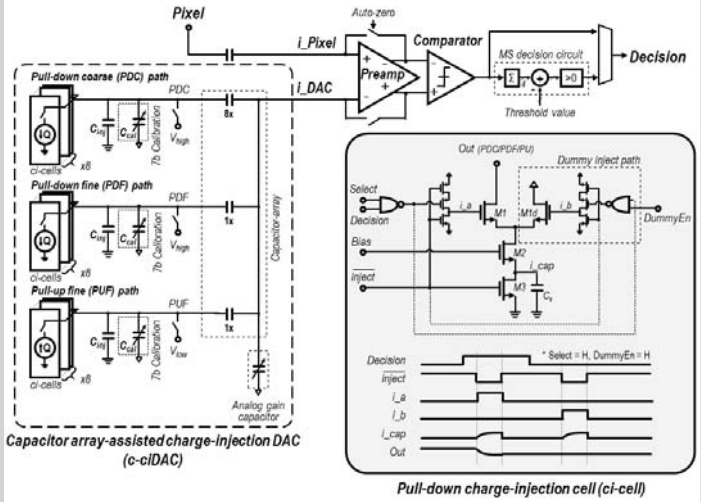


Figure 5.2.2: Detailed circuit diagram of capacitor array-assisted charge-injection SAR ADC (c-ciSAR). Capacitor array complements the charge-injection cell (ci-cell) to enable compact and energy efficient 10b operation.

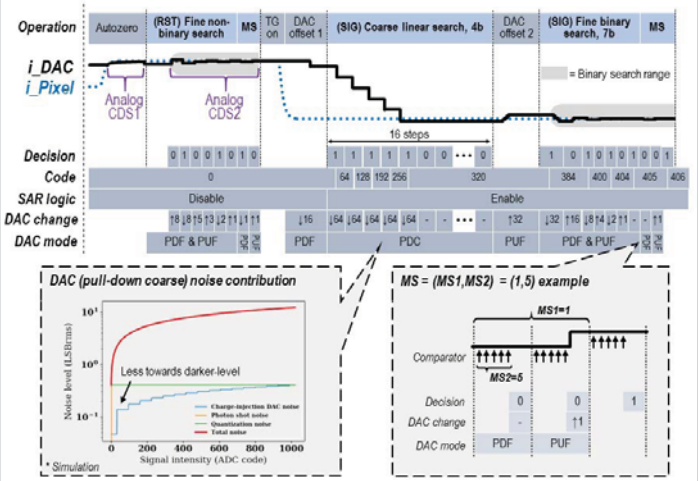


Figure 5.2.3: c-ciSAR row-conversion sequence. Programmability of c-ciSAR allows the ADC to perform not only binary search but also non-binary or linear search. Using appropriate search methods, the DAC noise contribution is minimized at dark level. Multiple-sampling mode is implemented.

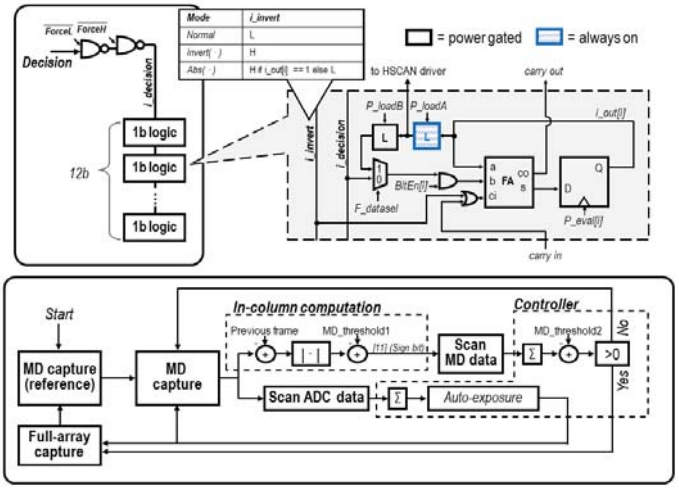


Figure 5.2.4: Circuits and algorithms for in-column motion evaluation. FA-based SAR logic is reused for in-column motion evaluation. Motion flags generated in-column are aggregated by the controller and used in auto-exposure adjustment and to trigger full-array capture.

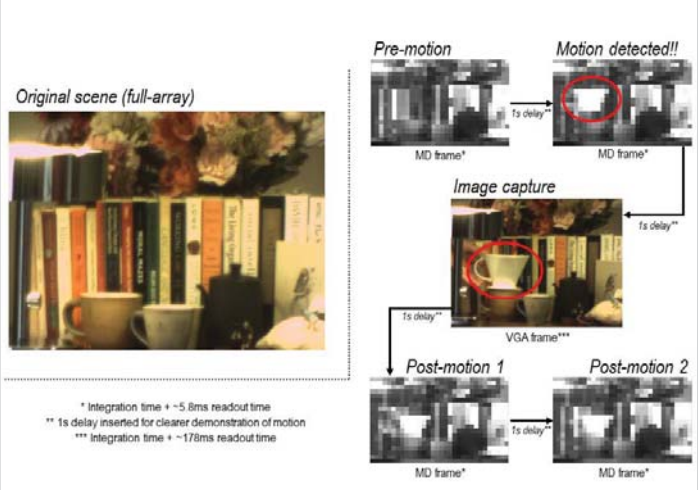
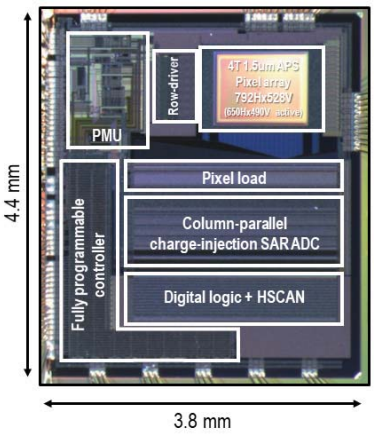


Figure 5.2.5: Captured images from full-array mode and motion detection (MD) mode. The sequence of images (right) shows the sensor in MD mode successfully triggering a full-array capture when motion (red circle) is detected.

		This work		Kumagai ISSCC 2018 [1]	Kim ISSCC 2013 [2]	Ji VLSI 2016 [4]
Technology		65 nm CIS		90 nm CIS + 40 nm	130 nm	180nm
Pixel structure		4T 1.5 um		4T 1.5 um	3T 6.4 um	3T
Full array resolution		792 x 528 = 418.1 K (Active=VGA)		2560 x 1536 = 3.93 M	128 x 128 = 16.3 K	320 x 240 = 76.8 K
MD mode support (& MD resolution)		O (32 x 20 = 640)		O (16 x 5 = 80)	O (48 x 16 = 778)	X
Readout circuit	ADC type	Capacitor-array assisted charge-injection SAR ADC		Single-slope ADC	Single-slope ADC	SAR ADC
	Resolution	10 b		10 b	8 b	10 b
	Full signal range	500 mV		435 mV	-	-
	ADC noise [uVrms]	Condition: no MS, AG*1=7.7 dB; MS=(4,1)*2, AG=7.7dB; MS=(1,5), AG=7.7 dB, I_{comp}↑; MS=(2,15), AG=7.7 dB, I_{comp}↑	Meas.: 226*3, 180, 136, 106	Q. adj*4: 211, 161, 108, 68	Cond.: AG=18 dB	Meas. / Q. adj: 100.4 / 98	450 (w/ pixel noise)
Full capture mode	Dynamic range	64.3 dB		67 dB	38.5 dB	-
	Max frame-rate	5.6 fps		60 fps	19 fps	130 fps
	@ dark condition, no MS, PMU off	Readout only (ADC + pixel)	Sensor (w/ controller)	Sensor	Sensor	Readout only (ADC + pixel)
	Energy / frame [uJ]	26.6	70.1	1583	1.5	16.9
	Energy / frame / pix [pJ]	63.6	167.5	400	610	220
	ADC FoM [uV·nJ]*5	14.4	37.9	40.1	-	99 (w/ pixel noise)
	ADC FoM2 [uV·pJ/DRU]*6	15.7	41.4	73.5	-	-
MD mode	Res. & max. frame-rate	10 b, 170 fps		8 b, 10 fps	3 levels, 30 fps	-
	Energy / frame [uJ]	0.26	1.7	110	0.036	-
	Energy / frame / pix [pJ]	400	2650	1375000	46.3	-
	ADC FoM [uV·nJ]*5	90.4	598.9 (x1)	138050 (x230.5)	-	-

*1 AG = Analog Gain
*2 Multiple-sampling (MS) notation : MS=(MS1, MS2)
*3 This number is used for the rest of the table
*4 Quantization noise adjust : sqrt(ADCnoise^2-2/12·LSB^2)
*5 ADC FoM : ADCnoise [uV] * (Energy / frame / total pix) [nJ]
*6 ADC FoM2 : ADC FoM [uV·nJ] *1000 / DRU

Figure 5.2.6: Comparison table.



Technology	TPSCo CIS 65nm 1P3M
Die Size	3800 um (H) x 4400 um (V)
Pixel pitch	1.5um
APS array	792H x 528V (Active : 650H x 490V > VGA)
# of ADC ch.	792
ADC pitch	3.1 um

Figure 5.2.7: Chip photograph.

978-1-5386-8531-0/19/$31.00