A 31 pW-to-113 nW Hybrid BJT and CMOS Voltage Reference with 3.6% ±3σ-inaccuracy from 0 ºC to 170 ºC for Low-Power High-Temperature IoT Systems

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Abstract

This paper proposes a low-power voltage reference generating 736 mV from 0 ºC to 170 ºC for low-power high-temperature IoT sensing systems. Using subthreshold current, a BJT diode develops a process-insensitive complementary-to-absolute-temperature voltage, and stacked CMOS transistors compensate the temperature sensitive by adding a proportional-to-absolute-temperature voltage. To maintain a reference voltage at high temperature, the circuit is designed considering *pwell*-to-*deep nwell* diode leakage. 76 samples from 3 different wafers, fabricated in a 180 nm process, show a ±3σ inaccuracy of 3.6% from 0 ºC to 170 ºC without any trimming. It consumes 31 pW at 27 ºC and 113 nW at 170 ºC from 0.9 V supply.

Introduction & Motivation

A millimeter-scale sensing system is an attractive solution for high-temperature applications such as downhole monitoring [1]. However, such systems need to tolerate temperature higher than 125 ºC while consuming low power due to limited battery size and thus capacity. For example, in standby mode, an advanced millimeter-scale system consumes 12 nW at room temperature and 190 nW at 125 ºC [2].

A voltage reference is an essential circuit for a system. For the high-temperature applications, the following specifications are desirable for the voltage reference: 1) operating temperature range higher than 125 ºC; 2) power consumption less than 10% of the total system power in standby mode; 3) no required trimming for cost reduction.

Voltage references using an SOI process have been proposed for high temperature applications, but they consume more than 2 µA [3]. Nano-watt bandgap references (BGR) have been proposed, but the maximum operating temperature is limited to less than 125 ºC [4]−[6]. Recently, a 76 pA CMOS voltage reference was proposed with operation up to 170 ºC using body diode leakage compensation [7]. However, it requires trimming to suppress a ±3σ inaccuracy from 10.3% to 3.4%.

This paper proposes a hybrid BJT and CMOS voltage reference satisfying the requirements for millimeter-scale high-temperature systems. 76 samples from 3 wafers, fabricated in 180 nm process, show a ±3σ inaccuracy of 3.6% from 0 ºC to 170 ºC without trimming. It consumes 31.4 pW at room temperature and 6.2 nW at 125 ºC (0.26% & 3.3% of the total system power budget of [2]).

Proposed Circuit

Fig. 1 conceptually explains how the proposed hybrid BJT & CMOS voltage reference creates a reference voltage (Vref). As a typical BGR, a complementary-to-absolute-temperature (CTAT) voltage is generated from a PN diode using a current source. To compensate its temperature sensitivity, a proportional-to-absolute-temperature (PTAT) voltage is created from a CMOS transistor using a subthreshold current, but its temperature coefficient (TC) is not large enough to cancel the TC of the CTAT voltage. Therefore, to boost the TC of the PTAT voltage, multiple number (N) of transistors are connected in series. By connecting the transistors on the top of the PN diode, the two different types of devices compensate their TC and obtain the output voltage (Vref) with a low TC. Also, this method saves power consumption by using a subthreshold current and also sharing the same current for both PTAT and CTAT voltage generation.

Fig. 2 shows the proposed voltage reference details. It generates a supply-independent supply current using two native NMOS thick-oxide transistors (M1 & M2) and a standard NMOS transistor (M3) [7],[8]. M3 with 0 V Vgs operates in subthreshold region [5],[6],[9]. M1 and M2 assigns 160 mV – 280 mV to Vds of M3 (simulated), and it helps the current avoid GIDL/DIBL effect. Also, their thick-oxide gate allows Vdd up to 3.3 V. The supply current can be expressed as follows:

$$I = \mu C_{ox} \frac{W_{M3}}{L_{M3}} (m-1) V_T^2 exp\left(-\frac{Vth}{mV_T}\right). \quad (1)$$

μ is mobility, C_{ox} is oxide capacitance, W_{M3} and L_{M3} are the size of M3, m is subthreshold slope factor, Vth is threshold voltage of M3, and V_T is the thermal voltage.

The current sets Vbe of the PN diode (D1) with a negative TC (-1.24 mV/ºC, simulated). To cancel the temperature sensitivity, three diode-connected NMOS transistors (M4, M5, and M6) are stacked in series on the top of D1. The three transistors provide a PTAT voltage, compensating the TC at the output (Vref). Vref can be expressed as follows:

$$\text{Vref} = \frac{Eg}{q} - \frac{Vth}{m} + \ln\left\{\frac{\mu C_{ox}(m-1)k}{qT^{2+m}} \cdot \frac{W_{M3}}{L_{M3}}\right\} + \frac{NmkT}{q} \cdot \ln\left(\frac{W_{M3}}{W_{PTAT}}\right). \quad (2)$$

Eg/q is the bandgap voltage, N is the number of NMOS transistors connected in series for a PTAT voltage, and W_{PTAT} is their width. In [7] and [8], the output voltage is a function of $N \times Vth$ and sensitive to process variation. In the proposed approach, however, Vref is a function of attenuated Vth and process-insensitive Eg/q, suppressing sensitivity to process variation. Threshold voltages of M4 − M6 are cancelled by using M3 with 0 V Vgs [5],[6],[9].

To avoid the body effect of NMOS transistors, the body is tied to their source using deep-nwell, and the nwell is connected to Vdd. A deep nwell-to-psub leakage (ileak1) increases power consumption but does not disturb Vref. However, a deep nwell-to-pwell leakage (ileak2) increases current at lower devices. In [8], nwell leakage degrades TC, and it cannot maintain a low TC at high temperature only with transistor sizing. However, the proposed approach weakens the impact of the leakage current since it does not requires perfectly matched Vds of M4 − M6. Instead, it only needs the total PTAT voltage to null the TC of the CTAT Vbe. Thus, without a complicated leakage compensation technique used in [7], a low TC can be achieved by proper transistor sizing, considering ileak2.

Measurement Results

The proposed voltage reference was fabricated in a 180 nm process (Fig. 9). Figs. 3 – 5 show the measured V_{REF} and TC distribution from 76 samples from 3 different wafers. Without trimming, the voltage references achieve a ±3σ inaccuracy of 3.6% from 0 ºC to 170 ºC. The average TC is 27 ppm/ºC. Fig. 6 shows power consumption across temperatures and supply voltages. It only consumes 31.4 pW at 27 ºC and 0.9 V. The increased power consumption at high temperature is acceptable in typical systems since their total system power is also increased and the portion of the proposed circuit will be kept small (e.g., only 3.3% at 125 ºC at the advanced low-power system [2]). Fig. 7 displays V_{REF} across supply voltages at room temperature. Line sensitivity is 0.27 %/V from 0.9 V to 3.3 V. Fig. 8 shows a measured oscilloscope waveform at startup. Vref is settled to the final value without any stability issue. Table I shows performance summary and comparison with state-of-the-art low-power (pW or nW) voltage references. The proposed voltage reference and [7] cover the highest temperature (170 ºC) and also the widest temperature range. Compared with [7], this work shows 2.9× less ±3σ inaccuracy without trimming, 2.4× lower TC on average, 4.4× smaller power consumption, and 0.9 V lower minimum supply voltage.

References

[1] Z. Shi, *et al*., *SPE Digital Energy Conference and Exhibition*, 2015.
[2] Q. Dong, *et al*., *ISSCC* 2017. [3] M. Assaad, *et al*., *HiTEN* 2011.
[4] Y. P. Chen, *et al*., *VLSI* 2012. [5] J. M. Lee, *et al*., *ISSCC* 2015.
[6] Y. Ji, *et al*., *ISSCC* 2017. [7] I. Lee, *et al*., *ASSC* 2017.
[8] I. Lee, *et al*., *JSSC* 2017. [9] S. Jeong, *et al*., *CICC* 2013.
[10] Q. Dong, *et al*., *VLSI* 2016.

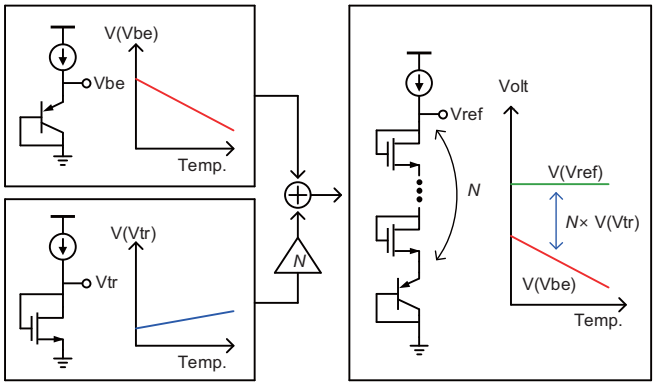

Figure 1. Basic operation concept of proposed voltage reference..

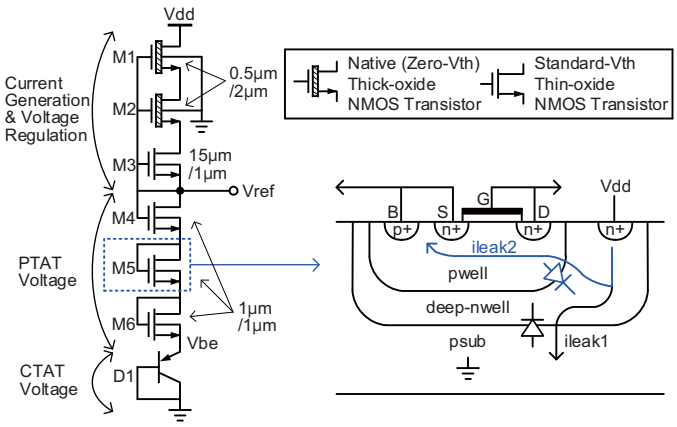

Figure 2. Proposed voltage reference.

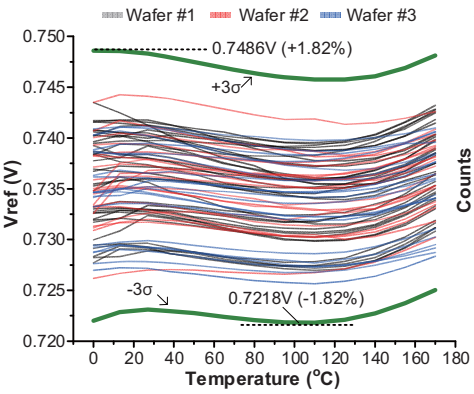

Figure 3. Measured V_{REF} across temperatures from 3 different wafers.

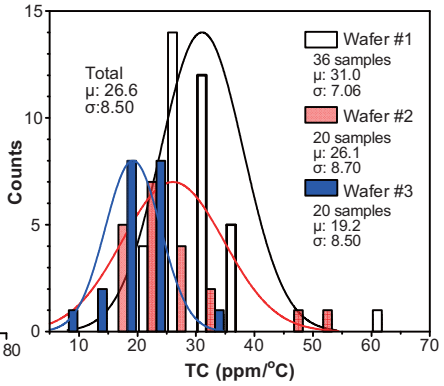

Figure 4. Measured distribution of TC from 3 different wafers.

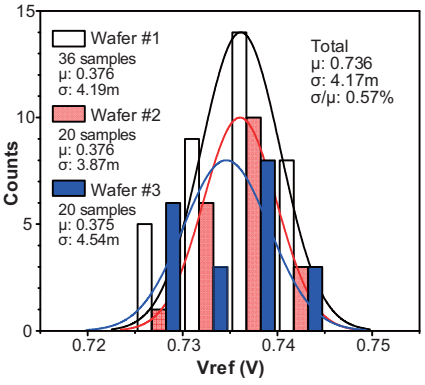

Figure 5. Measured distribution of V_{REF} from 3 different wafers.

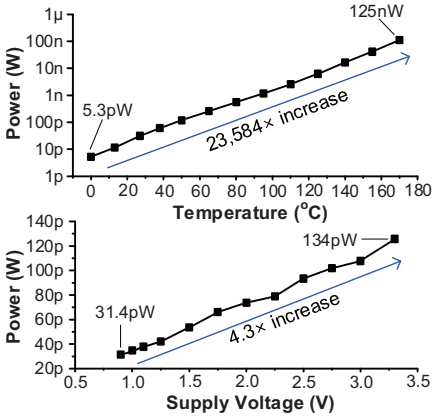

Figure 6. Measured power consumption
(a) Across temperatures
(b) Across supply voltages.

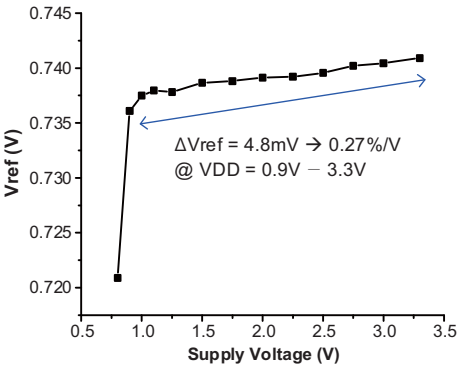

Figure 7. Measured supply sensitivity.

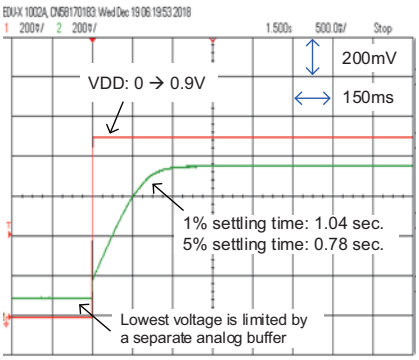

Figure 8. Measured waveform at startup.

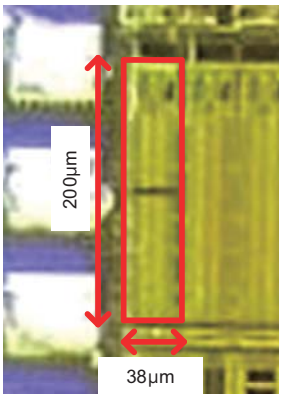

Figure 9. Chip Photo.

	This Work	[7] ASSCC'17	[8] JSSC'17	[10] VLSI'16	[4] VLSI'12	[5] ISSCC'15	[6] ISSCC'17
Technology (nm)	180	180	180	180	180	350	180
Vref Generation Method	BJT + CMOS	CMOS	CMOS	CMOS	BJT	BJT	BJT
Vref (V)	0.74	1.17	1.25	0.98	1.19	1.18	1.24
Temperature Range (°C)	0 ~ 170	0 ~ 170	0 ~ 100	-40 ~ 85	-20 ~ 100	-10 ~ 110	0 ~ 110
Supply Voltage (V)	0.9 ~3.3	1.8 ~ 3.6	1.4 ~ 3.6	1.2 ~ 2.2	1.8 ~ 3.6	1.2 ~ 2.2	1.3 ~ 1.8
±3σ Inaccuracy @ Entire Temp. Range (%) (w/o trimming)	3.6	10.3	4.9	1.9	N/A	N/A	N/A
TC (ppm/°C)	10 ~64 µ:27	32 ~106 µ:64	11 ~73 µ:31	48 ~124	µ:25	13	26
Power @ Room Temp. (W)	31.4p	137p	33.6p	114p	3.6n	34.8n	9.3n
Line Sensitivity (%/V)	0.27	0.09	0.31	0.38	2.03	0.20	0.08
# Measured Samples	76 (3 wafers)	40	60 (3 wafers)	60 (3 wafers)	10	10	10
Active Area (mm^2)	0.0076	0.0081	0.0025	0.0049	0.098	0.48	0.055

Table I. Performance summary and comparison with other state-of-the-art low-power voltage references.