A 4×4×4-mm^3 Fully Integrated Sensor-to-Sensor Radio using Carrier Frequency Interlocking IF Receiver with -94 dBm Sensitivity

Li-Xuan Chuo[#1], Yejoong Kim[#], Nikolaos Chiotellis[#], Makoto Yasuda[$], Satoru Miyoshi[*], Masaru Kawaminami[$*], Anthony Grbic[#], David Wentzloff[#], Hun-Seok Kim[#], David Blaauw[#]
[#]University of Michigan, Ann Arbor, USA
[$]Mie Fujitsu Semiconductor Limited, Yokohama, Japan
[*]Fujitsu Electronics America, Inc., Sunnyvale, USA
[1]lxchuo@umich.edu

***Abstract*— Ultra-low power mm-scale IoT platforms enable newly emerging applications such as pervasive agricultural monitoring and bio-sensing. Although there is an increasing interest in sensor-to-sensor communication, as defined in Bluetooth v5.0, prior research in mm-scale wireless systems is mostly limited to asymmetric sensor-to-gateway communication. This paper introduces a 4×4×4 mm^3 fully integrated radio system that integrates a transceiver chip, antenna, power management unit and baseband processor for sensor-to-sensor mesh networks. The proposed system uses a low power 32 kHz reference frequency and a carrier frequency interlocking IF receiver. It achieves -94 dBm sensitivity with 97 µW power consumption and -12.6 dBm EIRP for sensor-to-sensor mesh network communication.**

***Keywords*— radio transceivers, low-power electronics, dipole antennas, wireless sensor networks, wireless mesh networks.**

I. Introduction

Newly emerging Internet of Things (IoT) applications, such as agricultural monitoring, smart cities and ubiquitous beacon services, require ultra-low power (ULP) platforms of cm- and even mm-scales. Although there is increasing interest in sensor-to-sensor mesh networks, such as the new Bluetooth v5.0 standard, prior work in mm-scale ULP wireless communication systems mostly utilize a sensor-to-gateway topology (star-network) [1]. Millimeter-scale dimensioned systems exacerbate the challenges in sensor-to-sensor transceiver design, including: 1) accurate timing and carrier frequency synchronization among ULP transceiver nodes; 2) extremely stringent link budget stemming from the poor, electrically-small, antenna efficiency; and 3) inadequate battery capacity (~10 uAh) and instantaneous battery current capacity (~100 uA) due to mm-scale battery size and constrained by VDD fluctuation.

This work proposes a mm-scale fully self-contained radio system that supports sensor-to-sensor communication, enabling mesh network formation for mm-scale devices. Conventional transceivers use a tens of MHz crystal oscillator (XO) as the frequency reference. However, their long start-up time (~1 ms) and the high power consumption of their crystal oscillator (~100 µW) and PLL (~1 mW) [2] make it incompatible with mm-size batteries. Instead, our proposed design uses only a 32.768-kHz real-time clock (RTC) with <10nW power consumption to frequency lock a power oscillator merged with a high-Q 3D loop antenna, which doubles as a DCO and operates in open loop after locking. Hence, the proposed design combines the conventional PA and PLL and eliminates the power-hungry high frequency crystal and DCO, enabling a highly energy efficient TX design and reducing off-chip components. The locked power oscillator is then reused at the start of each RX operation to generate a calibration tone. To this tone a free-running ring oscillator (RO) is tuned such that the center of the down-converted RF signal aligns to the passband of the IF amplifier. This achieves TX-RX carrier frequency synchronization, which is critical in narrowband communication. It also eliminates the need for explicit estimation of the bandpass IF amplifier center frequency, which significantly lowers the RX power consumption and simplifies the design. Combined with the reuse of TX power oscillator as a Q-enhanced amplifier (QEA) [3, 4], we achieve good sensitivity of -94 dBm at the input of the -7.8 dBi (estimated from simulation) mm-scale antenna with 97 µW power consumption. TX consumes 3.5 mW peak power for 125µs pulse duration drawn from decaps and achieves -12.6 dBm EIRP. The complete system, including the proposed transceiver chip, high-Q antenna, 32 kHz crystal, Cortex-M0 processor and power management unit, is integrated within a 4×4×4 mm^3 sensor platform and communicates at a data rate of 4 kbps.

II. Carrier Frequency Interlocking IF Receiver

Fig. 1 shows our proposed radio architecture. Unlike conventional low-power receiver approaches such as direct conversion, low-IF, and uncertain-IF [5], the proposed architecture takes advantage of a high-Q antenna and TRX front-end sharing. A direct-conversion scheme is popular for its simplicity but suffers from flicker noise, DC offset, and LO leakage, making it hard to achieve good sensitivity. A low-IF architecture has been widely used to address these issues, but it requires a high quality RF local oscillator (LO), which is very power hungry. Recently, uncertain-IF architectures using a low-power unlocked LO were proposed where uncertain-IF is accommodated by increasing the IF amplifier bandwidth. However, widening the IF amplifier bandwidth to address IF uncertainty increases power and reduces SNR (by incorporating more noise), nullifying the benefit of narrowband communications to achieve superior sensitivity.

The proposed architecture instead uses a narrow band RX chain that combines the band-selective (Q~1000, bandwidth ~2 MHz) QEA and a bandpass IF amplifier to obtain superior SNR than typical uncertain IF architectures while maintaining low power consumption. First the digitally-controlled power

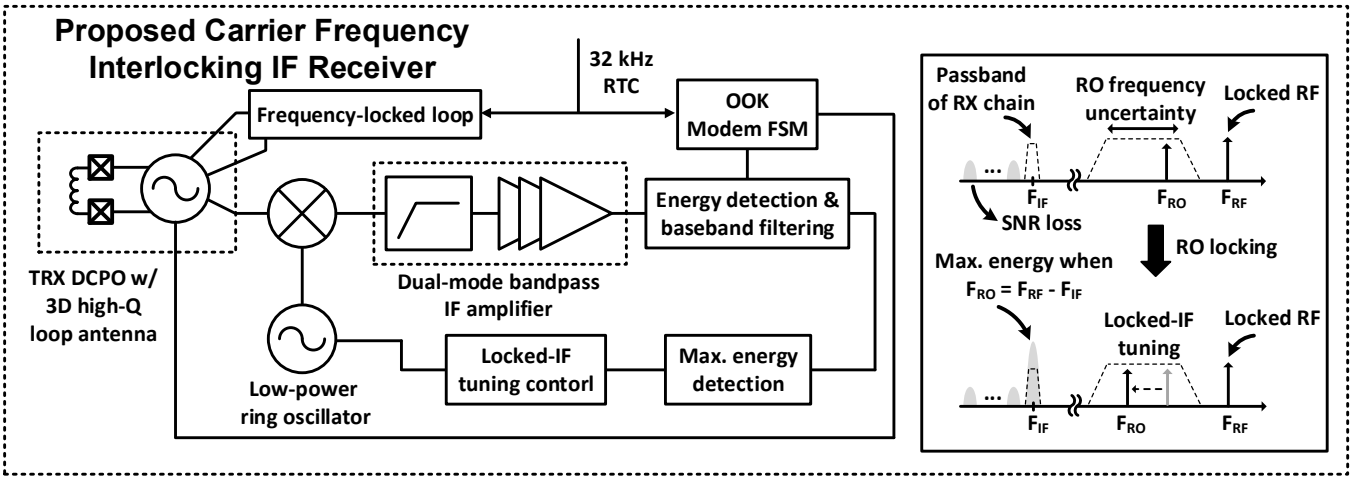

Fig. 1. The proposed carrier frequency interlocking IF radio architecture and frequency domain explanation

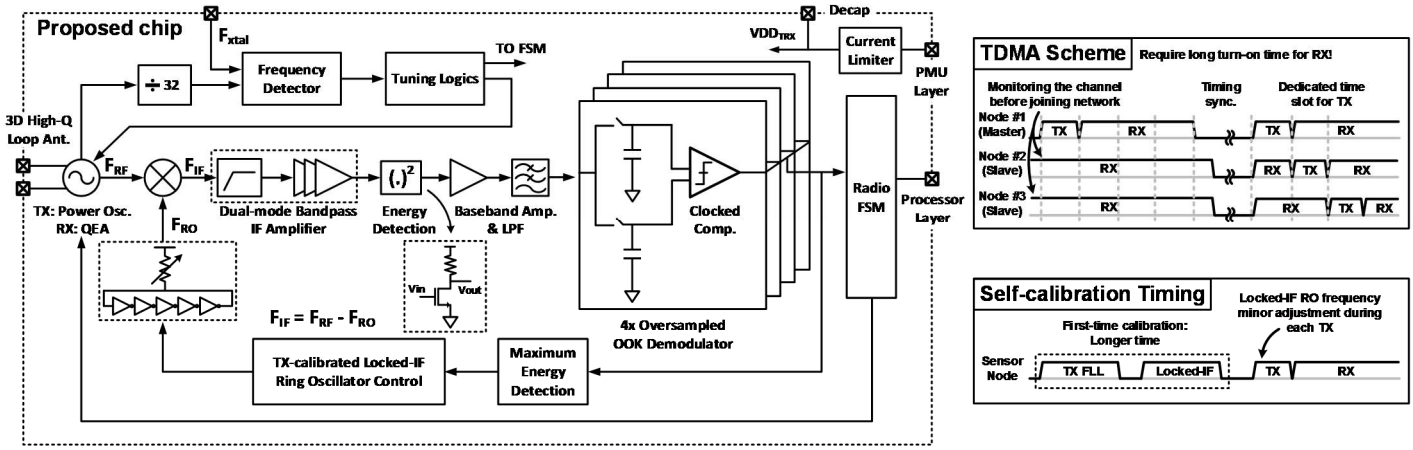

Fig. 2. Details of the transceiver circuits with calibration loop timing and the radio sensor node multiple access scheme

oscillator (DCPO) is frequency-locked using the 32 kHz crystal for TX. The DCPO also serves as the RX front-end by implementing the QEA and provides the RF reference tone for calibration to align the down-converted IF signal to the passband of the IF amplifier in the receive chain. During this calibration, the frequency-locked DCPO signal (F_{RF}) is down-converted to IF (F_{IF}) by the RO frequency (F_{RO}) and passed through dual-mode bandpass IF amplifiers. A maximum energy detection loop then sets F_{RO} such that the bandpass IF amplifier output is maximized which ensures that the RO is tuned and F_{IF} is centered in the IF-amplifier's passband for maximum sensitivity. As a result, the IF amplifier bandwidth can be reduced. The proposed architecture preserves the high sensitivity while using a low-power RO as LO (Fig. 1).

III. Transceiver Circuits Implementation

A. Transceiver Overview and System Timing

The DCPO uses a co-designed high-Q 3D loop antenna as the resonant component, which lowers the power consumption in TX mode and also serves as a highly band-selective filter in RX mode (Fig. 2). The TX and RX front-ends share the same circuits with different bias conditions, resulting in naturally similar carrier frequency. Though there is still frequency difference results from non-linearity of capacitors, it was found to be small compared to the RX QEA bandwidth (2 MHz). The TX DCPO frequency calibration is performed first, followed by the RX interlocking IF tuning. Depending on the initial control setting, the TX DCPO frequency-locked loop (FLL) may require a long settling time at first due to the use of 32 kHz reference. However, once the initial calibrated frequency control word is stored in the processor, the radio will only need to fine-tune and update the setting each time before communicating. The self-calibration timing is shown in Fig.2.

B. DCPO Front-End Design and Operation

During TX DCPO frequency locking, the DCPO cross-coupled transistors are biased with high current (~850 μA) to start the oscillation. The FLL is composed of a 32x divider, asynchronous counter, and frequency tuning logic (Fig.3). The counter is clocked by a divided RTC (32.768/4 = 8.192 kHz) supplied by the processor for high frequency resolution. It counts the number of divided RF signal transitions (~75 MHz) and locks the frequency accordingly. Since the carrier frequency is set by the 3D loop antenna and the (mostly) off-chip capacitance, it does not have significant VDD dependency.

Thus, the FLL is mainly for compensating the antenna and off-chip capacitor variations. In RX mode, the same cross-coupled pair is biased in the Q-enhanced region for boosting the Q value of the loop antenna to have a band-selective filter response and in-band voltage gain (62.7 dB, simulation). The targeted RF front-end filter bandwidth of the receiver chain is 2 MHz (Q ~ 1000), meaning that the TX frequency synchronization should also be within 0.1% (Q ~ 1000). The measured results shown in Fig.3 indicates that the FLL calibration can synchronize the carrier frequency to within 0.1% across 5 tested chips.

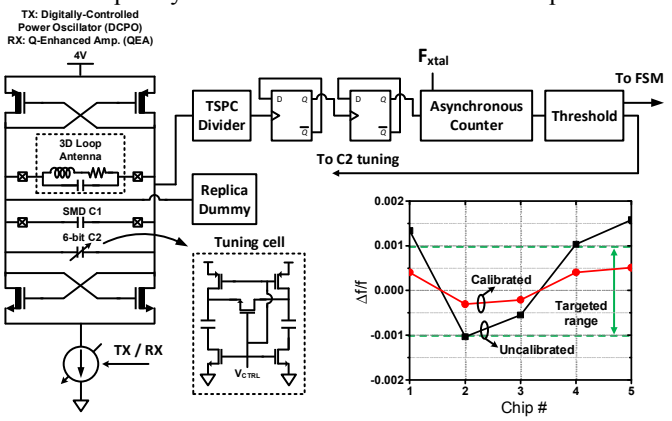

Fig. 3. Transmitter frequency-locked loop using 32-kHz RTC and the measured results, showing it can lock the frequency within 0.1% error from chip-to-chip

C. Carrier Frequency Interlocking IF Receiver Designs

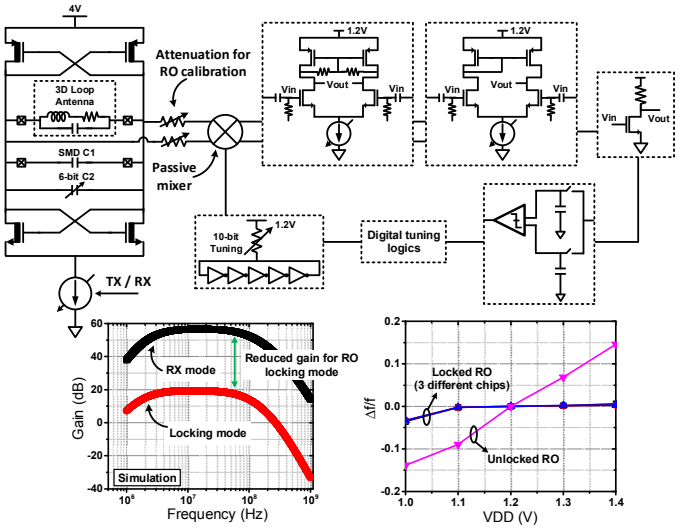

Fig. 4. Reuse the RX chain with lower gain setting for RO tuning loop and the measured RO frequency with different supply voltage

After the carrier frequency is locked, the radio starts IF calibration. The RX chain is turned on during the TX operation with the self-injected attenuated TX signal as shown in Fig.4. Because the input RF signal is strong (directly from the DCPO), the IF amplifiers were designed to have a calibration mode with 40dB less gain (Fig. 4, left, bot). This lowers power consumption during calibration and avoids saturation of the amplifier. The simulated results in Fig. 4 show that both high and low gain modes have identical bandpass frequency response but different gains. We reuse the remainder of the RX chain (energy detector and comparator) to detect the output signal from the IF amplifiers and tune the RO frequency. The energy detector output is sampled with different RO frequency settings and compared to the prior output by reusing the data-demodulation comparator. This search continues until it finds the maximum output level at which point the amplifier passband is aligned with the RX IF signal down-converted from the DCPO TX signal. In the mm-scale sensor node design, the VDD will fluctuate due to the limited battery and decap current and capacity. As a result, it is difficult to achieve a stable low-power RO frequency with a conventional design. Fig.4 shows the measured RO across VDD variation with and without the proposed TX-RX interlocking technique. The free-running RO frequency will deviate by more than 20% (100's MHz in GHz) when VDD varies from 1.4 V to 1.0 V. With the proposed locking calibration, the RO frequency is stable within 1% across VDD, meeting the bandwidth of the IF amplifier.

When both DCPO and RO are tuned, data communication is performed using binary pulse position modulation (PPM) that compares symbol power levels at two different position, eliminating the need of an accurate reference voltage. The proposed chip supports time-division multiple access (TDMA) scheme as shown in Fig.2. Each node is given a programmable time slot (ID) for collision-free transmission.

IV. Chip Measurement and Radio System Evaluation

The transceiver chip was fabricated in MIFS 55-nm DDC CMOS and integrated with a custom designed antenna in $4 \times 4 \times 4$ mm^3 form factor. Since this transceiver was co-designed with the antenna and was not matched to 50 ohm, its performance evaluation includes the antenna gain (-7.8 dBi). The measurement results are shown in Fig. 5.

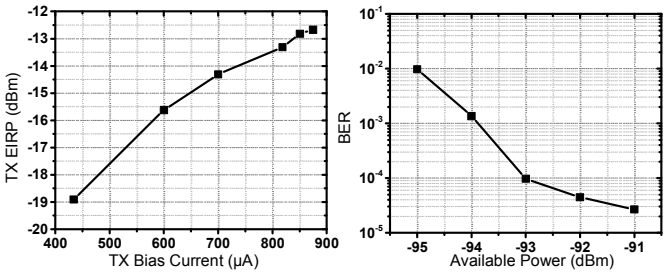

Fig. 5. Measured transceiver chip (w/ antenna) EIRP and sensitivity

In TX mode, the EIRP of the sensor node transmitting a continuous tone was measured using a horn antenna (LB-530-NF) in an anechoic chamber which ranged from -18.9 to -12.6 dBm with 1.7 to 3.5 mW TX power consumption. Due to the co-design of antenna, the radio will have emission during the calibration. However, the output power is low since the antenna has low gain and the signal does not contain the correct header for communication. The receiver has a sensitivity of -94 dBm measured at the input of a -7.8 dBi (simulation) antenna for 10^{-3} BER at 4 kbps. A measured time-domain waveform of wireless communication between two integrated nodes in Fig.6 validates TDMA based sensor-to-sensor communication. For measurement in Fig. 6, the number of TDMA slots are pre-

Table 1 Performance summary and comparison to other works

		This work	ISSCC 2017 [3]	ISSCC 2015 [5]	ISSCC 2015 [6]
Technology		55 nm	180 nm	65 nm	65nm
System Form Factor		4x4x4 mm^3	3x3x3 mm^3	4.6x4.6 mm^2 Receiver chip only	1.3x0.9 mm^2 Receiver chip only
# of off-chip components		5 (Antenna, xtal, decaps)	4 (Antenna, decaps)	11 (Inductors, decaps)	3 (Inductors)
Frequency		2.4 GHz	900 MHz	2.4 GHz	2.4 GHz
Sensor-to-Sensor Communication?		Yes	No	No	No
RX	Technique	Carrier Frequency Interlocking IF	Tuned-RF	Dual Uncertain-IF	RX-based FLL
	Modulation	Binary PPM	Binary PPM	OOK	OOK
	Power Consumption	97 µW	1850 µW	99 µW	227 µW
	Data Rate	4 kbps	7.8 kbps – 62.5 kbps	10 kbps	1 Mbps
	Sensitivity*	-94 dBm (@ input of -7.8 dBi antenna)	-93 dBm (@ input of -23.4 dBi antenna)	-97 dBm (@ input of AFE)	-83 dBm (@ input of AFE)
TX	Technique	RTC-FLL	Free-running	N/A (RX only)	N/A (RX only)
	Max. EIRP	-12.6 dBm	-26.9 dBm		
	Power Consumption	3.5 mW @ 4V	2 mW @ 4V		
	Data Rate	4 kbps	30 bps – 30.3 kbps		

programmed to six. Node #1 (ID=3) transmits at the third time-slot and listens at all other time-slots. The same rule applies to node #2 (ID=6) that uses the sixth time-slot for TX. The zoomed-in plot in Fig. 6 shows that the two mm-scale nodes synchronously transmit and receive using proper time slot, thus establishing successful communication links. Fig. 7 shows the fully integrated system that integrates a transceiver chip, antenna, power management unit, and baseband processor for wireless node-to-node communication measurements. Table 1 summarizes the overall performance and compares it to other low-power radio systems.

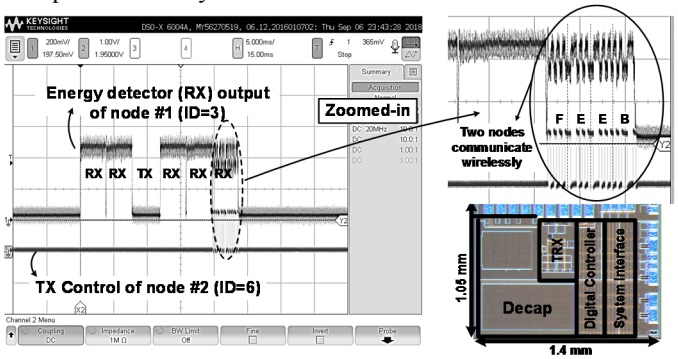

Fig. 6. Measured time domain sensor-to-sensor communication waveform using the fully integrated radio system and the transceiver chip micrograph

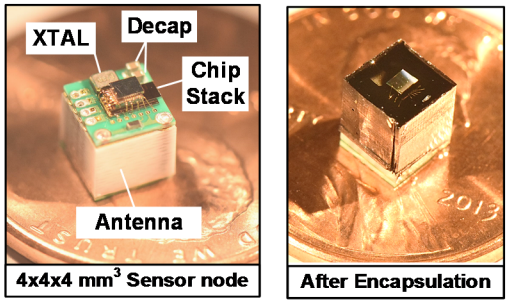

Fig. 7. The fully integrated radio system including transceiver, processor, PMU, antenna, XTAL, and decaps

V. Conclusion

Challenges in mm-scale node-to-node communication includes electrically small antenna (low radiation efficiency, difficult to impedance match), frequency / timing synchronization and stringent power / energy budget (limited peak current and battery capacity). In this paper, we present a 4x4x4 mm^3 fully stand-alone radio system that integrates an RF transceiver chip, antenna, power management unit and baseband processor with a new carrier frequency interlocking IF receiver architecture for low-power and high sensitivity node-to-node mesh networks. The proposed mm-scale system demonstrates sensor-to-sensor communication with -12.6 dBm EIRP for TX and -94 dBm sensitivity (at the input of a -7.8 dBi antenna) with 97 µW power consumption for RX.

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