Wang, Zhehong

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Education

Sep. 2016 – Present **University of Michigan, Ann Arbor**
Ph.D. Student (Electrical & Computer Engineering: VLSI)
Advisor: Professor David Blaauw

Sep. 2016 – Apr. 2019 **University of Michigan, Ann Arbor**
M.S. (Electrical & Computer Engineering: VLSI) CGPA 3.932/4

Sep. 2012 - Jun. 2016 **Zhejiang University, Hangzhou, China**
B.E. (Electronics & Information Engineering) CGPA 3.95/4 Ranking: 2/95

RESEARCH EXPERIENCE

Sep. 2016 - Present **Graduate Student Research Assistant, University of Michigan, Ann Arbor**

- Current Projects
  - Hardware Accelerator for Fully Homomorphic Encryption
- eRRAM Based DNN Accelerator
- DNA Sequencing Seeding Accelerator
- Low-power MRAM for Sensor-node Application

Publication

- *__Z. Wang__, *Z. Li, Q. Dong, C. Su, W. Chu, G. Tsou, Y. Chih, T. Chang, D. Sylvester, H. Kim, D. Blaauw, “An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM”, Symposium on VLSI Circuits (VLSI), June 2020
- X. Wu, A. Subramaniyan, **Z. Wang**, S Narayanasamy, R Das, D. Blaauw, “17.3 GCUPS Pruning-based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing”, Symposium on VLSI Circuits (VLSI), June 2020
- **Z. Wang**, T. Zhang, D. Fujiki, A. Subramaniyan, X. Wu, M. Yasuda, S. Miyoshi, M. Kawaminami, R. Das, S. Narayanasamy, D. Blaauw, “A 2.46M reads/s Genome Sequencing Accelerator using a 625 Processing-Element Array”, Custom Integrated Circuits Conference (CICC), March 2020
- T. Ajayi, V. A. Chhabria, M. Fogaça, S. Hashemi, A. Hosny, A. B. Kahng, M. Kim, J. Lee, U. Mallappa, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L Wang, **Z. Wang**, M. Woo, B. Xu, “Toward an open-source digital flow: First learnings from the openroad project”, Design Automation Conference (DAC), June 2019
- Q. Dong, **Z. Wang**, J. Lim, Y. Zhang, M. E Sinangil, Y. Shih, Y. Chih, J. Chang, D. Blaauw, D. Sylvester, “A 1-Mb 28-nm 1T1MTJ STT-MRAM With Single-Cap Offset-Cancelled Sense Amplifier and In Situ Self-Write-Termination”, IEEE Journal of Solid-State Circuits, 54, No. 1, January 2019, pg. 231-239
- S.Jeloka, **Z. Wang**, R. Xie, S. Khanna, S. Bartling, D. Sylvester, D. Blaauw, “Energy Efficient Adiabatic FRAM with 0.99 PJ/Bit Write for IoT Applications”, Symposium on VLSI Circuits (VLSI), June 2018
- K. Yang, Q. Dong, **Z. Wang**, Y. Shih, Y. Chih, J. Chang, D. Blaauw, D. Sylvester, “A 28nm Integrated True Random Number Generator Harvesting Entropy from MRAM”, Symposium on VLSI Circuits (VLSI), June 2018
- Q. Dong, **Z. Wang**, J. Lim, Y. Zhang, Y. Shih, Y. Chih, J. Chang, D. Blaauw, D. Sylvester, “A 1Mb 28nm STT-MRAM with 2.8 ns read access time at 1.2 V VDD using single-cap offset-cancelled sense amplifier and in-situ self-write-termination”, International Solid-State Circuits Conference(ISSCC), February 2018

RELEVANT COURSE PROJECTS

2018	Two-way Superscaler OoO Processor Based on R10K scheme (UoM, Ann Arbor)
2017	Dynamic Zoom ADC for Audio Application (UoM, Ann Arbor)
2016	Standard 6T SRAM for Machine-Learning Classifier (UoM, Ann Arbor)
2016	Chopper Amplifier for Biomedical Sensing (UoM, Ann Arbor)

HONORS AND AWARDS

2017	1st team project prize in Integrated Analog/Digital Interface Circuits (EECS511, UoM)
2015	Wang Guosong Scholarship, Zhejiang University
2015	1st prize in Undergraduate Electronic Design Contest of Zhejiang University
2014	Texas Instrument Student Grant, Zhejiang University
2013 & 2014	First-class Scholarship for Outstanding Students, Zhejiang University
2013 & 2014	Excellent Student Awards, Zhejiang University
2013 & 2014	National Scholarship, Zhejiang University
2013 & 2014	First-class Scholarship for Outstanding Merits, Zhejiang University

TECHNICAL SKILLS

- Graduate Courses
  - VLSI Design I
  - Monolithic Amplifier Circuits
  - Integrated Analog/Digital Interface Circuits
  - Analog Integrated Circuits
  - Machine Learning
  - Computer Architecture
  - Probability and Random Process
  - Computer Vision
  - Intro to Operating System
- CAD Tools and Programming Languages
  - Simulation Tools: HSpice, Spectre, VCS, Matlab
  - Physical Design Tools: Virtuoso, Calibre, Design Complier, Innovus, Voltus
  - HDLs: Verilog/SystemVerilog
  - Programming Languages: C/C++, Python, Perl