3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection

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In ultra-low-power crystal oscillators (XOs), the ideal circuit consumes minimum power while disturbing the oscillation as little as possible. In order to achieve sub-nW power consumption, there are three fundamental considerations: the loss in the crystal, the efficiency of energy injection, and the power required to extract oscillation frequency and phase as well as drive the injection. Crystal loss is a quadratic function of oscillation amplitude (V_{OSC}) in series resonance, and it is a quadratic function of both V_{OSC} and load capacitance (C_L) in parallel resonance. Recent nW XOs use an amplitude control circuit [1] or lower voltage supply [2-5] to reduce V_{OSC}, while [5] has no explicit capacitance on the crystal nodes to reduce C_L. These techniques greatly reduce the crystal loss such that it no longer dominates total power [1]. However, lower oscillation amplitude makes the oscillation more prone to noise injected by the driving circuit (Fig. 3.3.1). As a result, nW XOs typically exhibit sacrificed Allan deviation floor, which indicates degraded long-term frequency stability.

In this work, we propose an XO design with frequency-divided (4kHz), high energy-to-noise-ratio pulse-injection oscillation (HERO). The performance of the XO is compared with state-of-the-art XOs in Fig. 3.3.6. By allowing the crystal to run freely for a longer time between injections, HERO achieves a 2ppb Allan deviation floor, which is 5× lower than the deviation floors among the state-of-the-art nW XOs. Furthermore, the less-frequent injections significantly reduce the injection overhead, enabling lowest-reported power consumption (0.51nW) among prior-art oscillators shown in Fig. 3.3.6. An integrated phase extraction and delay circuit obtains accurate injection alignment, resulting in stable operation from –25ºC to 125°C, the widest reported range among the nW XOs shown in the comparison table.

A continuously driven conventional Pierce XO and series-mode XO [1] continuously inject circuit noise, requiring high amplitude oscillation to achieve high frequency stability (Fig. 3.3.1). Pulsed energy injection at peaks and valleys of the crystal oscillation was proposed in [4] to reduce phase error due to energy injection and enable lower amplitude oscillation, reducing power. However, this approach requires accurate T/4-delay generation and bootstrapped pulses at 32kHz to activate the driver. Instead, HERO injects high energy in short pulses at 4kHz around the peak and valley of the crystal oscillation. Between two injection events, the crystal is free running and the effect of low-frequency noise is minimized (Fig. 3.3.1). Pulses are higher energy to compensate for 8 cycles of XO loss (vs. 1 cycle) and therefore inject less efficiently. However, the lower injection frequency reduces switching loss at the driver inputs and pulse generator, yielding overall lower power.

Figure 3.3.1 presents the architecture of HERO. A proposed T/4-delay clock slicer converts sinusoidal crystal waveform, V_1, into an output clock of 32kHz, and it also introduces a delay of T/4 that provides proper timing for energy injection. This delay is controlled through bias current I_{REF}, which is designed to be proportional to V_{DD}. An 8-to-1 frequency divider generates the 4kHz clock for energy injection and accurate bias-current generation. The proposed differential all-NMOS driver requires only two bootstrapping circuits compared to four in a traditional PMOS/NMOS complementary driver [5]. This saves power and also enables super-cut-off operation, which reduces leakage from V_{DDL} during the free-running phase. Compared to pulse injection XOs with a delay-locking loop (DLL) [4] or phase-locking loop (PLL) [2], this open-loop structure does not require a large capacitor for ripple reduction or loop stability, saving layout area.

Figure 3.3.2 shows the schematic of the T/4-delay clock slicer. In recent XOs, a delay circuit for injection timing follows the slicer and the slicer delay itself is minimized by increasing current [4], or power is optimized at the cost of delay variation across PVT [5]. The proposed slicer merges the slicer and delay function and uses an accurate current reference derived from the XO frequency itself to control this delay accurately. Cascode transistors M_{CP} and M_{CN} are added for higher output impedance at node V_{ramp} as well as reduced Miller effect. Figure 3.3.2 shows simulated crystal waveforms at node V_1 and slicer outputs (with ideal I_{REF}) to show delay variation due to the slicer itself.

Figure 3.3.2 also shows frequency divider, pulse generation, and bootstrapping circuits. Pulse width is set to 1µs, and I_{REF} biases the delay cells to control pulse width across PVT. Even with careful layout and dummy fill control, parasitic capacitance remains at 20 to 30fF in the pulse generator and the bootstrapped 0.9V domain, which would result in ~600pW power consumption at 32kHz. By lowering frequency to 4kHz on most of these signals (green in Fig. 3.3.2), overall pulse generation and bootstrapping power reduces by 3× in measurement, which conservatively includes frequency-divider power (141pW) although it is often already present in real-time clock logic. Operating at a lower frequency is feasible but the overhead due to extra frequency dividers and bigger drivers would be larger than the reduction of the switching loss.

Reference current generation (Fig. 3.3.3) uses a voltage feedback loop to regulate V_{Reg} to V_{REF}, set to $V_{DD}/5$. V_{REF} and switched-capacitor resistance at the 4kHz clock define the current, I_{Reg}, which is mirrored to obtain I_{REF}. Since I_{REF} is designed to be 11pA and V_{Cap} is switched between ground and a relatively low voltage of 90mV (V_{DD}=0.45V), there are two design challenges to control PVT sensitivity of I_{REF}: switch leakage and clock feedthrough to node V_{Cap}. Ultra-low-leakage composite switches [6] are used to suppress leakage by reducing V_{DS} of “off” transistors. Dummy switches and transmission gates are implemented to compensate clock feedthrough. The two amplifiers in this block are self-biased with I_{REF}. Simulated I_{REF} variation is –2% to 10% across V_{DD} from 0.45V to 0.9V and 15 conditions (TT/FF/SS/FS/SF at –40/25/100°C). The V_{DD} dependence of I_{REF} is intentional and cancels out delay dependence of V_{ramp} on V_{DD} (Fig. 3.3.2).

The HERO design was fabricated in 40nm CMOS. A Chip-on-Board (COB) package is used to reduce parasitic capacitance at the crystal nodes, and there is no external capacitor for the crystal. The output frequency is 32.788kHz (ECS-2X6-FLX crystal) and total C_L is estimated at <1.9pF. Ten chips were tested with 10 ECS-2X6-FLX crystals across –25°C to 85°C. Figure 3.3.4 shows total power and frequency deviation across temperature with V_{DD} swept from 0.4V to 0.9V (V_{DDL} = 0.15V). Frequency variation due to the COB package is measured to be within ±3ppm by re-soldering one crystal to all 10 COBs. The average power consumed by the frequency divider in the 10 chips is 141pW at 0.45V, which is 28% of the total 0.51nW. In most highly duty-cycled systems, frequency dividers are already included with the XO (e.g., to enable calendar functions), which alleviates this power overhead. Figure 3.3.5 shows the measured waveform of the crystal at node V_2, monitored through an on-chip source follower. Allan deviation floor is 2ppb, and is measured in a temperature chamber at 25°C, 0.45V V_{DD}, and 0.15V V_{DDL}. Three baseline XOs are tested to show the frequency stability improvement offered by pulse injection with high energy-to-noise ratio: 1) A Pierce XO with a discrete inverter on PCB; 2) on-chip Pierce structure (also used for startup) with slicer and IREF; 3) HERO with 32kHz injections. The Pierce XO on PCB consumes 1.9µW at an oscillation amplitude of 1.1V, while the other two baselines are tested with 0.45V V_{DD} and 0.15V V_{DDL}. Because the ECS-2X6-FLX crystal has a temperature limit of 85°C, 1 COB chip with ECX-34Q-S crystal (–40 to 125°C capable) was tested to show stable operation across –25°C to 125°C. Operation at lower temperature than –25°C can be achieved with a higher V_{DD} than 0.45V.

Figure 3.3.6 summarizes HERO performance and compares it to prior state-of-the-art nW XOs. The proposed design achieves the lowest power consumption, operates at the widest temperature range, and demonstrates 5× lower Allan deviation floor. Figure 3.3.7 shows the die micrograph and COB package.

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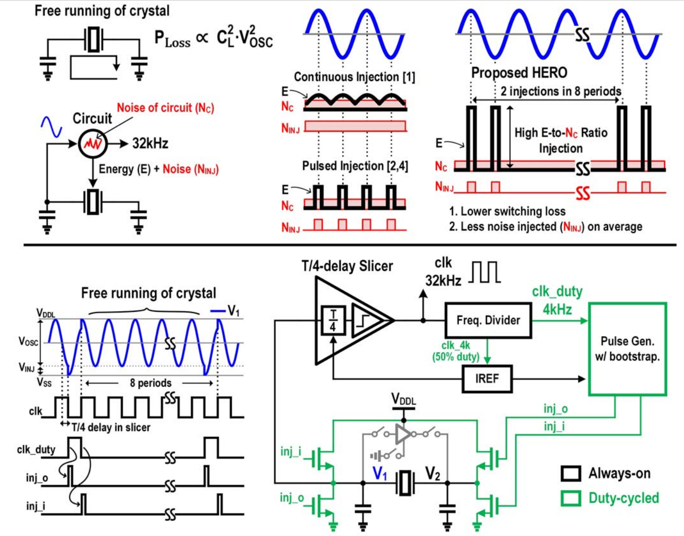

Figure 3.3.1: Concept of the proposed pulse injection of high energy-to-noise-ratio oscillation (HERO), architecture, and signal waveforms.

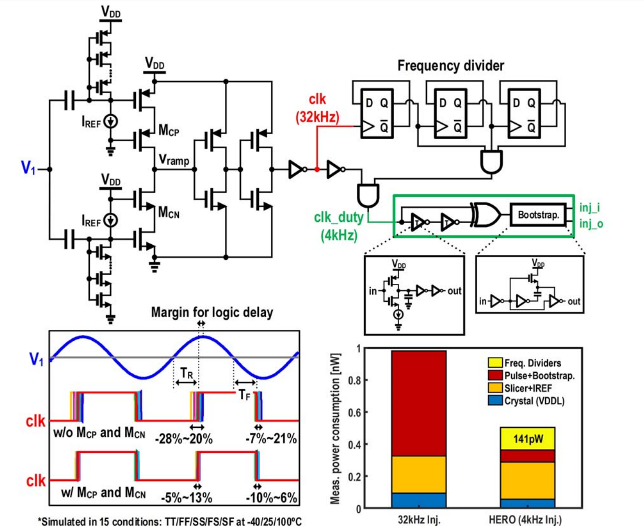

Figure 3.3.2: Simplified schematic of the proposed T/4-delay clock slicer with frequency divider, pulse generation, and bootstrapping circuit.

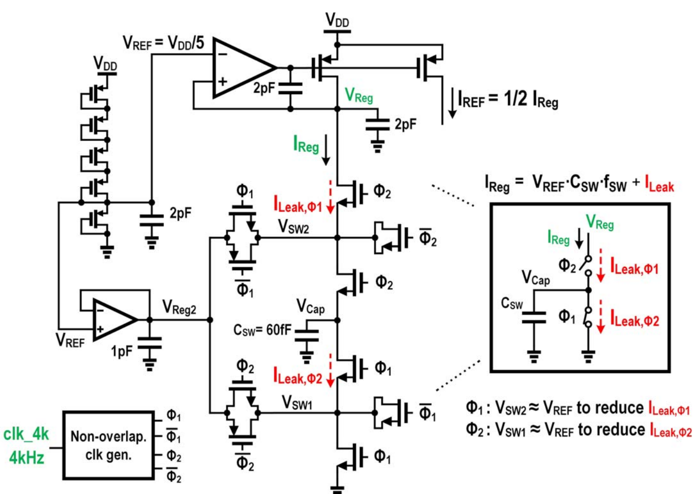

Figure 3.3.3: Simplified schematic of IREF with switched-capacitor resistance.

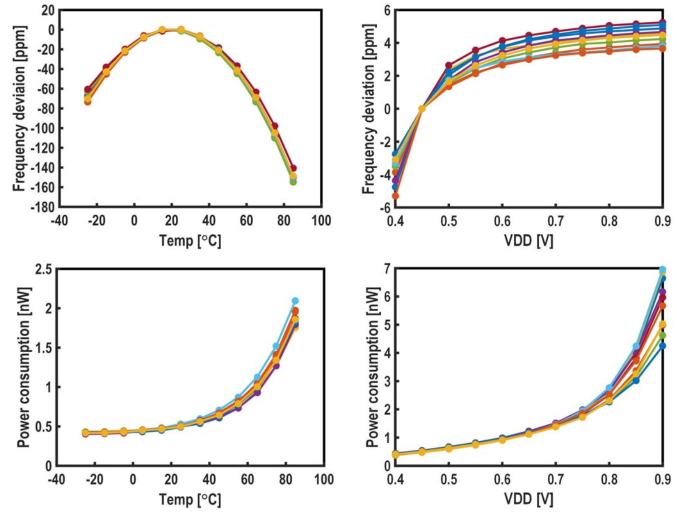

Figure 3.3.4: Measured results of 10 chips in COB packages: frequency deviation vs. temperature and V_{DD} (V_{DDL} = 0.15V); power vs. temperature and V_{DD} (V_{DDL}=0.15V).

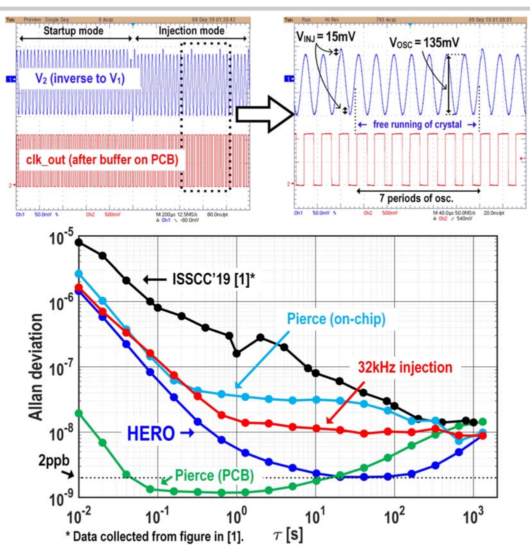

Figure 3.3.5: Measured crystal waveform and measured Allan deviation of HERO and three baseline approaches.

	This work		ISSCC'19 [1]	VLSI'17 [2]	JSSC'16 [3]	JSSC'16 [4]	ISSCC'14 [5]
Technology	40nm		65nm	55nm	130nm	180nm	28nm
Area [mm^2]	0.02		0.027	0.16	0.062	0.3	0.03
Supply Voltages [V]	0.45 & 0.15		0.5	0.4 & 0.1	0.3	0.94	0.15
Output Frequency [kHz]	32.788kHz	32.796kHz	-	-	32.768kHz	32.76783kHz	-
Crystal Operating temperature	ECS-2X6-FLX -40 to 85 °C	ECX-34Q-S -40 to 125 °C	ECX-34Q* -40 to 85 °C	-	-	ECS-2X6-FLX -40 to 85 °C	-
Amplitude Across Crystal [mV]	135	130	<9$	100	230	160	-
Load capacitance [pF]	<1.9**	1.55**	-	-	6	10~20	Parasitic
Power @25°C [nW]	0.51	0.55	0.55	1.7	1.5	5.58	1.89
Power w/o f divider @25°C [nW]	0.37	0.41	0.55	1.7	1.5	5.58	1.89
Temperature stability [ppm] (Variation due to crystal***)	154 (<169) -25 to 85 °C	410 (252~441) -25 to 125 °C	80 (70~144) -20 to 80 °C	109 -20 to 80 °C	150 0 to 80 °C	133 (<144) -20 to 80 °C	48.8 -20 to 80 °C
Line sensitivity [ppm/V]	18	30	13	6.7	7	30.3	85
Allan deviation floor [ppb]	2	4	14	25	70	10	10
# samples reported	10	1	20	1	25	1	1
Calibration Required?	NO		NO	NO	YES	YES	NO

* Confirmed by the author through email.
$ Calculated with $V^2/2R$ < 0.55nW, R is 70kΩ (ESR of ECX-34Q crystal).
** Estimated with output frequency.
*** Intrinsic temperature stability of the crystal itself, taken from datasheet

Figure 3.3.6: Comparison with existing ultra-low-power-XO state-of-the-art.

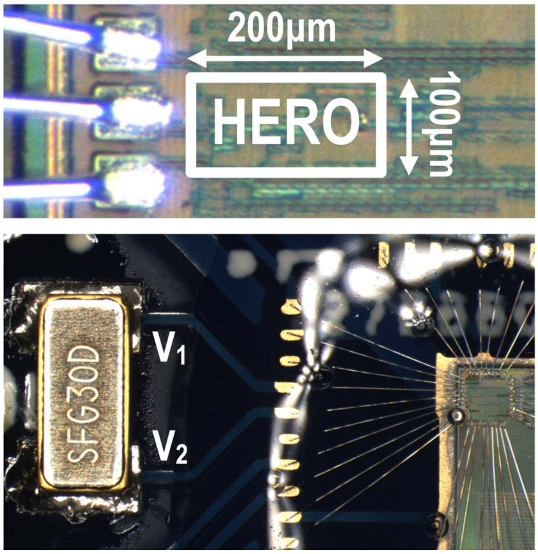

Figure 3.3.7: Die micrograph and COB package with transparent epoxy.

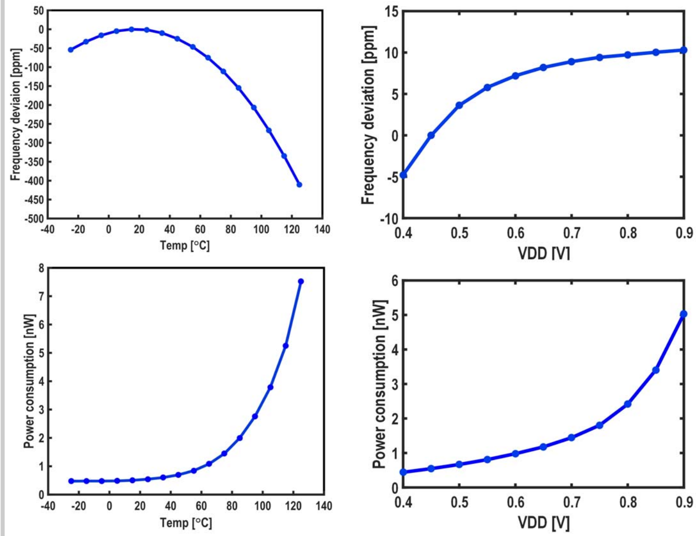

Figure 3.3.S1: Measured results of 1 chip in COB with ECX-34Q-S crystal.

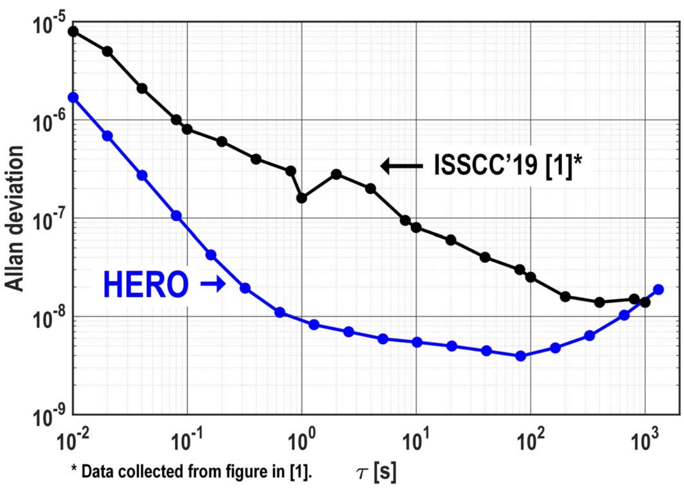

Figure 3.3.S2: Measured Allan deviation with ECX-34Q-S crystal at V_{DD} = 0.45V and V_{DDL} = 0.15V; Comparison with [1] that also uses ECX-34Q crystal.

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