An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Sense-and-Set Rectifier

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***Abstract*— Piezoelectric energy harvesters (PEHs) are widely deployed in many self-sustaining systems, and proper rectifier circuits can significantly improve the energy conversion efficiency and, thus, increase the harvested energy. Various active rectifiers have been proposed in the past decade, such as synchronized switch harvesting on inductor (SSHI) and synchronous electric charge extraction (SECE). This article presents a sense-and-set (SaS) rectifier that achieves maximum-power-point-tracking (MPPT) of PEHs and maintains optimal energy extraction for different input excitation levels and output voltages. The proposed circuit is fabricated in the 0.18-μm CMOS process with a 0.47-mm^2 core area, a 230-nW active power, and a 7-nW leakage power. Measured with a commercial PEH device (Mide PPA-1022) at 85- and 60-Hz vibration frequency, the proposed circuit shows 512% and 541% power extraction improvement [figure of merit (FoM)] compared with an ideal full-bridge rectifier (FBR) for ON-resonance and OFF-resonance vibrations, respectively, while maintaining high efficiency across different input levels and PEH parameters.**

***Index Terms*— DC–DC converter, maximum-power-point-tracking (MPPT), piezoelectric energy harvesting (PEH), rectifier.**

I. Introduction

ENERGY harvesting from ambient sources has drawn much interest in recent decades as it can provide power for energy-autonomous systems or significantly extend the lifetime for battery-powered systems. Among various energy harvesting techniques, the use of piezoelectric materials to harvest energy from mechanical vibration has become popular due to its high power density and good sustainability. A piezoelectric energy harvester (PEH) converts mechanical strain into electrical charge by means of the direct piezoelectric effect [1], and the charge can be extracted to generate ac power (usually in the nW–mW range), which can be applied to the electrical load. The output power of a given PEH can be optimized in terms of these two processes. On the one hand, the efficiency of the electromechanical energy conversion is optimized when the PEH is precisely vibrated at its resonant frequency, matching the natural characteristics of its mass-spring-damping system. This is rarely achieved in practical applications since most ambient vibration sources have a relatively unstable, broadband frequency spectrum [2]. Hence, some prior works have aimed to improve the bandwidth energy conversion, although with limited success [3], [4]. On the other hand, the design of interface circuits that perform impedance matching or maximum-power-point-tracking (MPPT) can significantly improve the charge extraction efficiency and, thus, increase the output power of the PEH. Most of the circuit techniques discussed in this article aim to improve the efficiency of this process rather than control the electromechanical conversion.

Among various interface circuits, full-bridge rectifiers (FBRs) are the most commonly used for their simplicity and stability [5], [6]. However, their power efficiencies are usually low since most of the PEH-generated charges are not extracted but remain within the large intrinsic capacitors of the PEHs. Several different techniques have been proposed to help with energy extraction from PEHs. The bias-flip (BF) technique, proposed by Ramadass *et al.* [7], manually sets a high bias voltage at the PEH's output in order to extract more energy from a certain charge generated by the PEH. When the charge generation (current) changes the direction with the input vibration oscillation, the bias voltage is flipped. This is performed adiabatically to limit the energy loss of the operation. Prior BF-based works generally achieved the highest power efficiency when compared to other energy extraction techniques, and they can be divided into two categories, synchronized switch harvesting on inductor (SSHI) [8]–[10] and synchronized switch harvesting on capacitor (SSHC) [11]–[13], depending on whether an inductor or a capacitor array is used for the voltage flip. Other charge extraction techniques, such as synchronous electric charge extraction (SECE) [14] and energy pile-up resonant circuit [15], are generally less power efficient than the BF-based circuits but offer other advantages such as being more suitable for non-periodic vibrations.

However, all the above techniques have disadvantages for MPPT while extracting energy from PEHs. Theoretically, SSHI and SSHC can achieve near-MPPT in energy harvesting,

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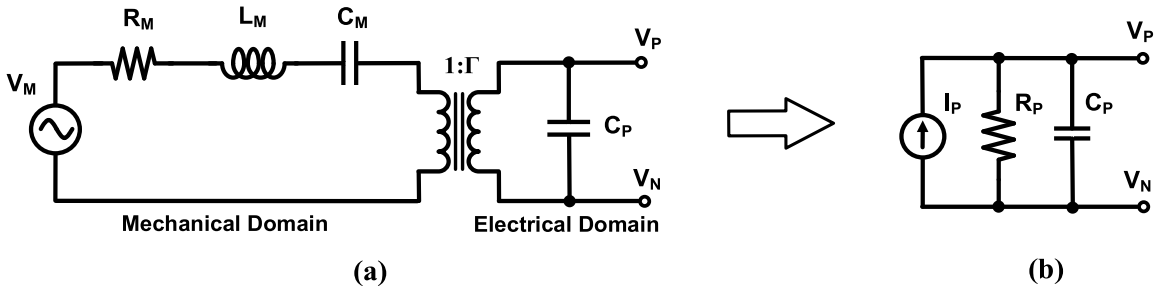

Fig. 1. Modeling of the piezoelectric transducer. (a) Complete model with the electromechanical coupling. (b) Simplified model on the resonant frequency.

but they usually do not adapt to various input-vibration types (periodic or shock) and amplitudes, which decreases their power efficiencies in practical applications. SECE automatically adapts to different vibration amplitudes, but its efficiency is significantly degraded by the large intrinsic capacitor C_P, and it generates unregulated output voltage for non-periodic vibrations.

In this article, we present a sense-and-set (SaS) interface circuit for PEHs, which is fundamentally different from prior techniques and achieves MPPT for arbitrary input vibrations. The proposed SaS technique has the following advantages over prior art.

1) SaS dynamically senses the PEH's charge generation and sets the harvesting voltage accordingly. The power efficiency of SaS is, thus, adjusted to approach the theoretical limit.
2) SaS maintains MPPT for different vibration types, strengths/amplitudes, and PEH characteristic parameters without the need to manually tune the circuit for each condition.
3) SaS produces rectified output voltage without an additional passive rectifier, which eliminates the conduct loss (voltage drop) associated with the rectifier diode and improves the efficiency, especially for low-amplitude vibration (low-voltage) applications.
4) SaS de-couples the output node from the input so that a fixed output voltage does not interfere with the MPPT. In previous techniques, $V_{\rm OUT}$ needs to change with the vibration strength to achieve high-power efficiency which clearly cannot be performed dynamically.

The remainder of this article is organized as follows. Section II presents the background of the PEH model and interface circuit approaches. The operation principle and implementation of the proposed SaS circuit are described in Sections III and IV, respectively. Section V shows the measurement results and analysis, while the conclusion is drawn in Section VI.

II. PEH Model and Interface Circuits

A. Modeling of Piezoelectric Transducers

The PEH or piezoelectric transducer generates electrical charges when the piezoelectric material is compressed or deflected by mechanical stress derived from external vibrations. It can be modeled as an electromechanical system, as shown in Fig. 1(a). The left part of the model illustrates the mechanical structure of the PEH, in which R_M, L_M, and C_M are the equivalent circuit components for the mass-spring-damping system of the piezoelectric layer. With the electromechanical coupling factor Γ, power generated at the mechanical side is transformed to the electrical side and stored in the PEH intrinsic capacitor C_P. When the PEH is excited at or close to its resonant frequency, L_M and C_M are cancelled out, and the model can be simplified into a model without the transformer, as shown in Fig. 1(b), where

$$I_P = \frac{V_M}{\Gamma R_M} \tag{1}$$

$$R_P = \Gamma R_M^2. \tag{2}$$

I_P defines the charges generated by the PEH in a certain time, and R_P is the equivalent loss in the electromechanical conversion. According to the theory of the maximum power transfer, the load receives the maximum power

$$P_{\max} = \frac{1}{4} I_P^2 R_P \tag{3}$$

from the current source when

$$V_P = V_{\rm MPP} = \frac{1}{2} I_P R_P. \tag{4}$$

However, the impedance of C_P is usually much smaller than R_P at the vibration frequency f (or ω). As a result, the V_P amplitude is much smaller than $V_{\rm MPP}$ even for the open-circuit condition

$$V_{P\text{-OC}} = I_P(R_P || X_{CP}) = \frac{I_P}{\omega C_P}. \tag{5}$$

Since $1/\omega C_P \ll R_P$, $V_{P\text{-OC}} \ll V_{\rm MPP}$. For the same I_P generated by the vibration, the low V_P value limits the power efficiency. Furthermore, V_P will be affected by the impedance-match condition between the PEH and interface circuits. The ideal interface circuit that delivers $P_{\max}$ to the load should achieve complete impedance matching to the PEH, where the load impedance $X_L = R_L + \omega L_L$ is given by

$$R_L = R_P, \quad \omega L_L = \frac{1}{\omega C_P}. \tag{6}$$

However, the required L_L value is usually hundreds of Henries, which is impractical for system-on-chip (SoC) or even on-board systems. Thus, prior interface circuit designs tend to achieve better impedance match by placing V_P to be near $V_{\rm MPP}$, which counteracts the negative effect of C_P. The following paragraphs will continue this discussion in more detail.

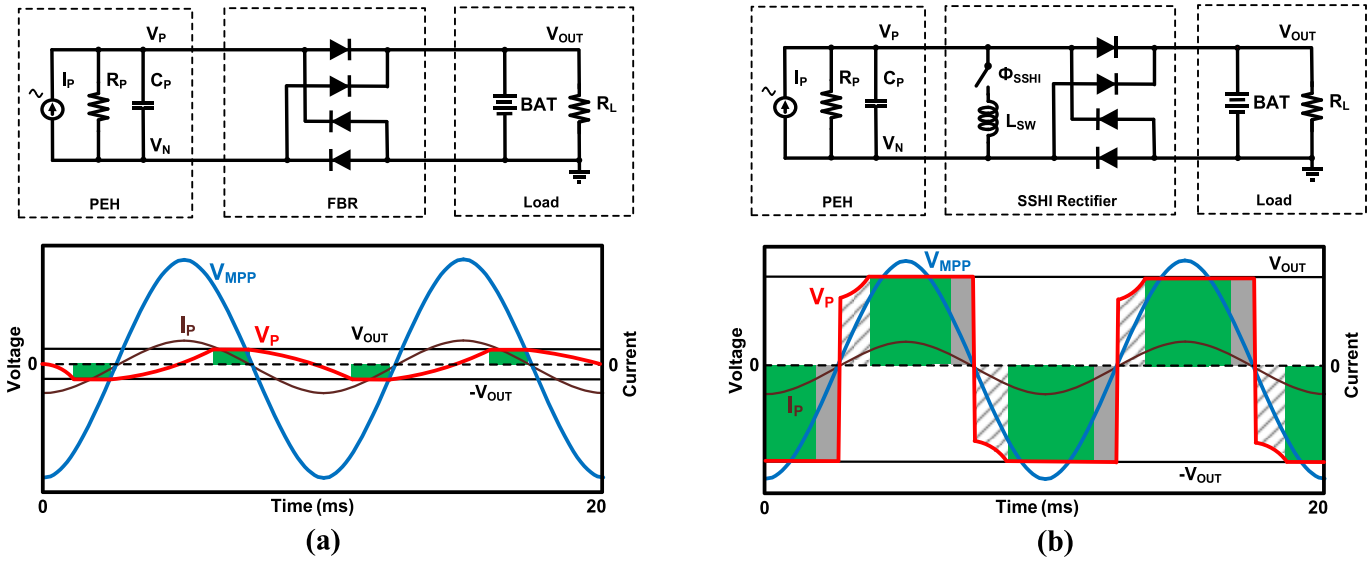

Fig. 2. Schematic and waveform for PEH through (a) FBR and (b) SSHI rectifier.

B. Full-Bridge Rectifier

The FBR is the most widely used interface circuit that allows energy harvesting from PEHs. As shown in Fig. 2(a), the PEH current I_P first charges C_P until V_P reaches V_{OUT}. Then, all of I_P will flow through the FBR diodes to the load (represented by the green region) except for the loss by R_P. When I_P changes the direction with the input vibration, it must first discharge C_P to 0 and then repeat the voltage build-up process in the other direction. During the charge–discharge operation, no power is transferred through the rectifier.

In FBR circuits, the output voltage V_{OUT} must be between 0 and $V_{P\text{-OC}}$ in order to harvest energy from the PEH. Assuming ideal diodes (with no voltage drop) are used, the FBR delivers the maximum output power when V_{OUT} is equal to half of $V_{P\text{-OC}}$, according to [7]

$$P_{\text{max-FBR}} = fC_P V_{P\text{-OC}}^2 = \frac{I_P^2}{2\pi\omega C_P}. \tag{7}$$

Comparing this to the theoretical maximum power, we get

$$\frac{P_{\text{max-FBR}}}{P_{\text{max}}} = \frac{2}{\pi}\frac{1}{\omega C_P R_P} = \frac{2}{\pi Q_{\text{PEH}}} \tag{8}$$

where Q_{PEH} is the quality factor of the piezoelectric transducer. Since generally $1/\omega C_P \ll R_P$, then $Q_{\text{PEH}} \gg 1$ (in the range of 10–100 for most of PEHs), and the maximum output power delivered by an FBR is significantly lower than the theoretical maximum value.

C. Bias-Flip Rectifiers

One reason for the low-power efficiency of the FBR is that V_P is limited within $V_{P\text{-OC}}$, which is far below V_{MPP}, which is shown as the blue line in Fig. 2(a). For the same PEH current I_P, this much lower voltage results in the output power degradation. One effective way to improve the efficiency is to manually set a bias voltage (usually higher than $V_{P\text{-OC}}$) on V_P so that the same I_P produces larger output power. When I_P changes the direction, the bias voltage is then flipped so that no energy is lost due to discharging C_P. The circuits that utilize such a "BF" operation can be divided into two categories, SSHI [7]–[10] and SSHC [11]–[13], depending on whether they use an inductor or a capacitor array for the voltage flip.

Fig. 2(b) shows the schematic and waveform of an SSHI circuit. It still has an FBR for rectifying the output, but it has an additional switch-controlled inductor in parallel. V_P is set manually to be a fixed high voltage, as demonstrated by the red line. I_P will flow through the FBR to the load without charging C_P, as indicated by the green region. When I_P changes the direction, discharging C_P is avoided by turning on the switch and shorting the PEH through the inductor L_{SW}. By precisely controlling the switch's turn-on period, Φ_{SSHI}, V_P will be adiabatically flipped to a slightly lower negative value due to the circuit loss during the flip. Then, the inversed current IP charges V_P back to V_{OUT}, and energy harvesting begins again at this voltage.

From previous discussions, we know that for each interface circuit, the energy extraction from the PEH peaks when V_P gets closer to V_{MPP}. In the SSHI circuit, that is, when $V_P = V_{\text{OUT}} = Q_{\text{BF}} V_{P\text{-OC}}$, and the maximum power delivered by an SSHI rectifier is

$$P_{\text{max-SSHI}} = 2fC_P V_{P\text{-OC}}^2 Q_{\text{BF}} = \frac{I_P^2 Q_{\text{BF}}}{\pi\omega C_P} \tag{9}$$

where Q_{BF} is the combination of quality factors of the PEH and the $C_P L_{\text{SW}}$ resonant circuit, and thus, usually $1 \ll Q_{\text{BF}} < Q_{\text{PEH}}$. Again, we compare it to the theoretical maximum power

$$\frac{P_{\text{max-SSHI}}}{P_{\text{max}}} = \frac{4Q_F}{\pi}\frac{1}{\omega C_P R_P} = \frac{4Q_F}{\pi Q_{\text{PEH}}}. \tag{10}$$

Although the power efficiency seems to be much better than that of an FBR, SSHI circuits does not achieve MPPT because the square-wave-shaped V_P does not track the waveform of V_{MPP}, which is defined by the vibration pattern (normally it will be a sine wave). In addition to the voltage-flip loss, which is shown by the gray dashed region in Fig. 2(b), it also

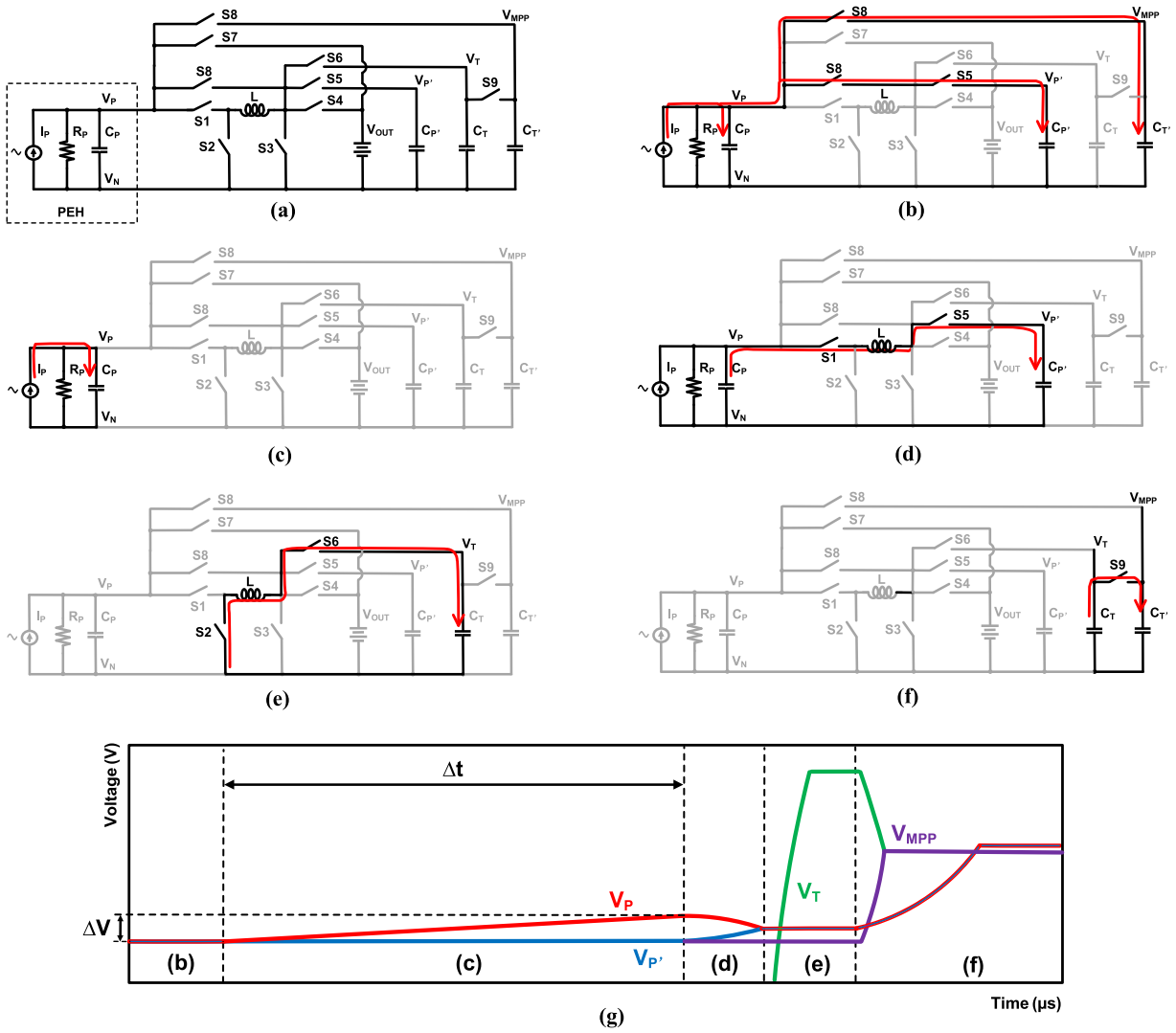

Fig. 3. (a) SaS core circuit where $C_P = C_{P'}$ and $C_T = C_{T'}$. (b) Set initial voltage V_P on C_P, $C_{P'}$, and $C_{T'}$. (c) Leave the PEH in the open circuit and let I_P only charge C_P. (d) Short C_P and $C_{P'}$ through an inductor until their voltages merge. (e) Transfer the energy in the inductor into the smaller capacitor. (f) Short C_T and $C_{T'}$ to get V_{MPP}. (g) Waveforms showing the voltages for important nodes.

has a "dead time" when V_P is larger than $2V_{\text{MPP}}$ and all the current will flow through R_P instead of the FBR (gray solid region). More importantly, in order to achieve the peak output power, SSHI circuits must set the value of V_{OUT} wisely since it defines the amplitude of V_P, which further determines the output power. In practical applications, it is hard to predict $V_{P\text{-OC}}$ and set the correct V_{OUT} before the vibration happens. Also, the system output must be stable, not changing with the vibration's amplitude, and an additional voltage converter will be needed, which further decreases the total power efficiency.

These limitations were partly addressed by some recent energy extraction techniques, such as SECE [14], which builds V_P by the input current I_P and harvests only at the peak value. However, these techniques lack the advantages of using a higher voltage at V_P, so the overall power efficiency is less than the BF-based technique.

III. Fundamentals of Sense-and-Set Technique

To achieve MPPT for PEHs, V_P needs to be equal to V_{MPP}, whose waveform and amplitude vary with the vibration. Hence, there are two main challenges to dynamically adapt V_P to V_{MPP}.

1) Determining the Value of VMPP: It is not possible to directly observe V_{MPP} due to the large intrinsic C_P. Neither can we measure R_P in the circuit (and multiply it by I_P to get V_{MPP}) since it is not in the real electrical domain but derived from the electromechanical model.
2) Maintaining VP Equal to VMPP: If we determine V_{MPP} and V_P is adapted to the V_{MPP} level, its value will change with the oscillation. Since C_P is large, keeping V_P at/near V_{MPP} requires a large energy transfer to charge or discharge C_P, which results in the significant power loss.

Our proposed SaS technique addresses these two challenges by adiabatically estimating the value of V_{MPP} (the "sense" operation) and then adiabatically adjusting V_P to it (the "set" operation). The operation of SaS will be introduced in the following paragraphs.

A. Sense Phase

As previously discussed in Section II-A, a PEH's open-circuit voltage $V_{P\text{-OC}}$ is far less than V_{MPP}. The difference comes from the current that flows through C_P, and, hence, we can recover V_{MPP} by taking this current into account. Assuming the PEH is left in the open-circuit state, then

$$I_P = I_R + I_C \tag{11}$$

where I_R and I_C are the current flowing through R_P and C_P, respectively. I_R can be derived by V_P/R_P, in which R_P is an unknown but fixed value for a given PEH. To measure I_C, we can wait for a short-time period Δt and measure the voltage accumulation ΔV on a capacitor C_P. I_C is approximately constant during Δt, and its value is given by

$$I_P = \frac{V_P}{R_P} + \frac{C_P \Delta V}{\Delta t}. \tag{12}$$

Then, V_{MPP} can be recovered by

$$V_{\text{MPP}} = \frac{1}{2} I_P R_P = \frac{1}{2}\left(V_P + \frac{R_P C_P}{\Delta t}\Delta V\right). \tag{13}$$

Since R_P, C_P, and Δt are constant, we can "sense" V_{MPP} no matter what the current V_P is by measuring ΔV.

However, since we want to keep Δt relatively short (for the approximation that I_C is constant), the resulting ΔV is usually in the sub-mV range. In order to operate with such a small signal, it is necessary to design delicate amplification and offset-cancelling circuits, which induce large power overhead. Fortunately, the energy difference from ΔV on the capacitor C_P is not small due to the large value of C_P. In SaS, we use an inductor-based amplification where we transfer the energy difference into a smaller capacitor to generate higher voltage (tens of mV). Then, a serial-to-parallel switched capacitor array is used to further convert it to higher voltage (hundreds of mV).

Fig. 3(a) shows the SaS circuit schematic, which consists of multiple switches, capacitors, and a shared inductor. It can be reconfigured to different sub-circuits during the sense phase, as shown in Fig. 3(b)–(f); the red curve shows the direction of current flow. Initially, C_P, $C_{P'}$, and $C_{T'}$ are at the same potential as they are all connected and charged by the PEH [Fig. 3(b)]. When the sense phase begins, the PEH is left in the open-circuit mode for the time Δt, and a voltage difference ΔV develops between C_P and $C_{P'}$ [Fig. 3(c)]. Since C_P and $C_{P'}$ have relatively large capacitances, their energy difference is large, and we can use this for the charge-based amplification. In Fig. 3(d), we first short C_P and $C_{P'}$ through the inductor L to equalize their voltages, energizing L by

$$E_L = \frac{1}{2}\left[C_P V_P^2 + C_P(V_P + \Delta V)^2 - 2C_P\left(V_P + \frac{\Delta V}{2}\right)^2\right] = \frac{1}{4} C_P \Delta V^2. \tag{14}$$

E_L is then transferred into a much smaller capacitor C_T in Fig. 3(e) to get a higher voltage V_T

$$V_T = \sqrt{\frac{2E_L}{C_T}} = \sqrt{\frac{C_P}{2C_T}}\Delta V. \tag{15}$$

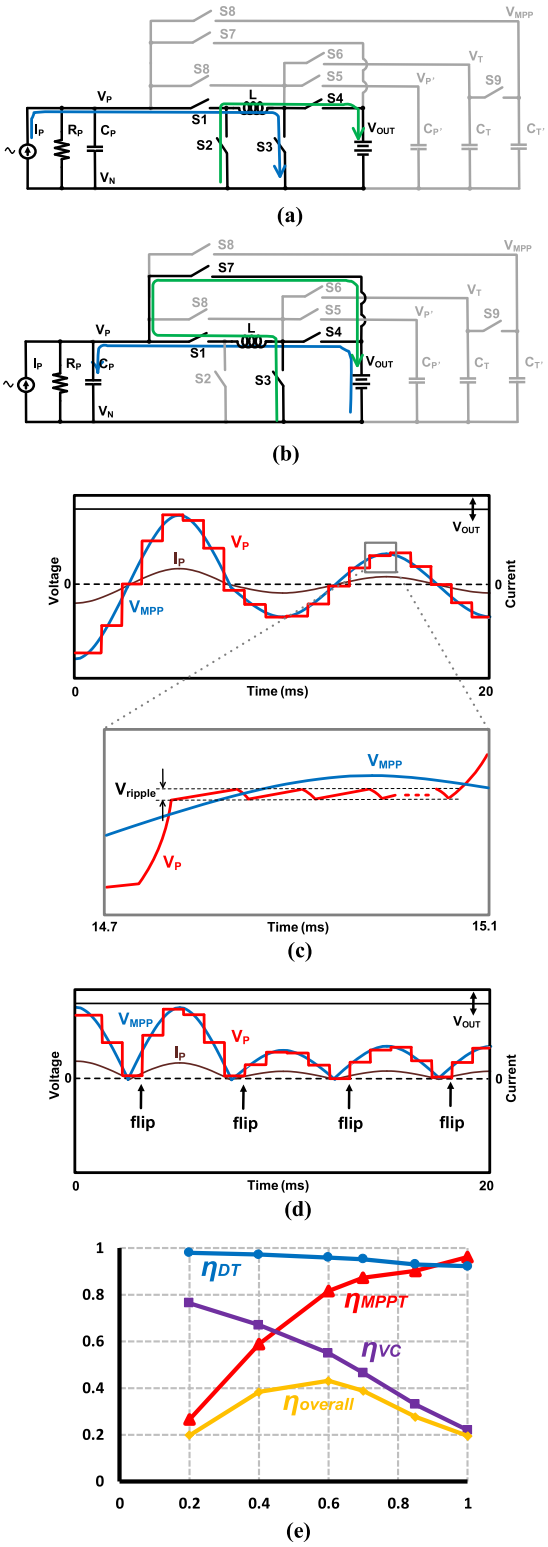

Fig. 4. SaS rectifier in the set phase. (a) Down-convert operation. (b) Up-convert operation. (c) SaS waveform (without voltage flip) and its zoomed-in view region. (d) SaS waveform with voltage flip. (e) SaS efficiency with different MPPT ratios.

By replacing the ΔV term in (13) with V_T, we rewrite the V_{MPP} expression as follows:

$$V_{\text{MPP}} = \frac{1}{2} I_P R_P = \frac{1}{2}\left(V_P + V_T \frac{\sqrt{2C_T C_P R_P^2}}{\Delta t}\right). \tag{16}$$

If the constant $\sqrt{2C_TC_PR_P^2/\Delta t}$ is tuned to be 1, then V_{MPP} is the average of V_P and V_T. Thus, in Fig. 3(f), we short C_T and $C_{T'}$ to generate V_{MPP} and we can set V_P to this value for the MPPT operation.

B. Set Phase

The SaS circuit "sets" V_P to V_{MPP} after obtaining its value during the sense phase. This is performed by configuring the SaS circuit into an inductor-based up-down converter, as shown in Fig. 4(a) and (b). Converting the voltage up and down are adiabatic processes; the blue path shows the charging or discharging current that energizes L, and the green path shows the energy recycle back to the battery.

After converting V_P to V_{MPP}, the SaS maintains V_P around this value by disconnecting itself from the PEH, as shown in Fig. 4(c). Then, I_P gradually charges C_P, causing V_P to rise, and when $V_{P'}$ exceeds the preset threshold, SaS harvests from C_P by down-converting its voltage back to V_{MPP} to maintain MPPT. The harvested energy is then transferred to the load (battery), and V_{OUT} can be arbitrarily set regardless of the input amplitude.

The set phase lasts until V_{MPP} drifts away after a time period, and the SaS ceases energy harvesting and enters the sense phase again. The new sense phase happens at the old V_{MPP} value, and error correction is performed to get the new V_{MPP}. Then, SaS converts V_P to the new V_{MPP} and begins another round of harvesting. By re-sensing repeatedly at a higher frequency than the vibration, the SaS technique achieves energy harvesting that tracks V_{MPP} dynamically, as shown in Fig. 4(c). Also, when the current crosses zero and changes its direction, there is a voltage flipping operation so that VP remains positive, as will be further explained in Section III-C.

Since SaS always performs energy harvesting near the maximum power point, its power efficiency can approach 100% except for the loss caused by circuit non-ideality, which is given by

$$\frac{P_{\mathrm{SaS}}}{P_{\max}} = \eta_{\mathrm{MPPT}}\eta_{\mathrm{DT}}\eta_{\mathrm{VC}}. \tag{17}$$

In (17), η_{MPPT} is the MPPT tracking error for V_P not perfectly following V_{MPP}, and η_{MPPT} characterizes the dead-time loss since SaS does not harvest energy during the sense phase. There is a tradeoff between η_{MPPT} and η_{DT} when choosing the SaS frequency. More frequent SaS operations increase the V_{MPP} tracking precision and, thus, improve η_{MPPT}, but degrade η_{DT} because the circuit spends more time overall in determining V_{MPP}.

With the optimal frequency, the efficiency of $\eta_{\mathrm{MPPT}}\eta_{\mathrm{DT}}$ is usually around 85% or higher. However, the voltage conversion loss due to the switching and conduction activities usually dominates the total efficiency number. Although the inductor-based voltage converter has a high efficiency itself, it transfers the energy in $C_P(\propto C_PV_P^2)$ which is several times larger than the energy generated by the PEH in each cycle ($\propto V_P^2/R_P$). Hence, the energy loss in the voltage conversion is amplified by this ratio, resulting in a low η_{VC}.

Fig. 4(e) shows the post-pex simulation result for (17). The x-axis is the proportion of V_P/V_{MPP} and the y-axis is the overall efficiency of the system. We know from Section II-A that the efficiency should be optimized when $V_P/V_{\mathrm{MPP}} = 1$ in the ideal condition. However, larger V_P/V_{MPP} ratio results in larger amount of energy transfer, which significantly reduce η_{VC} as well as the overall efficiency. Hence, the system efficiency peaks at smaller V_P/V_{MPP} which means we track V_{MPP} at a proportion of its exact value. In such cases, the overall efficiency is around 42%, mainly due to the low conversion efficiency. To further increase the overall efficiency, we could probably use low-series-resistance (LSR) inductor or other converter topologies to reduce the conversion loss.

C. Flipping Phase

The advantages of SaS come from its dynamic adjustment of V_P according to the vibration waveform. However, this restricts the use of conventional rectifiers that handle negative voltages. To address this problem, we implemented a flipping phase which is a special case of the set phase. When the V_{MPP} generated in the sense phase is negative, it indicates that I_P has changed direction and V_{MPP} entered its negative half-cycle. V_P is then converted to this negative V_{MPP} as usual in the set phase but followed by a flipping operation, where the connections to the two PEH terminals are swapped. As a result, V_P is flipped to the positive value and future V_{MPP} will stay positive until the next flipping happens.

The flipping phase happens twice for each vibration cycle, and it ensures that V_P remains positive without the use of rectifiers, as shown in Fig. 4(d). Some energy loss may be incurred in the flipping operation; however, since the V_P values at the time of flipping is near zero, the loss is typically negligible.

D. Calibration Phase

As previously mentioned in (16), it is necessary to tune the constant $\sqrt{2C_TC_PR_P^2/\Delta t}$ to be 1 so that V_{MPP} can be obtained by averaging V_P and V_T. Unlike C_P and C_T, the value of R_P is difficult to measure or control, and it varies among different PEHs. Moreover, there may be mismatches on V_T due to circuit non-idealities, resulting in inaccurate V_{MPP} estimates. To compensate for this, the SaS circuit performs self-calibration by adjusting the sense phase time Δt automatically without knowing the values of these parameters.

The calibration process is very similar to the sense phase in terms of obtaining V_{MPP}. But instead of entering the set phase, SaS converts VP to $2V_{\mathrm{MPP}}$ and performs another sense operation at this voltage. If the voltage V_T appears to be negative (which means V_P was over-estimated in the previous sense phase due to a V_T constant larger than 1), SaS decreases Δt to get a lower V_T and compensate for the larger constant. The process is repeated, and Δt is adjusted in a digit-step manner until there is a positive V_T, which indicates over-tuning.

The calibration phase only needs to be performed once when SaS is connected to a new PEH. Once the right Δt value is

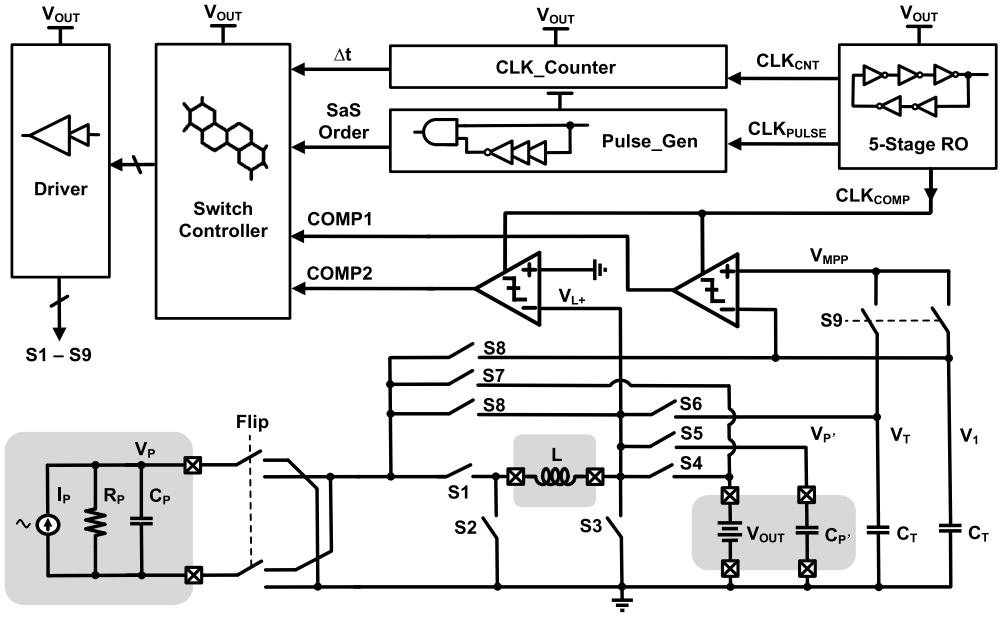

Fig. 5. Top-level diagram for the proposed SaS circuit (grayed area indicates components that are off-chip).

TABLE I
CIRCUIT PARAMETERS FOR THE SAS CIRCUIT

Component	Parameters
S1 - S4, S7	W/L = 100μm/0.5μm
S5 - S6, S8 - S9	W/L = 0.5μm/0.3μm
Flip Switch	W/L = 200μm/0.5μm
C_P, $C_{P'}$	10nF
C_T, $C_{T'}$ [a]	1pF

[a] In order to increase V_T we prefer C_T to be small. However, there is a relatively large parasitic capacitor for the off-chip inductor, so we want to keep C_T large enough to overcome the parasitic loss during the amplification. The decrease on amplify ratio is then compensated by a parallel-to-serial switched capacitor circuit.

tuned, the SaS circuit can harvest energy from the PEH with MPPT for arbitrary vibration inputs.

IV. CIRCUIT IMPLEMENTATION OF SENSE-AND-SET

A. Inductor-Sharing Circuit

The top-level schematic of the proposed SaS circuit is shown in Fig. 5. The lower part is the inductor-sharing circuit, which performs the adiabatic SaS operations. In addition to what was described in Section II-A, there is one additional switch pair that connects PEH with the SaS input to assist the flipping phase. By combining the "flip" switch with the up-down converter that was previously introduced, SaS eliminates the passive rectifier which limits the efficiency for low vibration (voltage) applications.

All switches are implemented with CMOS transmission gates but with different sizing considerations. For switches with only a control purpose, minimum-sized transistors are used for low switching loss. For the switches on the power path between the PEH and the load, the transistor sizes are selected to optimize the total conduction loss and switching loss during voltage conversion. A list of detailed switch sizes and other parameters can be found in Table I.

B. Clock Generator

SaS clocks are implemented on-chip and divided into three domains.

1) The MPPT clock (f_{MPPT}) defines the frequency of SaS refreshing its V_{MPP} value by performing SaS operations. This clock frequency, which is denoted by f_{MPPT}, is usually in the 1-kHz range, tens of times higher than the vibration frequency.
2) The digital counter clock (f_{CNT}) is related to the sense phase time Δt. Since $\Delta t = N_{\mathrm{CNT}}/f_{\mathrm{CNT}}$, a larger f_{CNT} means finer control over Δt but higher power overhead. Hence, the clock frequency is chosen to be 100 kHz.
3) The comparator clock (f_{COMP}) runs the clocked-comparator and controls the switches for voltage conversion and is implemented to be 10 MHz in order to achieve high power efficiency by decreasing timing errors.

For low-power operation, the three clocks are generated with the five-stage ring oscillators (ROs) proposed by Lee *et al.* [16] to achieve constant energy-per-cycle across wide frequency range. As shown in Fig. 6(a), the ROs consist of leakage-based inverters with an additional low-V_{th} (LVT) device pair in the middle. When the input voltage flips, the leakage path through the LVT latch controls the delay of output toggling and determines the oscillation frequency. Further tuning on the frequency can be achieved by adding a current path with the parallel transistors. The voltage to bias parallel transistors (VBP or VBN) are generated by diode-connected transistors and selected with a 64-to-1 multiplexer.

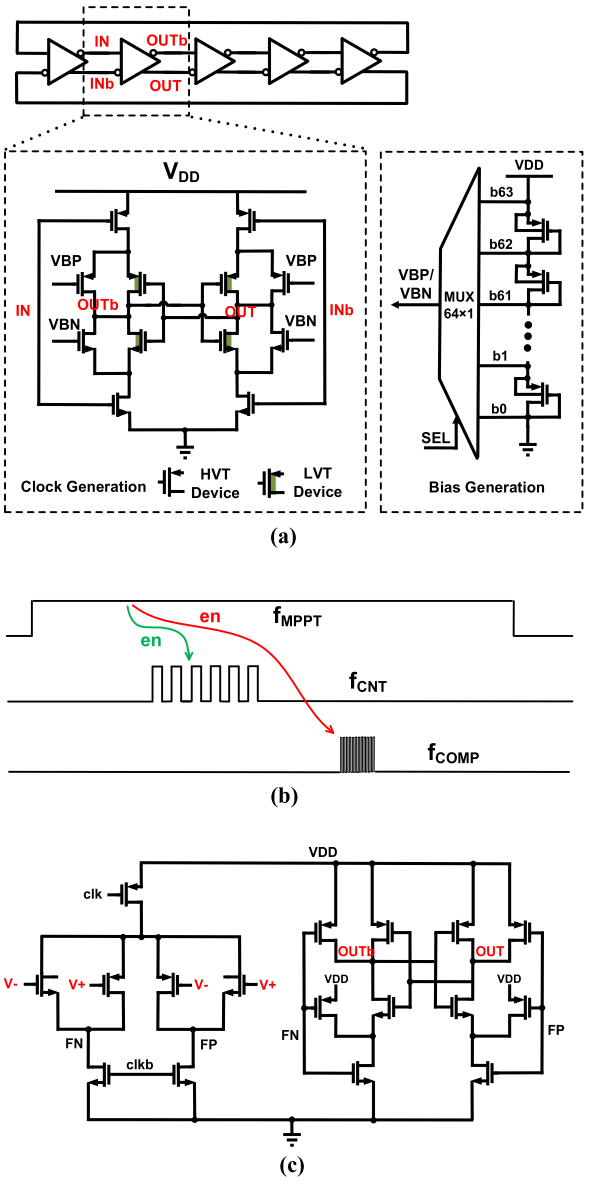

Fig. 6. (a) Circuit schematic of the five-stage RO and its biasing circuit. (b) f_{CNT} and f_{CMOP} that run at higher frequency are awoken by f_{MPPT} at a specific time. (c) Schematic of two-stage comparator.

Among the three clocks, f_{MPPT} needs to be always-on in order to track V_{MPP} in real time. It will result in large power overhead if we run the oscillator at 10 MHz and divide it to generate f_{MPPT}. Instead, we implemented three separate ROs in SaS, and the fast ROs (f_{CNT} and f_{COMP}) are only awoken when their controlled blocks are used. Fig. 6(b) shows the duty-cycled clocks for the counter and comparators.

C. Pulse Generation and Clock Counter

The sequential SaS operation is hard-coded in the SaS, and its order is determined by the pulse generation circuit. The circuit takes f_{MPPT} as input, propagating its rising edge through multiple delay stages, and generates pulses that activate different switches in SaS. The delay cells are similar to what is used in clock generation, with specific bias voltage to control its delay and the pulse width.

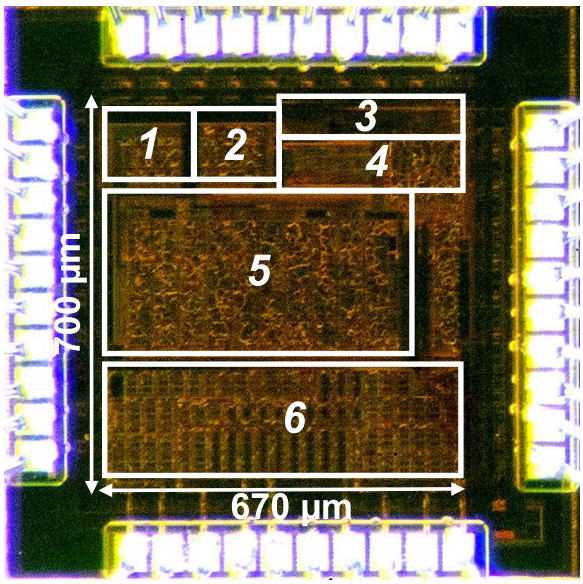

Fig. 7. Micrograph of the test chip fabricated in the 180-nm CMOS process. The active area of the circuit is 0.47 mm^2. (1) Bias voltage generator. (2) ROs. (3) Scan chain for tuning. (4) Clocked comparators. (5) Pulse generator. (6) Inductor sharing circuit.

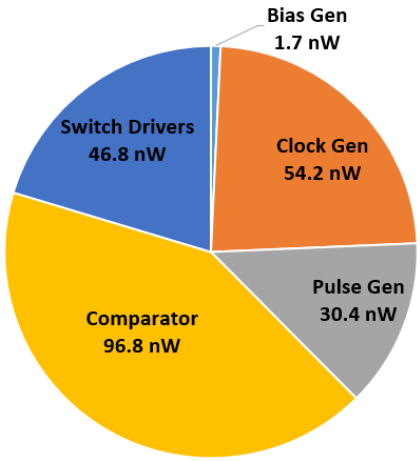

Fig. 8. Breakdown of power consumptions of SaS sub-circuit blocks under the normal operation. The total power (230 nW) is measured in a room temperature and the proportion numbers come from post-pex simulation.

Especially, the pulse width that defines Δt cannot be hard-coded as it needs to be adjustable during the calibration phase. Thus, we implemented a digital counter that counts f_{CNT} until it reaches a given number N. Then

$$\Delta t = \frac{N}{f_{\mathrm{CNT}}} \tag{18}$$

where f_{CNT} determines the resolution of Δt, and N gives the range. The value of N is stored in another counter-like structure that is kept tuned during the calibration phase.

D. Comparators

The SaS circuit performs voltage conversion when it changes V_P. The voltage conversion efficiency η_{VC}, which dominates the overall SaS efficiency as we discussed,

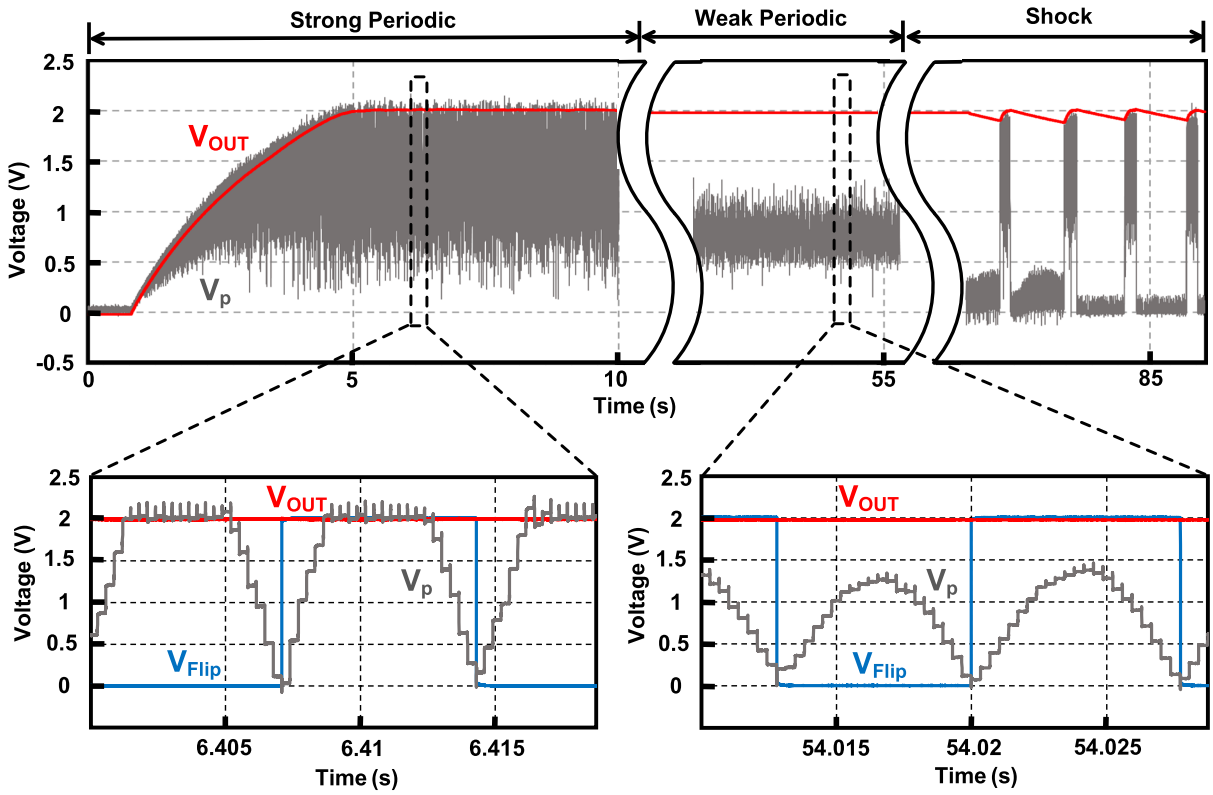

Fig. 9. Measured transient waveform of V_P, $V_{\rm OUT}$, and the $V_{\rm Flip}$ (flip control signal) under different vibrations in the long term (top) and its zoom-in view regions (bottom). Amplitude/frequency for strong and weak periodical vibrations are 2 g/85 Hz and 0.2 g/85 Hz, respectively. The shock vibration has an amplitude of 3 g, with a (rough) period of 1 s.

is affected by the timing error of the switches. To determine the correct timing signals for the switches, we implemented two comparators in SaS, as shown in Fig. 6(c). The first one compares V_P with the target voltage and produces turn-off signals when V_P has been converted to the target voltage. The second one performs cross-zero detection for the inductor L's current by measuring its terminal voltage and helps with the energy recycling from L.

In order to control the switching activities for voltage conversion while maintaining high efficiency, the comparator clock signal $f_{\rm COMP}$ needs to be approximately 10 MHz to reduce timing error. We implemented $f_{\rm COMP}$ in a highly duty-cycled manner where only when a switching activity begins, the fastest oscillator is enabled and provides clocks to the comparator. Since the switching time is only a small portion of the total SaS time, both the comparator and the corresponding oscillator will be idle for most of the time. By this technique, we reduced the power consumption of timing control from 14.5 μW to 151 nW, as shown in Section V.

E. Switch Controller and Switch Drivers

The sequential signals generated by the pulse generator, clock counter, and comparators need to be mapped into the final control signals that apply to S1–S9. Thus, a look-up table is implemented, and the switch control signals are buffered to drive some of the large switches in SaS. The power supply for the switch controller as well as other circuit blocks comes from $V_{\rm OUT}$, which is the harvested energy. But for testing purpose, we use separate 2-V supply so that we can quantify the power consumption by the SaS circuit. To extend the output voltage and the operation range of SaS, the switches can be implemented with high-voltage transistors, and a level converter may be inserted between it and the controller circuit.

V. Measurement Results and Analysis

The proposed SaS circuit [17] is designed and fabricated in the 180-nm CMOS process with a core area of 0.47 mm^2, as shown in Fig. 7. The measured leakage and active power in the room temperature for SaS are 7 and 230 nW, respectively, and Fig. 8 shows the power proportion of each circuit block when SaS is in operation. In addition, 91% of the clock generation power and 88% of the comparator power are related to the high-frequency operations ($f_{\rm COMP}$), while the latter only takes about 1% of the total operation time. The fabricated chip was tested with a commercially available piezoelectrical transducer, PPA-1022 from Mide Technology, Woburn, MA, USA. The transducer was clamped on the PPA-9001 kit (position 0 with 11.2-g tip mass) and mounted on a shaker table (Sentek Dynamic IA20N) as the vibration source. The transducer is excited with a 85-Hz sinusoidal signal (OFF-resonance), a 53-Hz sinusoidal signal (ON-resonance), as well as pulse/chock signals.

Fig. 9 shows the SaS start-up and harvesting waveforms with 85-Hz periodic and shock vibrations. Given an initial vibration to the PEH, the SaS circuit harvests energy from it and gradually builds up $V_{\rm OUT}$ and V_P amplitude until they

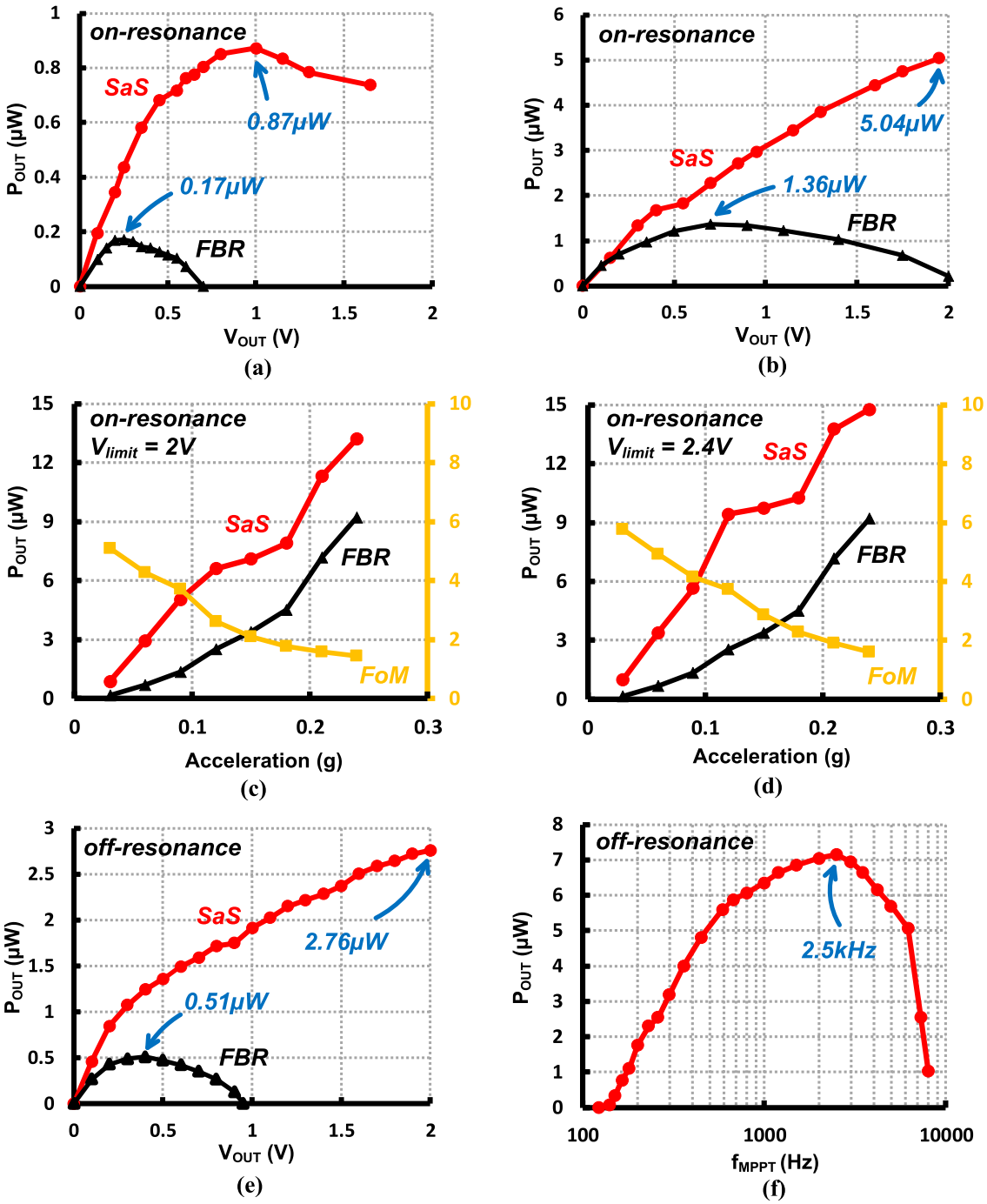

Fig. 10. Measured output power of SaS and ideal FBR for (a) different V_{OUT} values with 0.03 g/53 Hz vibration, (b) different V_{OUT} values with 0.09 g/53 Hz vibration, (c) different vibration strengths with $V_{\mathrm{limit}} = 2$ V, (d) different vibration strengths with $V_{\mathrm{limit}} = 2.4$ V, (e) different V_{OUT} values with 0.5 g/85 Hz vibration, and (f) different f_{MPPT} values and different input vibration strengths.

reach 2 V, the voltage limit for this CMOS process. Since the V_{MPP} value for the strong vibration may exceed 2 V, V_P stops tracking it but maintaining at 2 V to approach V_{MPP}, and SaS performs partial MPPT for energy harvesting (left bottom in Fig. 9). This limitation can be removed by implementing the inductor sharing circuit in high-voltage process so that higher V_{OUT} can be expected. When the input vibration is relatively weak (right bottom in Fig. 9), V_P tracks V_{MPP} for its whole period, and optimized energy extraction from the PEH is achieved. If the vibration is of pulse type, which is common in practical applications, V_P still tracks the input and performs MPPT for the activation period and remains static for the intermittent time. In addition, V_{OUT} is kept at the same value with different vibration strengths and types, which decouples the output node from the input and makes SaS self-adaptable to various vibration sources.

We measured the electrical output power of the PEH using an SaS circuit and compared it with that obtained using an ideal FBR, which we implemented off-chip with active diodes (MAX40200 with <10-mV voltage drop). Fig. 10(a) and (b)

TABLE II
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART INTERFACE CIRCUITS

Publication	Process	Tech-nique	PEH Type	C_P	Frequency	Input Type	$V_{P\text{-}OC}$	FoM (periodic)	$\frac{FoM}{Q_{PEH*}}$	FOM (shock)	Input/output decoupling
JSSC 2010 [7]	0.35µm	SSHI	MIDE V22B	9nF	225Hz	Periodic	2.4V	4×	0.168	N/A	No
JSSC 2016 [8]	0.35µm	SSHI	MIDE V21/22B	9.6 - 27nF	134.6-229.6Hz	Periodic & Shock	0.8V	6.81×	0.286	2.69×	No
CAS 2017 [10]	0.25µm	SSHI	MIDE V22B	19nF	144Hz	Periodic	4.9V	2.07×	0.087	N/A	No
ISSCC 2018 [11]	0.18µm	SSHC	Custom MEMS	1.94nF	219Hz	Periodic	2.5V	3.58 - 8.21×	Unknown	N/A	No
JSSC 2017 [12]	0.18µm	SSHC	PSI-5A4E ($5mm^3$)	78.4pF	110kHz	Periodic	2V	4.83×	Unknown	N/A	No
JSSC 2017 [13]	0.35µm	SSHC	MIDE V21BL	45nF	92Hz	Periodic	2.5V	2.7-9.7×	0.057-0.206	N/A	No
ISSCC'18 [14]	40nm	SECE	MIDE PPA-1011	43nF	75.4 Hz	Periodic & Shock	2.85V	3.14×	0.132	4.20×	No
[15]	0.35µm	Energy pileup	Unknown	220nF	100Hz	Periodic	1.3V	4.22×	Unknown	N/A	No
This Work	0.18µm	SaS	MIDE PPA-1022	8nF	53Hz 85Hz	Periodic & Shock	2.13V 0.95V	5.12× 5.41×	0.299 0.316	4.59×	Yes

*The value of Q_{PEH} is measured for this work to be 17.12, and the value for other works are estimated from the product datasheet. For example, from the datasheet of Mide V22B we know its capacitance CP=9nF and the serial resistor RM=2.4kΩ at f=100Hz. Using a common Γ value of 42, we calculated the quality factor of this device to be 23.8.

shows the measured output power versus different V_{OUT} values at the PEH resonant frequency. For low vibration strengths such as in Fig. 10(a), the FBR power is limited by its low V_P, while the SaS circuit can convert V_P to higher values and track V_{MPP}. Therefore, SaS achieves 4–5 times higher efficiency than the FBR [which means the figure of merit (FoM) is around 4–5]. For relatively stronger vibrations such as Fig. 10(b), the resulting open-circuit voltage is higher and FBR achieves better power efficiency. In such cases, V_{MPP} amplitude may be larger than 2 V, and SaS can only convert V_P to 2 V to approach V_{MPP}. As a result, the SaS achieves less efficiency gain over the FBR due to its voltage limitation.

Fig. 10(c) shows the relationship of the output power of SaS and FBR over different vibration strengths. Given the mentioned process voltage limit (2 V), the stronger the input vibration is, the lesser the efficiency gain can be achieved by SaS because V_P will be more limited. Hence, the current version of SaS is suitable for low-amplitude-vibration applications, such as harvesting energy from wind-induced vibration of a window or the oscillation of a bridge under traffic. However, this disadvantage can be addressed by increasing the voltage limit by changing the technology or transistor type. In Fig. 10(d), we show that by temporarily increasing V_{limit} to 2.4 V, the SaS achieves better FoM in all testing cases, especially for stronger vibration conditions. Further increase in V_{limit} can be done by implementing the voltage comparator and power switches in high-voltage process, and in such case, the SaS circuit could gain high FoM for wider input power range.

We also measured the output power and the corresponding FoM for OFF-resonance vibrations, as shown in Fig. 10(e). The behavior of SaS stays similar except for the lower power level at the same vibration strength. Another factor that influences the SaS output power is f_{MPPT}, which determines how frequently SaS adapts V_P to V_{MPP}. A low f_{MPPT} results in a large tracking error and low η_{MPPT}, as shown in Fig. 10(f), but if SaS adapts V_P too frequently, its dead time will become evident, and η_{DT} is degraded. For the input vibration with 85-Hz frequency, SaS produces its maximum power with f_{MPPT} being 2.5 kHz, which is about 30 times faster than the vibration. Generally, the optimal value of f_{MPPT} will be between 20 and 35 times the vibration frequency according to the measurement results.

Table II shows the comparison of the proposed SaS circuit with prior state-of-the-art works on PEH. The first three columns show basic information about the circuits, and the next two columns summarize the specifications of the tested PEHs. The next three columns show the vibration frequency, input type, and amplitude, in which the PEHs were tested. The output power of each PEH is measured using energy extraction techniques and normalized with their FBR counterpart, which gives each circuit's FoM.

Among different techniques, SaS achieves a high FoM for the ON-resonance (5.12×) and OFF-resonance (5.41×) input vibrations, as well as shock vibrations (4.59×) and weak vibrations (5.56×). Furthermore, from (8), we know that

$$\frac{P_{\text{max-FBR}}}{P_{\text{max}}} = \frac{2}{\pi\, Q_{\text{PEH}}} \propto \frac{1}{Q_{\text{PEH}}} \tag{19}$$

which means the FoM number is heavily related to the PEH parameters and does not solely reflect the improvements from the circuit techniques. Hence, we propose to normalize the FoM with $1/Q_{\text{PEH}}$ so that it reflects the harvester's output power as a ratio of its theoretical maximum value. Although Q_{PEH} varies with device tuning and setups, we have found two ways to obtain its value during testing.

1) Excite the PEH at its resonant frequency and then plot the signal waveform which is used as the excitation input (same phase with I_P) and the resulting PEH open-circuit voltage (V_P). From the phase shift of these two waveforms, we can calculate the effective quality factor Q for the RC network of PEH.
2) If the above method is not available, we can observe Q_{PEH} by giving the PEH a shock vibration. In such case, V_P will be a damped sine wave, and according to the definition of quality factor, Q_{PEH} equals (to the first order) to the cycles that the sine wave decays to the 5% of its initial value.

For our PEH (Mide PPA-1022), the Q value is found to be 17.1 via the first method, and for prior papers, we estimate the Q_{PEH} with its product datasheet. Using this normalized FoM, SaS achieves the highest gain (0.299 and 0.316) among all other energy extraction techniques for ON-and-OFF resonance vibration inputs. This confirmed the simulation results shown in Section III, and to further improve this FoM, we could use LSR inductor or other high-efficiency converter topology in future designs. In addition, SaS is the only technique that eliminates the input–output coupling effect. If V_{OUT} is high enough, its value does not need to be changed according to the input amplitude to guarantee the optimal harvesting condition. This feature helps SaS maintain a stable output voltage under vibration or load changes, making it suitable for various applications.

VI. Conclusion

This article presents a new energy extraction technique, SaS, for PEH. SaS performs MPPT by dynamically sensing and setting the optimal voltage (V_{MPP}) for the PEH. It also adapts to various input vibrations and load changes while maintaining the peak output power. The SaS circuit was fabricated in the 180-nm CMOS process with a core area of 0.47 mm^2 and a static power of 7 nW. Tested with a commercial PEH (PPA-1022), the SaS chip extracted 5.41× and 4.59× more power from a PEH compared with that obtained with an ideal FBR, and the normalized performance number is the highest among all prior works.

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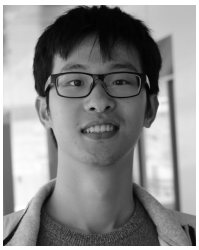

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