KUAN-YU CHEN

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Summary

PhD ECE student interested in **Integrated Circuits**, specialized in **DSP** & **Accelerator Architecture**

Education

- **University of Michigan, Ann Arbor,** Ph.D, Electrical and Computer Engineering
- **University of Michigan, Ann Arbor,** M.S., Electrical and Computer Engineering (GPA: **4.00**/4.00) *04/2020*
  - ◇ Relevant Courses: EECS 427 VLSI Design I, EECS 470 Computer Architecture, EECS 627 VLSI Design II
- **National Taiwan University(NTU),** B.S., Electrical Engineering (GPA: **4.15**/4.30) *01/2018*

Publications

- D.H. Park et. al "A 7.3 M Output Non-Zeros/J, 11.7 M Output Non-Zeros/GB Reconfigurable Sparse Matrix-Matrix Multiplication Accelerator," IEEE Journal of Solid State Circuits (JSSC), Vol. 55, No. 4, September 2020, pgs. 933-944
- S. Pal et. al "A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator using Memory Reconfiguration in 40 nm," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2019

Skills

- **Simulation Tools:** System Verilog, Vivado, Spectre, Virtuoso, HSPICE, MATLAB, SIMPLIS, C, Python
- **Languages:** English, Chinese, Japanese

Work Experiences

- **Graduate Student Research Assistant (GSRA)**,University of Michigan, Ann Arbor *since 01/2019*
  - ◇ Michigan Integrated Circuits Laboratory (MICL) (Advisor: Prof. David Blaauw)
- **Teaching Assistant**, Department of Electrical Engineering, NTU *02/2017 - 01/2018*
  - ◇ EEE 5010 SoC Design Lab, EE 4039 Computer Architecture
- **Intern**, Chip Implementation Center, National Applied Research Laboratories, Taiwan *07/2016 - 08/2016*

Research Experiences

Digital Systems (1 real silicon tape-out)

- **Michigan Integrated Circuits Laboratory, U of M** (Advisor: Prof. David Blaauw) *since 09/2018*
  - ◇ **DAP: Domain Adaptive Processor**
  - ◇ **Transmuter**: Software-Defined Reconfigurable Computer **(taped-out in 28nm process)**
  - ◇ **Reconfigurable Multi-Thread FFT & FIR Accelerators** portable on **FPGA**
- **Department of Electrical Engineering, NTU**
  - ◇ Software Defined Network **OpenFlow Switch** implementation on **SoC** (Advisor: Prof. An-Yeu Wu) *09/2016 - 01/2018*
  - ◇ **SLAM Car** that explores and prints mazes' maps on display screen(controlled by **FPGA**) (EE3016, NTU) *07/2016*

Analog Circuits (2 real silicon tape-out in 0.18um CMOS process)

- **Department of Electrical Engineering, NTU**
  - ◇ Research of **On-Chip DC-DC Voltage Converter** (Advisor: Prof. Tsung-Te Liu) *03/2016 - 01/2018*
  - ◇ Design of 2.4 GHz **All-Digital PLL** and 2.4 GHz **Charge Pump PLL** (Advisor: Prof. Shen-Iuan Liu) *08/2015 - 06/2016*
- **National Chip Implementation Center, Taiwan** (Director: Dr. Liang-Hung Lu)
  - ◇ **Offset Variance Mitigation** of multiple on-chip **Low Power Operational Amplifiers** *07/2016 - 08/2016, 08/2015*

Honors & Awards

- **Presidential Awards,** (Dean's List) **2** times *09/2015, 03/2016*
- **First Prize,** **2017 Undergraduate Innovation Award** *09/2017*
- **Third Prize,** **2017 Integrated Circuits Design Contest** *05/2017*
- **Certificate of Outstanding Achievement,** **2016 Innovative Asia FPGA and SoC Design Contest** *08/2016*
- **Undergraduate Assistantship,** **TSMC** *09/2015 - 06/2016*