YICHEN GU

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EDUCATION

University of Michigan *2019 - Present*
Ph.D. Student in Electrical and Computer Engineering

University of Illinois at Urbana-Champaign *2015 - 2019*
B.S. in Electrical and Computer Engineering

RESEARCH

Research Interest

- Signal Processing
- Algorithm Design
- Machine Learning
- Hardware Acceleration

DNA Read Alignment September 2019 - Present
Algorithm Design *University of Michigan*

- Third-generation DNA sequencing technology produces much longer and more noisy DNA sequences. The state-of-art read mappers follow a seed-chain-extend approach to map DNA sequences to a reference genome. A key to the algorithm is to provide more error-free seeds in the seeding step. New approaches can be applied to the seeding stage to correct the erroneous base pairs.

COURSEWORK

Graduate Level

- Information Theory
- Machine Learning
- Design and Analysis of Algorithms
- Probability Theory and Random Processes
- Accelerator for AI and Health Applications
- Computational Data Science and Machine Learning

Undergraduate Level

- Machine Learning
- Multimedia Signal Processing
- Digital and Analog IC Design
- Digital and Analog Signal Processing
- Data Structure
- Physics and Modeling of Semiconductor Devices

COURSE PROJECTS

Basecaller Accelerator (Team Project) December 2019
Hardware Design *University of Michigan*

· The whole project aims at designing a basecaller for DNA sequencing using SystemVerilog. It's an accelerator of RNN neural network. I was in charge of the design of the convolutional layer plus some verfication work.

Self-Adjusting Helmet (Team Project) February - May 2019
Hardware Design *University of Illinois*

· This project is an electronic-mechanical co-design of a helmet with a rotating shield. The shield rotates towards the direction of sunlight to provide protection. My work is PCB design and some programming of the micro-controller.

Simple Machine Learning Kernal Design (Team Project) December 2018
Digital IC Design *Univeristy of Illinois*

· In this project, we design a simple 4-bit machine learning kernal. It's a pipelined design composed of a clock divider, an accumulator and a comparator. My job is to design the accumulator. The final product is an IC layout.

Simple LDO Design (Team Project) April 2018
Analog IC Deign *University of Illinois*

· This project is a simple LDO circuit. We are trying to design a 2-stage operational amplifier. The final product is a circuit schematic.

Noise Cancelling via Adaptive Filtering (Team Project) December 2017
DSP Algorithm *Univeristy of Illinois*

· In this project, we try to eliminate sinusoidal noise from an audio signal using adaptive filtering. We implemented our algorithm on an Android tablet. My job is to understand and design the algorithm.

FPGA Game Design (Team Project) December 2017
Hardware Design *University of Illinois*

· This project is a game run on an FPGA board with a screen and keyboard. We implemented a simplified version of the game "Bomberman" using SystemVerilog.

TECHNICAL STRENGTHS

Programming	C++, Python, Julia, SystemVerilog
Software	Matlab, Cadence
Typesetting Document	Latex

AWARDS AND RECOGNITIONS

Graduation with High Honor (2019)	University of Illinois
Membership (2018-2019)	Eta Kappa Nu, University of Illinois