LI-YU CHEN

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Summary

MS ECE student interested in **Integrated Circuits** industry, specialized in **Analog Circuits** & **Power Electronics**

Education

- **University of Michigan, Ann Arbor,** M.S., Electrical and Computer Engineering (GPA: **4**.0/4.0) ***01/2021***
- **National Taiwan University(NTU),** B.S., Electrical Engineering (GPA: **3**.83/4.30) ***06/2018***

Skills

- **Tools:** HSPICE, LTspice, Verilog, Spectre, Virtuoso, SIMPLIS, Protel, MATLAB
- **Languages:** English, Mandarin

Honors & Awards

- **WeTech Qualcomm Global Scholars Program** ***01/2017 - 07/2017***
- **Integrated Circuits Design & Layout Test** ***11/2017***
- **Third Prize, 2017 Integrated Circuits Design Contest** ***05/2017***

Working Experiences

- **Intern, Texas Instruments** ***06/2020 - 08/2020***
- **Intern, Analog Devices** ***01/2018 - 11/2018***
- **Intern, National Chip Implementation Center** ***07/2016 - 08/2016***

Research Experiences

- **Michigan Integrated Circuits Laboratory, U of M** (Advisor: Prof. David Blaauw) ***since 01/2020***
  - ◇ High Voltage DC-DC Up Converter
- **Analog Devices** ***01/2018 - 11/2018***
  - ◇ MOSFET gate leakage current sensor in the scale of 0.1nA
  - ◇ ±250V, 0.5A Low Noise Power Supply
  - ◇ Load share circuit for parallel buck-boost DC - DC controllers
- **Energy Efficient Circuits and Systems Lab** (Advisor: Prof. Tsung-Te Liu)
  - ◇ Voltage-Scalable **Ultra-low Power (3.92nW)** All-Digital **Temperature Sensor** ***02/2017 - 01/2018***
    - ∗ **Ultra-low power (3.92nW)** operation in the subthreshold region to sense temperature
    - ∗ **Tape-out** in 0.18um CMOS process
- **National Chip Implementation Center** (Director: Prof. Liang-Hung Lu)
  - ◇ **Low Power** Rail-to-Rail **Operational Amplifier** ***07/2016 - 08/2016***
    - ∗ Full-Custom Design of a Low Power Rail-to-Rail I/O OP Amp operates in subthreshold region
    - ∗ **Tape-out** in 0.18um CMOS process

Selected Term Projects

- **Advanced Analog Integrated Circuits** ***01/2018***
  - ◇ 12-bit 8-MS/s **SAR ADC** with a Split Capacitor Switching Procedure
- **Phase-Locked Loop** ***06/2017***
  - ◇ A Digital Calibration Technique for Charge Pumps in **Phase-Locked Systems**
- **Power Electronics and Integrated Circuit Control** ***06/2018***
  - ◇ 2-MHz **Buck Converter** with AOT/COT Dual-Mode Ripple-Based Control
- **EECS 427 VLSI Design I** ***12/2019***
  - ◇ **RISC Processor** with CORDIC
- **Digital System Design** ***06/2018***
  - ◇ **Pipelined MIPS** with branch prediction, L2 cache, multiplication and division using Verilog