

# ROHIT ROTHE

## PERSONAL INFORMATION

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ADDRESS : 1301 Beal Avenue, Ann Arbor, Michigan - 48109  
EMAIL : [rohitrr@umich.edu](mailto:rohitrr@umich.edu), [rohitrr95@gmail.com](mailto:rohitrr95@gmail.com)  
INTERESTS : Low Power Analog & Mixed Signal VLSI Design and RF VLSI Design

## EDUCATION

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**University of Michigan**, Ann Arbor SEP 2018 - PRESENT  
PhD in Electrical & Computer Engineering  
Advisor: Prof. David Blaauw  
CGPA: **4.0/4.0**

**Indian Institute of Technology Bombay**, Mumbai, India JUL 2013 - JUL 2018  
Dual Degree (B.Tech + M.Tech) in Electrical Engineering  
CGPA: **9.39/10.00**

## PUBLICATIONS

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- **Rohit Rothe**, Sechang Oh, Kyojin Choo, Seokhyeon Jeong, Minchang Cho, Dennis Sylvester, David Blaauw, “**Sample and Average Common-Mode Feedback in a 101 nW Acoustic Amplifier**”, *IEEE Symposium on VLSI Circuits (VLSI-Symp)*, June 2020
- Sechang Oh, Minchang Cho, Zhan Shi, Jongyup Lim, Yejoong Kim, Seokhyeon Jeong, Yu Chen, **Rohit Rothe**, David Blaauw, Hun-Seok Kim, Dennis Sylvester, “**An acoustic signal processing chip with 142-nW voice activity detection using mixer-based sequential frequency scanning and neural network classification**”, *IEEE Journal of Solid-State Circuits ( Volume: 54 , Issue: 11 , Nov. 2019 )*
- **Rohit Rothe**, Rajesh Zele, “**Enhanced IIP2 Chopper Stabilized Direct Conversion Mixer Architecture**”, *2019 International Conference on VLSI Design (VLSID)*, January 2019

## RESEARCH EXPERIENCE

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**Sample and Average Common Mode Feedback for CCIAs** JAN 2019 - PRESENT  
Advisors: Prof. David Blaauw & Prof. Dennis Sylvester, *University of Michigan*

- Devised a switched capacitor based feedback structure which ensures DC bias and sets the high pass corner frequency of the amplifier.
- This technique is used in lieu of a pseudo resistor thereby ensuring reliable performance across temperature and process corners.
- An equivalent resistance as high as 100 TΩ can be implemented on chip using this technique.
- This technique also has the added benefit of programmability of the high pass corner. Using this feature, the amplifier startup and recovery from artifacts can be accelerated.

**Dynamic Matching in Direct Conversion Mixers** MAY 2017 - JUL 2018  
Master's Thesis  
Advisor: Prof. Rajesh Zele, *IIT Bombay*

- Designing a new topology of Direct Conversion Mixer for RF frequency 2.4 GHz with **improved 2<sup>nd</sup> order Input Inter-modulation Point (IIP2)** and lower flicker noise making use of Correlated Double Sampling.
- Investigating RF performance improvements using **chopper stabilization** (Correlated Double Sampling) in various topologies for CMOS RF Mixers.

**Delta-Sigma ADC for Particulate Measurement System** MAY 2017 - JUN 2018  
Research and Development Project  
Advisor: Prof. Maryam S. Baghini, *IIT Bombay*

- Designing a low-voltage, low power and high bandwidth Delta Sigma ADC with **12-bits** resolution
- Aimed to be compatible with requirements of precise **portable energy autonomous instrumentation** systems. Target future application is particulate measurement system with **sensitivity of 1 ppm** (collaboration with University of Cambridge, UK).

## SELECT COURSE PROJECTS

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**Hardware for Chiron Basecaller** | EECS 627 : VLSI Design II WINTER 2019

*Instructor:* Prof. David Blaauw, University of Michigan

- Implemented hardware for a neural network consisting of 3 ResNets and 3 layers of bidirectional RNN layers
- Achieved a performance of 3.2 TOPS/W @ 10 MHz for the CNN. The overall size of the design is 1.68 cm<sup>2</sup> in 130 nm IBM technology.

**Wide Bandwidth Trans-Impedance Amplifier** | EECS 413 : Monolithic Amplifier Circuits FALL 2018

*Instructor:* Prof. Ehsan Afshari, University of Michigan

Designed a 3 stage 4 GHz bandwidth TIA based on inductive peaking for optical fibre communication

**Rational Arithmetic Accelerator** | EE 705 : VLSI Design Lab SPRING 2017

*Instructor:* Prof. Sachin Patkar, IIT Bombay

Optimized 8 bit Dadda multiplier to design 13 stage pipeline for 32 bit multiplier using optimal carry save adders & 8 stage pipelined carry select adders to reduce delay. Achieved > 2x increase in maximum operating frequency.

## ACADEMIC ACHIEVEMENTS

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- Awarded the **Certificate of Appreciation for Excellence in Teaching Assistantship** for the graduate level course of CMOS Analog VLSI Design in the Autumn 2017 semester.
- All-India Rank of **136** in Joint Entrance Examination (JEE - Main) among more than 1.3 million candidates.
- Awarded the **Institute Technical Special Mention** for exemplary performance in the year of 2015-16.

## WORK EXPERIENCE

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**Design and Analysis of Phase Locked Loops** MAY 2016 - JUL 2016

*Guide:* Mr. Rajendrakumar Joish, High Precision Analog Group, Texas Instruments, India

- Investigated the different **architectures** of Phase Locked Loops (PLLs) and characterized their stability using continuous time and discrete time and frequency domain analysis.
- Studied the various designs of individual components constituting a PLL such as Phase Frequency Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillators and Frequency Divider.

**Design and Fabrication of Electric Vehicle for Formula Student** MAY 2014 - JUL 2016

*Part of IIT Bombay Racing Team of 70 students to build India's Fastest Electric racecar for **Formula Student UK**, an international racecar competition; won **FS Award of £3000** for major design improvements*

- Designed and implemented the team's first **Controller Area Network (CAN)** based sensor network on the ORCA car thereby enabling an efficient bus based system for data collection.
- Enabled higher data speed of 500 kbps with increased accuracy and supplemented seamless system integration by significantly reducing the wiring and hence **reducing the harness size**.
- Headed Data Acquisition Division (DAQ), overseeing the team of 4 Junior Design Engineers

## ACADEMIC SERVICES - TEACHING ASSISTANT

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- **EE 619: RF Microelectronics Chip Design**, IIT Bombay SPRING 2019
- **EE 618: CMOS Analog VLSI Design**, IIT Bombay AUTUMN 2017
- **EE 101: Introduction to Electrical and Electronic Systems**, IIT Bombay SUMMER 2017

## TECHNICAL PROFICIENCY

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SOFTWARE      Virtuoso, Calibre, Quartus, NgSpice, LTspice, Eagle  
LANGUAGES     VHDL, Verilog, C++, Python, MATLAB

## RELEVANT GRADUATE COURSEWORK

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UNIVERSITY OF MICHIGAN    Monolithic Amplifier Circuits, Analog –Digital Interface Circuits, VLSI Design I, VLSI Design II, Advanced Analog and Mixed Signal Circuits

IIT BOMBAY                    RF Microelectronics Chip Design, Mixed Signal VLSI Design, CMOS Analog VLSI Design, Systems Design, Digital VLSI Design, Foundations of VLSI CAD