KUSH GOLIYA

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EDUCATION

University of Michigan, Ann Arbor, MI, USA December 2017

Master of Science in Electrical and Computer Engineering

Relevant Courses: VLSI Design I (EECS 427), Computer Architecture (EECS 470), Digital Integrated Technology (EECS 523), Parallel Computer Architecture (EECS 570), Logic Circuit Synthesis and Optimization (EECS 478).

GPA 4.0 / 4.0.

Veermata Jijabai Technological Institute, Mumbai, India June 2016

Bachelor of Technology in Electronics Engineering

Relevant Courses: Basics of VLSI, Mechatronics, Digital Design, Integrated Circuits Application.

GPA 9.65 / 10 (3.95/4). Rank 1 in a class of 74 students.

PROFESSIONAL EXPERIENCE

University of Michigan - Ann Arbor, MI February 2018 - Present

Engineer in Research Associate

- Responsible for hardware and software co-design to accelerate the secondary analysis used in genomics applications including mapping and alignment, sorting and duplicate marking.
- Responsible for hardware architecture research and evaluation aiming to optimize compute and memory bandwidth resources.
- Responsible for testing and deploying hardware designs on AWS F1 environment with Xilinx Ultrascale+ FPGAs.

CME Group, Chicago, IL June 2017 - August 2017

Software Engineering Intern

CME Group is the one of the world's largest and most diverse derivatives marketplace, popular for futures and option trading.

- Designed and implemented the Smart Order Injector to provide a dynamic testing infrastructure for CME's matching engine.
- Responsible for performance analysis and optimization of the Smart Order Injector.

PROJECT EXPERIENCE

16-bit Two stage pipelined processor with In-memory compute 4x4 SRAM Cache September 2017 - December 2017

- Designed the program counter, ALU, Register File of the 16-bit processor, some designed using Automatic Placement and Routing and others by hand using Cadence.
- Designed and implemented the Digital to Analog converters used in the 4x4 SRAM Cache which enables in-memory computation and can be used to perform dot-products between a row matrix and a square 4x4 matrix.
- Developed a testing script which runs analog simulations on the full SRAM design with self-checking capability for easier testing, full system verification and Monte-Carlo simulations.

Smart Order Injector January 2017 - December 2017

- Created a Market Data transmitter and UDP receiver to send and receive historic market data provided by CME group.
- Implemented a pipelined, multi-threaded architecture for the injector to ensure best performance and efficiency.
- Designed and implemented a network interface that can be used by the application to communicate with CME's markets.
- Designed multiple trading strategies that can take trading decisions based on the market analysis done by the application.

Hardware Accelerated Regular Expression Matching January 2017 - April 2017

- Created an algorithm to support multiple nested *Kleene ** and *Kleene +* operations used for matching regular expressions in hardware. This was additional support to the existing architecture HARE proposed by Vaibhav Gogte and Thomas Wenisch (http://pages.cs.wisc.edu/~loris/papers/micro16.pdf).
- Achieved speedup of 16 GB/s (ASIC implementation 50 times faster than *grep* assuming both infrastructures work at the same input bandwidth) with only 72 bytes of memory overhead.

2-way Superscalar Out-of-Order MIPS R10k processor October 2016 - December 2016

- Designed a 2-way superscalar processor based on MIPS R10k design with an out of order execution core.
- Designed the complete fetch stage, branch predictor, branch target buffer and branch history table, instruction cache controller and pre-fetcher.
- Designed a N-way set associative Non-blocking write-back Data cache with LRU replacement which can handle multiple outstanding requests to memory using Miss Status Handling Registers(MSHR).

SKILLS

- **Computer Skills:** SystemVerilog, C, Java, BASH scripting, Cadence, Hspice, Encounter, Python, MATLAB.