

CURRICULUM VITAE

David T. Blaauw

August 2020

I Personal Data

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II Employment History

A. Education

Doctor of Philosophy in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: “Functional Abstraction in Switch-Level Simulation.”
Advisor: Professor Jacob A. Abraham

Master of Science in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: “Automatic Generation of Behavioral Models.”
Advisor: Professor Jacob A. Abraham

Bachelor of Science in Physics with a second major in Computer Science, Duke University, May 1986.

B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

C. Employment History

- September 2007 - Present: Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
- August 2001 - September 2007: Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
- September 1994 - August 2001: Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
- August 1993 - September 1994: Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.
- August 1992 - August 1993: Development Staff Member, IBM Corporation, Endicott, New York.

D. Honors and Awards

- 2019 Distinguished University Innovator Award given to one team in the university for developing and marketing transformative ideas and technologies
- Named the Kensall D. Wise Collegiate Professor of Electrical Engineering and Computer Science, 2019
- Best Student Paper Award, “A 4×4×4-mm³ Fully Integrated Sensor-to-Sensor Radio using Carrier Frequency Interlocking IF Receiver with -94 dBm Sensitivity,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2019
- 2019 IEEE Micro Top Picks special issue on the Computer Architecture Conferences, “Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks”
- 15 year retrospective most influential paper in ISCA 2002 award for groundbreaking research in power-efficient computing, ACM/IEEE International Conference on Computer Architecture (ISCA), 2017
- Member of University of Illinois Engineering Advisory Panel. 2015 through current.
- Ranked as the top publishing author at IEEE VLSI Circuits Symposium over the last 30 years of the conference with 38 publications. June, 2017
- 2016 University Researcher Award, Semiconductor Industry Association (SIA) – Semiconductor Research Corporation (SRC), established by the semiconductor industry association to recognize lifetime research contributions to the U.S. semiconductor industry by university faculty. One award given per year for circuits and technology each.
- 2016 IEEE Micro Top Picks special issue "MBus: The Missing Interconnect that Enables the Modular Millimeter-Scale Computing Class and Connects the World's Smallest Computer,"
- Best Paper Award, “Racetrack Converter: A Low Power and Compact Data Converter Using Racetrack Spintronic Devices,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2015
- 2014 John von Neumann Student Research Award for Excellence in Systems Research – SONIC Annual Review Meeting
- Recognized as top 50 innovator over the last 50 years graduating from the University of Illinois EECS department in 2014
- College of Engineering Innovation Excellence Award for 2013-2014

- Design Automation Conference (DAC) 50th Anniversary award for being the top 10 most cited DAC authors in DAC's 50 year history, June 2013
- Design Automation Conference (DAC) 50th Anniversary award for publishing the most papers in the fifth decade of DAC's history, June 2013
- 2013 University of Michigan Electrical Engineering and Computer Science (EECS) Department Outstanding Achievement Award for innovative research in variation-tolerant and energy efficient integrated circuit design, and exceptional mentoring and teaching in the area of VLSI circuits
- International Solid-State Circuits Conference (ISSCC) 60th Anniversary Special Recognition top 10 contributing author over the last 10 years, February 2013
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award, "Combined Dynamic Voltage Scaling and Adaptive Body biasing for Lower Power Microprocessors under Dynamic Workloads," ICCAD 2002 Conference, November 2012
- Second Prize in the 18th Samsung Human-Tech Thesis Competition for research on millimeter sensor design, February 2012
- IEEE Fellow status, January 2012
- Winner MuSyC Research Consortium annual best poster award, "A Modular 1mm³ Die-Stacked Sensing Platform," Nov 2011
- Winner 11th International VLSI-Symposium Low Power Design Contest, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
- Winner Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Design contest, "Design and Implementation of Centip3De, a 7-layer Many-Core System," Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC), Feb/June 2011
- Best Paper Award, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan, College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for "development of the Razor technology" (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is "at least five years old and has had a significant industrial impact."
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, "Energy Efficient Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007

- Microprocessor Review Analysts' Choice Award in Innovation for "Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design," Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation"
- University of Michigan Henry Russel Award for "Exceptional Scholarship and Conspicuous Ability as a Teacher," November 2004
- Best Paper Nomination, "Parametric Yield Estimation Considering Leakage Variability," ACM/IEEE Design Automation Conference (DAC), June 2004
- Best Paper Award, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, "Noise Analysis Methodology for Partially Depleted SOI Circuits," IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003
- Best Paper Award, "Statistical Delay Computation Considering Spatial Correlations," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, "Pre-route Noise Estimation in Deep Submicron Integrated Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, "Driver Modeling and Alignment for Worst-Case Delay Noise," ACM/IEEE Design Automation Conference (DAC), June 2001
- Best Paper Award, "On-Chip Inductance Modeling and Analysis," ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

III Research Experience

A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

B. Doctoral Students Supervised

<u>Student</u>	<u>Thesis Title/Topic</u>	<u>Graduation Date</u>
Kuan Yu Chen	Low Power Signal Processing Through Reconfigurable Systolic Arrays	In Progress
Andrea Bejarano	mm-Scale Image Sensing Through Low Power Circuit and Algorithm Co-Design	In Progress
Chien-Wei Tseng	Ultra-Low Power RF-Localization for Asset Management	In Progress
Yichen Gu	Computational Genomics for RNA Velocity Modeling	In Progress
Rohit Rothe	Ultra-Low Power Audio Amplification Through Switch Capacitor T-Ohm Resistance Circuits	In Progress
Zhen Feng	mm-Scale RF Communications	In Progress
Jihwan Seol	PLL Design Through Over Sampling Techniques	In Progress
Zhehong Wang	Application of New Technologies to Neural Networks Processors	In Progress
Xiao Wu	Energy Efficient Circuits and System for Internet of Things and Hardware Accelerator Design for Genome Sequencing	July 2019
Li-Xuan Chuo	Miniaturized Low-Power and Energy-Efficient RF Wireless Communication and Sensing Systems	June 2019
Ziyun Li	Energy-Efficient Mobile Computer Vision and Machine Learning Processors	May 2019

Kyojin Choo	Charge-domain analog/mixed-signal circuits and applications	Sept 2018
Yao Shi	Millimeter-Scale and Energy-Efficient RF Wireless System	Aug 2018
Wootae Lim	Ultra-low Power Circuit Design for Miniaturized IoT Platform	May 2018
Taekwang Jang	Circuit and System Designs for Millimeter Scale IoT and Wireless Neural Recording	Dec 2017
Wanyeong Jung	Low-Power Energy Efficient Circuit Techniques for Small IoT Systems	April 2017
Supreet Jeloka	Cross-point Circuits for Computation, Interconnects, Security and Storage	Jan 2017
Yejoong Kim	Robust Circuit Design for Low-Voltage VLSI	May 2015
Nathaniel Pinckney	Near-Threshold design	July 2015
Dongmin Yoon	Low power timer references	Jan 2015
Inhee Lee	Power management for ultra-low power sensors systems	Oct 2014
Gyouho Kim	Ultra-low power visual monitoring	Aug 2014
Bharan Giridhar	Adaptive Computing	Dec 2013
Zhi Yoong Foo	Low power processor design techniques	Aug 2013
Sudhir Satpathy	Fast and low power inconnect fabrics	Dec 2012
David Fick	Adaptive Low-power design	Aug 2012
Yoonmyung Lee	Ultra Low-Power Memory Design	April 2012
Prashant Singh	Reliability analysis and wear-out detection	April 2010
Nurrachman Liu	Automatic tuning of VLSI circuits	April 2010

Brian Cline	Process variation modeling for advance semi-conductor circuits	Feb 2010
Cheng Zhuo	VLSI wearout modeling	Dec 2010
Ravikishore Gandikota	Crosstalk-Noise analysis for nanometer VLSI circuits	Aug 2009
Carlos Tokunaga	Circuits and architectures for secure processing	Sep 2008
Shidhartha Das	Razor: circuit speculation for power and performance efficient design	Oct 2008
Kaviraj Chopra	Statistical timing analysis including spatial correlations	Apr 2008
Eric Karl	Reliable computing on unpredictable silicon	Mar 2008
Sanjay Pant	Power grid analysis and design	Dec 2007
Mini Nanua	Leakage and noise analysis in nano-scale technologies	Apr 2007
Bo Zhai	Dynamic voltage scaling for embedded processor designs	Mar 2007
Rajeev Rao	Modeling and design of low-power VLSI systems under for multiple sources of uncertainty	Jul 2006
Dongwoo Lee	Analysis and minimization of leakage current	May 2005
Aseem Agarwal	Statistical timing analysis for VLSI circuits	Mar 2005

C. Masters Students Supervised

<u>Student</u>	<u>Thesis Title/Topic</u>	<u>Graduation Date</u>
Hengfei Zhong	Power Circuit Design	May 2020
Ashwin Bhat	Error Tolerant Long-Read Alignment for Genomic Sequencing	April 2020
Hyungjoo Seo	Low Power Energy Harvesting	May 2019
Tim Wesley	Low Power Neural Network Accelerators	May 2019
Yu Zeng	Low Power Crystal Oscillator Circuits	Dec 2017
Dongkwun Kim	Low Power Voltage References	May 2017
Skyler Skrzyniarz	Low Power Correlation Architectures for GPS	June 2015
Junhua Gu	Low Power Circuits for Analog to digital interfaces	May 2015
Ruochen Xie	Energy Reduction of FeRAM Memories for Millimeter Sensors	May 2015
Allen Wang	Low Power Level Conversion	May 2014
Naveen Akesh	Low Power Audio Device for Developing World	May 2014
Zhe Yu	RF Communication for Millimeter Scale Sensors	May 2014
Hsi-Shou Wu	Low Power Word-Spotting	April 2014
Siddharth Saxena	Low power correlation circuits	May 2013
Karan Jain	Low power synchronization using ambient RF signals	April 2012
Jordan LeNoach	pH sensor for millimeter sensors	Dec 2011

Jeffrey Yeh	Chip design for the developing world	April 2011
Nate Robert	Low power LDO	Dec 2010
Vikas Vinay	Low power Class-D amplifier for developing world applications	Dec 2010
Abhishek Madhavan	Low power chip design	Dec 2010
Junsun Park	Intra-cellular chip design	May 2010
Jou-ching (George) Sung	Low power ADC design	Aug 2009
Mao-Ter Chen	Low power sensor node design	Dec 2008
Sudharsen Kalaiselvan	Razor-3: A circuit speculation and SEU tolerant circuit technique	May 2007
Deepesh John	Low power design through typical-case optimization	May 2006
Yueh-Chuan Tzeng	Encryption processor for side channel attack avoidance	May 2006
Meghna Singhal	Low power design using subthreshold operation	May 2006
Amir Borna	Analysis of lithographic variations for chip performance	Aug 2005
Amit Jain	Delay modeling for non-ramp input transitions	Nov 2004
Toan Pham	Clock skew reduction using Razor flip-flops	Dec 2003
Bhavana Thudi	Non-iterative switching window computation for delay noise	May 2003
Wesley Kwong	Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs	May 2003

D. Research Grants

- Facebook, “Context-Aware Multi-Sensor Fusion System and SoC Integrated Circuits and Digital Signal Processing,” \$239,752, with \$119,876 to Blaauw, PI: Dennis Sylvester, 1/1/20-12/31/21
- ARM, “ULP Sensor Fusion SoC for Micro Robots and Tiny IoT,” \$320,000 with \$160,000 to Blaauw, PI: David Blaauw, 9/1/19-8/31/21
- Sony Corporation of America, “Ultra Low Power intelligent imaging sensors for the Internet of Things,” \$1,493,433, with \$511,041 to Blaauw, PI: Dennis Sylvester, 9/1/19-8/31/22
- Government Communications Planning Directorate (GCPD)/ Defense Science and Technology Laboratory (DSTL), “Ultra-Miniature Imager Technical Demonstrator,” \$1,057,762, with \$657,762 to Blaauw, PI: David Blaauw, 7/18/19-8/31/20
- Government Communications Planning Directorate (GCPD)/ Defense Science and Technology Laboratory (DSTL), “M3 Audio-Logger,” \$1,204,352, with \$704,352 to Blaauw, PI: David Blaauw, 2/18/19-8/31/20
- Semiconductor Research Corporation (SRC), “Mixed-Signal Circuits Enabling Ultra-Low Power Wireless Sensors,” \$270,000, with \$139,995 to Blaauw, PI: David Blaauw, 1/1/18-12/31/20
- Advanced Energy Consortium (AEC), “Millimeter Scale Down-hole Sensors,” \$650,000, with \$400,000 to Blaauw, PI: David Blaauw, 3/1/18-02/28/21
- National Science Foundation (NSF), “NCS FR - Elucidating the relationship between motor cortex neural firing rates and dextrous finger movement EMG for use in brain computer interfaces,” \$2,276,395, with \$194,603 to Blaauw, PI: Cindy Chestek, 9/1/19-8/31/23
- DARPA, “Domain-focused Advanced Software-reconfigurable Heterogeneous System-on-Chip (DASH-SoC),” \$2,420,233, with \$1,318,078 to Blaauw, PI: Hun-Seok Kim, 7/18/18-6/30/22
- NSF, “SHF: Medium: Compute Caches: Opportunistic Extreme Scale Parallelism In General Purpose Processors,” \$300,000, with \$80,579 to Blaauw, PI: Reetuparna Das, 10/1/18-9/30/20
- Leidos, “Trestle – small acoustic sensors” \$1,882,300, with \$983,104 to Blaauw, PI: David Blaauw, 5/3/19-11/3/20
- National Institute of Health (NIH), “A 100 μ m Scale Single Unit Neural Recording Probe Using IR-Based Powering and Communication,” \$429,971, with \$224,890 to Blaauw, PI: David Blaauw, 9/1/18-8/31/20
- DARPA, “Transmuter: A Reconfigurable Computer,” \$5,845,690, with \$1,524,096 to Blaauw, PI: Ron Dreslinski, 8/6/18-3/30/21
- University of California-San Diego, “OpenROAD: Foundations and Realization of Open, Accessible Design Integrated Circuits and Digital Signal Processing,” \$1,600,000, with \$248,754 to Blaauw, PI Andre Kahng, 6/1/18-5/31/22
- DARPA, “Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits,” \$3,199,021, with \$482,255 to Blaauw, PI: David Wentzloff, 6/12/18-6/11/20
- Leidos, “NZero Acoustic Switch (Dorado),” 930,000, with \$699,424 to Blaauw, PI: David Blaauw, 11/11/17-6/30/19
- National Institute of Standards and Technology (NIST), United States Department of Commerce (DoC), “Decimeter Accurate, Long Range Non-Line-of-Sight RF Localization Solution for Public Safety Applications,” \$997,873, with \$310,041 to Blaauw, PI: Hun Seok Kim, 6/1/17-5/31/21

- Defense Science and Technology Laboratory (DSTL), “Highly Size Constrained Logging Sensor Development,” \$1,971,690, with \$209,999 to Blaauw, PI: David Blaauw, 10/01/16 – 08/15/18
- Sony Electronics, Inc., “Low Power Motion Detection for the Internet of Things,” 1,193,000, with \$400,000 to Blaauw, PI: Dennis Sylvester, 8/1/2016-12/31/2019
- DARPA, “Support for Porting S2CFF Design and Near-Threshold Voltage (NTV) Design Methodology to 32nm CMOS,” \$310,829 to Blaauw, PI: David Blaauw, 12/8/2015-8/31/2017
- DARPA, “Near Zero-Power, Continuous Acoustic Sensing Microsystem using Active Integrated Circuits and Digital Signal Processing,” \$2,505,000, with \$835,000 to Blaauw, PI: Dennis Sylvester, 9/28/2015-7/31/2019
- Semiconductor Research Corporation (SRC), “Infrared-Based Power Delivery and Communication for Implanted Sensors,” \$375,000 to Blaauw, PI: David Blaauw, 6/1/2015-5/31/2018
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Strategic Options and Scalability Limits,” \$1,170,000, with \$585,000 to Blaauw, PI: David Blaauw, 1/1/2015-7/1/2017
- ARM Ltd, “ARM III: Research into Low Energy Computer Systems,” \$3,000,148, with \$555,555 to Blaauw, PI: Trevor Mudge, 2015-2018
- National Institute of Health (NIH), “SCH: INT: Wireless Implantable Electronic Biosensors for Tumor Monitoring,” \$1,759,460 with \$849,804 to Blaauw, PI: David Blaauw, 9/22/2014 - 8/31/2018
- Defense Science and Technology Laboratory (DSTL), “M3 MM scale computing GPS logger,” \$1,352,145, with \$250,000 to Blaauw, PI: David Blaauw, 04/01/14 - 03/31/16
- Defense Science and Technology Laboratory (DSTL), “Dstl Sensor Development Kits,” \$400,000, with \$112,500 to Blaauw, PI: David Blaauw, 12/13/13 - 3/17/14
- DSTL/MoD, “Architectural Design Study for M3 MM Scale Computing GPS Logger,” \$400,000, with \$175,000 to Blaauw, PI: David Blaauw, 8/15/2013-3/14/2014
- NSF, “SHF: Small: Minimally Invasive Error Detection/Correction for Runtime Margin Elimination,” \$450,000, with \$252,750 to Blaauw, PI: David Blaauw, 7/2012-6/2015
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$400,000, with \$135,000 to Blaauw, PI:Kamal Sarabandi, 9/2013-8/2016
- DARPA, “The TerraSwarm Research Center,” \$4,234,183, with \$1,624,897 to Blaauw, PI: Edward Lee, 1/15/2013-12/31/2017
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000, with \$925,000 to Blaauw, PI: Trevor Mudge, 5/2010-5/2015
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Integrating Sensor Elements, Electronics, and Packaging,” \$950,000, with \$226,625 to Blaauw, PI: Yogesh Gianchandani, 6/2012-12/2014
- Semiconductor Research Corporation (SRC), “Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors,” \$360,000, with \$180,000 to Blaauw, PI: David Blaauw 8/2012 - 7/2015
- DARPA, “Systems on Nanoscale Information Fabrics (SONIC) Center,” \$7,008,335, with \$1,401,667 to Blaauw PI: Naresh Shanbhag, 1/2013-10/2017
- DSTL, “MM scale computing for GPS logger,” \$400,000, with \$175,000 to Blaauw, PI: David Blaauw

- Isocline Engineering LLC, “Power Efficient Software Define Radio (SDR) Mobile Architecture Technology for Handheld Devices,” \$220,093 to Blaauw, PI: David Blaauw, 03/01/2013 - 02/28/2015
- Isocline Engineering LLC, “ Programmable Microchip for Accelerating Neuromorphic Object Recognition,” \$45,715 to Blaauw, PI: David Blaauw, 07/01/2013 - 12/31/2013
- QUALCOMM, “Near Threshold Computing,” \$100,000, gift, 8/2011-8/2013
- Oracle, “High Performance Razor Architecture ” \$80,000, gift, 8/2013-8/2014
- AMD, “*In Situ* Wearout Detection and Mitigation,” \$100,000, gift, with \$50,000 to David Blaauw, 11/2011
- Food and Drug Administration, “Smart Rapid Palatal Expander for Pediatric Cleft and Palate Patients,” \$312,000, with \$136,000 to Blaauw, PI: Jeanne Nervina, 9/2011-8/2013
- National Science Foundation (NSF), “Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class,” \$2,533,000, with \$519,265 to Blaauw, PI: David Wentzloff, 08/2011 - 7/2016
- Qualcomm, “Near-Threshold Computing,” \$50,000, gift, PI: David Blaauw, 05/2011
- Department of Energy, “Hardware-Software Co-Design for Non-Volatile Memory in Exascale Systems,” \$525,000 with \$202,747 to Blaauw, PI: Trevor Mudge, 1/2011-12/2013
- Intel Corporation, “A Confidence-Driven Model for Predictable Computing in Future Technologies,” \$249,000 with \$65,916 to Blaauw, PI: Zhengya Zhang, 1/2010-10/2010
- QUALCOMM, “Adaptive Design Solutions for VLSI Circuits,” \$50,000, gift, 09/01/09
- National Science Foundation (NSF), “Reclaiming Moore’s Law through Ultra Energy Efficient Computing,” \$2,778,507, with \$643,700 to Blaauw, PI: Prof. David Blaauw, 9/2009-08/2014
- National Science Foundation (NSF), “Probabilistic Wearout in Nanoscale,” \$300,000, with \$150,000 to Blaauw, PI: Dennis Sylvester, 8/2008-7/2011
- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), “Strained Si/SiGe/Ge Heterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics,” \$17,971,252, with \$600,000 to Blaauw, PI: Steve Koester, 1/2008-12/2009
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” \$8,962,200 with \$700,000 to Blaauw, PI:Kamal Sarabandi, 5/2008-5/2013
- Intel Corporation, “Adaptive Digital Design in the Nanometer Regime,” \$100,000, gift, 3/2008-3/2010
- Sun Microsystems, “Robust Low Voltage SRAM Design,” \$150,000, gift, 9/2007-9/2010
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design,” \$40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon,” \$600,000 to Blaauw, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), “A Design Optimization Framework for Process Variation Tolerance,” \$390,000, with \$195,000 to Blaauw, PI: Dennis Sylvester, 9/2006 - 8/2009
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2006

- Semiconductor Research Corporation (SRC), “CAD Solutions for Parametric Yield Optimization,” \$321,000, with \$160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005-7/2008
- Intel Corporation, “Circuit and Microarchitectural Methods for Subthreshold Design” \$40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), “Sub-threshold Processor Design,” \$60,000 to Blaauw, PI: Kenneth Wise, 5/2005-5/2010
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$5,000,000, with approx. \$1,600,000 to Blaauw, PI: Trevor Mudge, 5/2005-5/2010
- Semiconductor Research Corporation (SRC), “Optimization of Lithographic Induced Variability for Improved Circuit Performance,” \$161,029 to Blaauw, PI: David Blaauw, 9/2004-8/2007
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2004
- Photronics, Inc. \$75,000, gift, 6/2004-5/2005
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000, with \$60,000 to Blaauw, PI: Trevor Mudge, 5/2004-5/2005
- National Science Foundation (NSF), Information Technology Research (ITR), “Collaborative Research ITR: Mobile Supercomputing,” \$1,900,000, with \$320,603 to Blaauw, PI: Trevor Mudge, 11/2003-11/2007
- Intel Corporation, “VLSI Design Curriculum,” \$247,292, with \$61,823 to Blaauw, PI: Richard Brown, 10/2003-10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Power Aware Systems,” \$600,000, PI: David Blaauw, 9/2003-9/2006
- IBM Corporation, Center for Advanced Studies, “Static Performance Analysis under Process and Environment Variations,” \$40,000, Faculty Award, 9/2003
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), “Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current,” \$360,000, with \$160,000 to Blaauw, PI: David Blaauw, 7/2003-7/2006
- National Science Foundation (NSF), “Performance Analysis and Optimization for Nanometer Design,” \$375,000, PI: David Blaauw, 6/2003-6/2006
- ARM, Ltd, “Low Power Computing for Embedded Applications,” \$240,000, with \$60,000 to Blaauw, PI: Trevor Mudge, 5/2003-5/2004
- IBM Corporation, Center for Advanced Studies, “Leakage Characterization and Analysis,” \$40,000, Faculty Award, 9/2002
- National Science Foundation (NSF), Information Technology Research (ITR), “Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty”, \$1,800,00 with \$450,000 to Blaauw, PI: David Blaauw, 8/2002-8/2006
- Intel Corporation, “Power Grid Integrity Analysis,” \$50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), “Power Management for Nanometer design,” \$197,000, PI: David Blaauw, 10/2001-8/2003
- Semiconductor Research Corporation (SRC), “Variability in Chip-Level Performance and Signal Integrity Verification,” \$257,000, PI: David Blaauw, 10/2001-10/2004

IV Teaching Experience

<u>Semester</u>	<u>Class</u>	<u>Course Number</u>	<u>Size</u>	<u>Rating (out of 5) Course/Instructor</u>
Winter 2020	Advanced VLSI Design	EECS 627	26	4.5/4.3
Winter 2019	Advanced VLSI Design	EECS 627	24	4.5/4.6
Winter 2018	Advanced VLSI Design	EECS 627	18	4.08/4.75
Fall 2016	VLSI Design I	EECS 427	36	4.85/4.91
Fall 2015	Digital Integrated Circuits	EECS 312	35	4.58/4.81
Fall 2014	Advanced VLSI Design II	EECS 628	26	4.86/4.90
Winter 2014	Advanced VLSI Design	EECS 627	38	4.77/4.77
Fall 2013	VLSI Design I	EECS 427	39	4.74/4.78
Winter 2013	Introduction to Electronic Circuits	EECS 215	120	3.56/4.09
Winter 2012	Advanced VLSI Design	EECS 627	37	4.87/4.87
Fall 2011	VLSI Design I (Section 2)	EECS 427	18	4.79/4.79
Fall 2011	VLSI Design I (Section 1)	EECS 427	35	4.83/4.83
Winter 2011	Advanced VLSI Design	EECS 427	9	4.88/4.88
Fall 2010	Advanced VLSI Design II	EECS 628	19	4.81/5.00
Winter 2010	Advanced VLSI Design	EECS 627	19	4.85/4.96
Winter 2009	Advanced VLSI Design	EECS 627	23	4.75/4.75
Fall 2008	VLSI Design I	EECS 427	28	4.67/4.56
Winter 2007	Advanced VLSI Design	EECS 627	20	4.79
Fall 2006	VLSI Design I	EECS 427	31	4.89
Winter 2006	Advanced VLSI Design	EECS 627	22	4.55
Fall 2005	Topics in VLSI Design	EECS 598	12	4.25
Winter 2005	Advanced VLSI Design	EECS 627	20	4.79

Winter 2004	Advanced VLSI Design	EECS 627	35	4.59
Fall 2003	Introduction to Logic Design	EECS 270	87	4.77
Winter 2003	Advanced VLSI Design	EECS 627	36	4.61
Fall 2002	Introduction to Logic Design	EECS 270	109	4.77
Winter 2002	Advanced VLSI Design	EECS 627	40	4.31
Fall 2001	Issues in High-Performance Deep-Submicron Design	EECS 598	11	4.75

V Publications

A. Books

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B. Book Chapters

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C. Invited Articles

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3. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyong Foo, Hyeongseok Kim, Anthony Grbic, Dennis

- Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor Nodes with illustration in a miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 64, No. 9, September 2017, pgs. 2237-2249
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159. Mohammad Hassan Ghaed, Gregory Chen, David Blaauw, Dennis Sylvester, "Analysis and Measurement of the Stability of Dual-Resonator Oscillators," IEEE Custom Integrated Circuits Conference (CICC), September 2011
160. Daeyeon Kim, Vikas Chandra, Robert Aitken, David Blaauw, Dennis Sylvester, "Variation-Aware Static and Dynamic Writability Analysis for Voltage-Scaled Bit-Interleaved 8-T SRAMs," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August, 2011
161. Mohammad Hassan Ghaed, Dennis Sylvester, David Blaauw, "A Dual-Passband Filter Architecture for Dual-Band Systems," IEEE Antennas and Propagation Society (AP-S), July 2011
162. Dongsuk Jeon, Mingoo Seok, Chaitali Chakrabarti, David Blaauw, and Dennis Sylvester, "A Super-Pipelined Energy Efficient Subthreshold 240MS/s FFT Core in 65nm," Design Automation Conference (DAC), June 2011
163. Bharan Giridhar, David Fick, Matthew Fojtik, Sudhir Satpathy, David Bull, Dennis Sylvester, David Blaauw, "Adaptive Robustness Tuning for High Performance Domino Logic," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
164. Yejoong Kim, Dennis Sylvester, David Blaauw, "LC²: Limited Contention Level Converter for Robust Wide-Range Voltage Conversion," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
165. Sudhir Satpathy, Ronald Dreslinski, Tai-Chuan Ou, Dennis Sylvester, Trevor Mudge, David Blaauw, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011, **Winner in the 11th Annual International VLSI-Symposium Low Power Design Contest**
166. Nurrachman Liu, Nathaniel Pinckney, Scott Hanson, Dennis Sylvester, David Blaauw, "A True Random Number Generator using Time-Dependent Dielectric Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
167. Dongsuk Jeon, Mingoo Seok, Chaitali Chakrabarti, David Blaauw, Dennis Sylvester, "Energy-Optimized High Performance FFT Processor," International Conference on Acoustics, Speech and Signal Processing (ICASSP), May 2011
168. Gregory Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, "A Dense 45nm Half-differential SRAM with Lower Minimum Operating Voltage," IEEE International Symposium on Circuits and Systems (ISCAS), May 2011

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170. Michael Wieckowski, Gregory Chen, Daeyeon Kim, David Blaauw, Dennis Sylvester, "A 128kb High Density Portless SRAM Using Hierarchical Bitlines and Thyristor Sense Amplifiers," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2011
171. Mark Woh, Sudhir Satpathy, Ronald G. Dreslinski, Daniel Kershaw, Dennis Sylvester, David Blaauw, Trevor Mudge, "Low Power Interconnects for SIMD Computers," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011
172. Chia-Hsiang Chen, Yejoong Kim, Zhengya Zhang, David Blaauw, Dennis Sylvester, Helia Naeimi, Sumeet Sandhu "A Confidence-Driven Model for Error-Resilient Computing," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011
173. Gregory Chen, Hassan Ghaed, Razi-Ul Haque, Michael Wieckowski, Yejoong Kim, Gyouho Kim, David Fick, Daeyeon Kim, Mingoo Seok, Kensall Wise, David Blaauw, Dennis Sylvester, "A 1 Cubic Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor," IEEE International Solid-State Circuits Conference (ISSCC), February 2011
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175. Yoonmyung Lee, Bharan Giridhar, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "A 660pW Multi-Stage Temperature Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization," IEEE International Solid-State Circuits Conference (ISSCC), February 2011
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177. Yoonmyung Lee, Mao-Ter Chen, Junsun Park, Dennis Sylvester, David Blaauw, "A 5.42nW/kB Retention Power Logic-Compatible Embedded DRAM with 2T Dual-Vt Gain Cell for Low Power Sensing Applications," Asian Solid-State Circuits Conference (A-SSCC), November 2010
178. Vineeth Veetil, Dennis Sylvester, David Blaauw, "A Lower Bound Computation Method for Evaluation of Statistical Design Techniques," ICCAD 2010, November 2010
179. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analysis and Optimization of SRAM Robustness for Double Patterning Lithography," ICCAD 2010, November 2010
180. Cheng Zhuo, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Active Learning Framework for Post-Silicon Variation Extraction and Test Cost Reduction," ICCAD 2010, November 2010
181. Prashant Singh, Eric Karl, Dennis Sylvester, David Blaauw, "Dynamic NBTI Management Using a 45nm Multi-Degradation Sensor," IEEE Custom Integrated Circuits Conference (CICC), **Invited Paper** to the *Special Issue on CICC, IEEE Transactions on Circuits and Systems I: Analog and Digital Signal Processing (T-CAS)*, September 2010
182. Vivek Joshi, Michael Wieckowski, Gregory Chen, David Blaauw, Dennis Sylvester, "Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS," IEEE Custom Integrated Circuits Conference (CICC), September 2010

183. Mingoo Seok, Gyouho Kim, David Blaauw, Dennis Sylvester, "Variability Analysis of a Digitally Trimmable Ultra-Low Power Voltage Reference," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010
184. Greg Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, "Crosshairs SRAM - An Adaptive Memory for Mitigating Parametric Failures," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010
185. Mingoo Seok, David Blaauw, Dennis Sylvester, "Clock Network Design for Ultra-Low Power Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August, 2010
186. Nurrachman Liu, Scott Hanson, Dennis Sylvester, David Blaauw, "OxID: On-Chip One-Time Random ID Generation using Oxide Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010
187. Sudhir Satpathy, Zhiyoong Foo, Bharan Giridhar, Dennis Sylvester, Trevor Mudge, David Blaauw, "A 1.07 Tbit/s 128x128 Swizzle Network for SIMD Processors," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010
188. Vineeth Veetil, Yung-Hsu Chang, Dennis Sylvester, David Blaauw, "Efficient Smart Monte Carlo based SSTA on Graphics Processing Units with Improved Resource Utilization," ACM/IEEE Design Automation Conference (DAC), June 2010
189. Vivek Joshi, "Closed-Form Modeling of Layout-Dependent Mechanical Stress," ACM/IEEE Design Automation Conference (DAC), June 2010
190. Mingoo Seok, Scott Hanson, Michael Wieckowski, Gregory K. Chen, Yu-Shiang Lin, David Blaauw, Dennis Sylvester, "Circuit Design Advances to Enable Ubiquitous Sensing Environments," IEEE International Symposium on Circuits and Systems (ISCAS), May 2010
191. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Process Variation and Temperature Aware Reliability Management," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010
192. Michael Wieckowski, Dennis Sylvester, David Blaauw, "A Black Box Method for Stability Analysis of Arbitrary SRAM Cell Structures," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010
193. David Bull, Shidhartha Das, Karthik Shivashankar, Ganesh Dasika, Krisztian Flautner, David Blaauw, "A Power-efficient 32bit ARM ISA Processor using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2010
194. Prashant Singh, Zhiyoong Foo, Michael Wieckowski, Scott Hanson, Matt Fojtik, David Blaauw, Dennis Sylvester, "Early Detection of Oxide Breakdown Through In Situ Degradation Sensing," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
195. Jae-sun Seo, Ron Ho, Jon Lexau, Michael Dayringer, Dennis Sylvester, David Blaauw, "High Bandwidth and Low Energy On-Chip Signaling with Adaptive Pre-Emphasis in 90nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
196. Gregory Chen, Matthew Fojtik, Daeyeon Kim, David Fick, Junsun Park, Mingoo Seok, Mao-Ter Chen, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "A Millimeter-Scale Nearly-Perpetual Sensor System with Stacked Battery and Solar Cells," IEEE International Solid-State Circuits Conference (ISSCC), February 2010

197. David Fick, Nurrachman Liu, Zhiyong Foo, Matthew Fojtik, David Blaauw, Dennis Sylvester, "In Situ Delay Slack Monitor for High-Performance Processors using an All-Digital, Self-Calibrating 5ps Resolution Time-to-Digital Converter," IEEE International Solid-State Circuits Conference (ISSCC), February 2010
198. Cheng Zhuo, Yung-Hsu Chang, Dennis Sylvester, David Blaauw, "Design Time Body Bias Selection for Parametric Yield Improvement," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010
199. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analyzing Electrical Effects of RTA-driven Local Anneal Temperature Variation," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010
200. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Post-Fabrication Measurement-Driven Oxide Breakdown Reliability Prediction and Management," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2009
201. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Interconnect Performance Corners considering Crosstalk Noise," IEEE International Conference on Computer Design (ICCD), October 2009
202. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Near-Field Communications using Phase-Locking and Pulse Signalling for Millimeter-Scale Systems," IEEE Custom Integrated Circuits Conference (CICC), September 2009
203. Mingoo Seok, Gyouho Kim, Dennis Sylvester, David Blaauw, "A 0.5V 3.6ppm/OC 2.2pW 2-Transistor Voltage Reference," IEEE Custom Integrated Circuits Conference (CICC), September 2009
204. Daeyeon Kim, Yoonmyung Lee, Jin Cai, Leland Chang, Steven J. Koester, Dennis Sylvester, David Blaauw, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009, **Best Paper Award**
205. Ronald G. Dreslinski, David Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Reconfigurable Multicore Server Processors for Low Power Operation," International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS), July 2009
206. Vineeth Veetil, Dennis Sylvester, David Blaauw, Saamil Shah, Steffen Rochel, "Efficient Smart Sampling based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence," ACM/IEEE Design Automation Conference (DAC), July 2009
207. Ravikishore Gandikota, Li Ding, Peivand Tehrani, David Blaauw, "Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models," ACM/IEEE Design Automation Conference (DAC), July 2009
208. David Fick, Andrew DeOrio, Jin Hu, David Blaauw, Dennis Sylvester, Valeria Bertacco, "Vicis: A Reliable Network for Unreliable Silicon," ACM/IEEE Design Automation Conference (DAC), July 2009
209. Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Crosstalk-Aware PWM-Based On-Chip Global Signaling in 65nm CMOS," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
210. Mike Wieckowski, Gregory K. Chen, Mingoo Seok, David Blaauw, Dennis Sylvester, "A hybrid DC-DC Converter for Sub-Microwatt Sub-IV Implantable Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
211. David Fick, Andrew DeOrio, Gregory Chen, Valeria Bertacco, Dennis Sylvester, David Blaauw, "A Highly Resilient Routing Algorithm for Fault-Tolerant NoCs," ACM/IEEE Design Automation and Test in Europe Conference (DATE), April 2009

212. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low Power Sensor Platforms," IEEE International Solid-State Circuits Conference (ISSCC), February 2009
213. Carlos Tokunaga, David Blaauw, "Secure AES engine with a local switched capacitor current equalizer," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2009
214. Ronald Dreslinski, Greg Chen, Trevor Mudge, David Blaauw, Dennis Sylvester, Krisztian Flautner, "Reconfigurable Energy Efficient Near Threshold Cache Architectures," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2008
215. Brian Cline, Vivek Joshi, Dennis Sylvester, David Blaauw, "Stress-Enhanced Standard Cell Library Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
216. Jae-Sun Seo, Igor Markov, Dennis Sylvester, David Blaauw, "On the Decreasing Significance of Large Standard Cells in Technology Mapping," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
217. Kaviraj Chopra, Cheng Zhuo, David Blaauw, Dennis Sylvester, Vladimir Zolotov, "A Statistical Approach for Full-Chip Gate-Oxide Reliability Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008
218. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "An Ultra Low Power 1V, 220nW Temperature Sensor for Passive Wireless Applications," IEEE Custom Integrated Circuits Conference (CICC), September 2008
219. Mingoo Seok, Scott Hanson, Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Robust Ultra-Low Voltage ROM Design," IEEE Custom Integrated Circuits Conference (CICC), September 2008
220. Michael Wieckowski, Young Min Park, Carlos Tokunaga, Dong Woon Kim, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "Timing Yield Enhancement Through Soft Edge Flip-Flop Based Design," IEEE Custom Integrated Circuits Conference (CICC), September 2008
221. Sanjay Pant, David Blaauw, "Circuit Techniques for Suppression and Measurement of On-chip Inductive Supply Noise," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008
222. Yoonmyung Lee, Mingoo Seok, Scott Hanson, David Blaauw, Dennis Sylvester, "Standby Power Reduction Techniques for Ultra-Low Power Processors," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008
223. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008
224. Mingoo Seok, Dennis Sylvester, David Blaauw, "Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008
225. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Sensor Data Retrieval Using Alignment Independent Capacitive Signaling," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*, June 2008
226. Mingoo Seok, Scott Hanson, Yu-Shiang Lin, Zhiyoong Foo, Dayeon Kim, Yoonmyung Lee, Nurachman Liu, Dennis Sylvester, David Blaauw, "The Phoenix Processor: A 30pW Platform for Sensor Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*, June 2008

227. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Modeling Crosstalk in Statistical Static Timing Analysis", ACM/IEEE Design Automation Conference (DAC), June 2008
228. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Leakage Power Reduction Using Stress-Enhanced Layouts," ACM/IEEE Design Automation Conference (DAC), June 2008
229. Vineeth Veetil, Dennis Sylvester, David Blaauw, "Efficient Monte Carlo based Incremental Statistical Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2008
230. Yu-Shiang Lin, Scott Hanson, Fabio Albano, Carlos Tokunaga, Razi-UI Haque, Kensall Wise, Ann Marie Sastry, David Blaauw, Dennis Sylvester, "Low-Voltage Circuit Design for Widespread Sensing Applications," IEEE International Symposium on Circuits and Systems (ISCAS), May 2008
231. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Stress Aware Layout Optimization", ACM/IEEE International Symposium on Physical Design (ISPD), April 2008
232. Eric Karl, David Blaauw, Dennis Sylvester, "Analysis of System-Level Reliability Factors and Implications on Real-time Monitoring Methods for Oxide Breakdown Device Failures," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2008
233. Brian Cline, Kaviraj Chopra, David Blaauw, Andres Torres, Savithri Sundareswaran, "Transistor-Specific Delay Modeling for SSTA," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2008
234. Eric Karl, Prashant Singh, David Blaauw, Dennis Sylvester, "Compact in situ Sensors for Monitoring NBTI and Oxide Degradation," IEEE International Solid-State Circuits Conference (ISSCC), February 2008
235. David Blaauw, Sudherssen Kalaiselvan, Kevin Lai, Wei-Hsiang Ma, Sanjay Pant, Carlos Tokunaga, Shidhartha Das, David Bull, "RazorII: In-Situ Error Detection and Correction for PVT and SER tolerance," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2008
236. Sanjay Pant, David Blaauw, "A Charge-Injection Based Active Decoupling Technique for Inductive Supply Noise Suppression," IEEE International Solid-State Circuits Conference (ISSCC), February 2008
237. Gregory Chen, David Blaauw, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, "Yield-driven Near-threshold SRAM Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
238. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Murat Becer, "Victim Alignment in Cross-talk Aware Timing Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
239. Vivek Joshi, David Blaauw, Dennis Sylvester, "Soft-edge Flip-flops for Improved Timing Yield: Design and Optimization," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
240. Ronald G. Dreslinski, Bo Zhai, Trevor Mudge, David Blaauw, Dennis Sylvester, "An Energy Efficient Parallel Architecture Using Near Threshold Operation," Parallel Architectures and Compilation Techniques (PACT), September 2007
241. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A sub-pW timer using gate leakage for ultra low power sub-Hz monitoring systems," IEEE Custom Integrated Circuits Conference (CICC), September 2007

242. Jae-sun Seo, Dennis Sylvester, David Blaauw, Himanshu Kaul, Ram Krishnamurthy, "A Robust Edge Encoding Technique for Energy-Efficient Multi-Cycle Interconnect," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
243. Bo Zhai, Ronald G. Dreslinski, Trevor Mudge, David Blaauw, Dennis Sylvester, "Energy Efficient Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007, **Best Paper Nomination**
244. Scott Hanson, Bo Zhai, Mingoo Seok, Brian Cline, Kevin Zhou, Meghna Singhal, Michael Minuth, Javin Olson, Leyla Nazhandali, Todd Austin, Dennis Sylvester, David Blaauw, "Performance and variability optimization strategies in a sub-200mV, 3.5pJ/inst, 11nW subthreshold processor," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*, June 2007
245. Mingoo Seok, Scott Hanson, Dennis Sylvester, David Blaauw, "Analysis and Optimization of Sleep modes in Subthreshold Circuit Design," ACM/Design Automation Conference (DAC), June 2007
246. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester, Murat Becer, "Top-k Aggressors Sets in Delay Noise Analysis," ACM/IEEE Design Automation Conference (DAC), June 2007
247. Scott Hanson, Mingoo Seok, Dennis Sylvester, David Blaauw, "Nanometer Device Scaling in Sub-threshold Circuits," ACM/Design Automation Conference (DAC), June 2007
248. Mini Nanua, David Blaauw, "Investigating Crosstalk in Sub-Threshold Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
249. Jae-Sun Seo, Prashant Signh, Dennis Sylvester, David Blaauw, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007, **Best Paper Nomination**
250. Bo Zhai, David Blaauw, Dennis Sylvester, Scott Hanson, "A sub-200mV 6T SRAM in 130nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *Special Issue on the 2008 Compound Semi-Conductor Integrated Circuit Symposium (CSICS'08)*, February 2007
251. Carlos Tokunaga, David Blaauw, Trevor Mudge, "A True Random Number Generator with a Meta-stability-Based Quality Control," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *Special Issue on the 2007 IEEE International Solid-State Circuits Conference (ISSCC)*, February 2007
252. Brian Cline, Kaviraj Chopra, David Blaauw and Yu Cao, "Analysis and Modeling of CD Variation for Statistical Static Timing," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
253. Sarvesh Kulkarni, Dennis Sylvester and David Blaauw "A Statistical Approach to Body Bias Clustering for Post-Silicon Tuning," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
254. Rajeev Rao, David Blaauw and Dennis Sylvester, "Soft Error Reduction in Combinational Logic Using Gate Resizing and Flip-flop Selection," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
255. Kaviraj Chopra, Bo Zhai, David Blaauw and Dennis Sylvester, "A New Statistical Max Operation for Propagating Skewness Statistical Timing Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006

256. Sanjay Pant, David Blaauw, "An Active Decoupling Capacitance Circuit for Inductive Noise Suppression in Power Supply Networks," IEEE International Conference on Computer Design (ICCD), October 2006
257. Scott Hanson, Dennis Sylvester, David Blaauw, "A New Technique for Jointly Optimization Gate Sizing and Supply Voltage in Ultra-Low Energy Circuits," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
258. Eric Karl, David Blaauw, Dennis Sylvester, Trevor Mudge, "Reliability Modeling and Management in Dynamic Microprocessor-Based Systems," ACM/IEEE Design Automation Conference (DAC), July 2006
259. Bo Zhai, Leyla Nazhandali, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Sanjay Pant, David Blaauw, Todd Austin, "A 2.60pJ/Inst. Subthreshold Sensor Processor for Optimal Energy Efficiency," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2006
260. Vivek Joshi, Rajevee Rao, Dennis Sylvester, David Blaauw, "Logic SER Reduction through Flip-flop Redesign," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2006
261. Rajevee Rao, Kaviraj Chopra, David Blaauw, Dennis Sylvester, "An Efficient Static Algorithm for Soft Error Rate Analysis of Combinational Circuits," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2006
262. Sanjay Pant, David Blaauw, "Timing-Aware Decoupling Capacitance Allocation in Power Distribution Networks," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2006
263. Saumil Shah, Ashish Srivastava, Dushyant Sharma, Dennis Sylvester, David Blaauw, Vladimir Zolotov, "Discrete Vt Assignment and Gate Sizing Using a Self-Snapping Continuous Formulation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
264. Kavi Chopra, Saumil Shah, Ashish Srivastava, David Blaauw Dennis Sylvester, "Parametric Yield Maximization using Gate Sizing based on Efficient Statistical Power and Delay Gradient Computation," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
265. Amit Jain, Vladimir Zolotov, David Blaauw, "Accurate Delay Computation for Noisy Waveform Shapes," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
266. Sanjay Pant, David Blaauw, "Static Timing Analysis Considering Power Supply Variations," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2005
267. Leyla Nazhandali, Michael Minuth, Bo Zhai, Javin Olson, Scott Hanson, Todd Austin, David Blaauw, "A Second-Generation Sensor Network Processor with Application-Driven Memory Optimizations and Out-of-Order Execution," ACM/IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), September 2005.
268. Bo Zhai, Scott Hanson, David Blaauw, Dennis Sylvester, "Analysis and Mitigation of Variability in Subthreshold Design," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2005
269. Shidhartha Das, Sanjay Pant, David Roberts, Seokwoo Lee, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, "A Self-Tuning DVS Processor Using Delay-Error Detection and Correction," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *Special Issue on the 2005 Symposium on VLSI Circuits*, June 2005

270. Leyla Nazhandali, Anna Reeves, Michael Minuth, Ryan Helfand, Javin Olson, Bo Zhai, Sanjay Pant, Todd Austin, David Blaauw, "Energy Optimization of Subthreshold Voltage Sensor Processors," International Symposium on Computer Architecture (ISCA), June 2005
271. Ashish Agarwal, Saulim Shah, Dennis Sylvester, David Blaauw, "Accurate and Efficient Gate-Level Parametric Yield Estimation Considering Power/Performance Correlation", ACM/IEEE Design Automation Conference (DAC), June 2005
272. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Circuit Optimization using Statistical Static Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2005
273. David Blaauw, Kaviraj Chopra, "CAD Tools for Variation Tolerance," ACM/IEEE Design Automation Conference (DAC), June 2005
274. Eric Karl, Dennis Sylvester, David Blaauw, "Timing Error Correction Techniques for Voltage-Scalable On-Chip Memories," IEEE International Symposium on Circuits and Systems (ISCAS), May 2005
275. Amit Jain, David Blaauw, "Slack Borrowing in Flip-Flop Based Sequential Circuits," ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), April 2005
276. Rajeev Rao, David Blaauw, Dennis Sylvester, Charles Alpert, Sani Nassif, "An Efficient Surface-Based Low-Power Buffer Insertion Algorithm," ACM/IEEE International Symposium on Physical Design (ISPD), April 2005
277. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Statistical Timing Based Optimization Using Gate Sizing," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2005
278. Himanshu Kaul, Dennis Sylvester, David Blaauw, Trevor Mudge, Todd Austin, "DVS for On-Chip Designs Based on Timing Error Correction," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2005
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25. Smitha Shyam, Sujay Phadke, Benjamin Lui, Hitesh Gupta, Valeria Bertacco, David Blaauw, "VOLTaiRE: Low-cost Fault Detection Solutions for VLIW Microprocessors," Workshop on Intropective Architecture (WISA), February 2006.
26. Amir Born, Christopher Proglor, David Blaauw, "Correlation Analysis of CD-Variation and Circuit Performance Under Multiple Sources of Variability," SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, May 2005

27. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Statistical Timing Based Optimization Using Gate Sizing," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005
28. Amit Jain, David Blaauw, Vladimir Zolotov, "Accurate Gate Delay Model for Arbitrary Waveform Shapes," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005
29. Christopher Proglor, Amir Borna, David Blaauw, Pierre Sixt, "Impact of lithography variability on statistical timing behavior," SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, Ed., Vol. 5379, May 2004, pg. 101-110
30. Amit Jain, David Blaauw, "Modeling Flip-Flop Delay Dependencies in Timing Analysis," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2004
31. Aseem Agarwal, David Blaauw, Vladimir Zolotov, Sarma Vrudhula, "Statistical Timing Analysis Using Bounds and Selective Enumeration," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 29-36
32. Aseem Agarwal, David Blaauw, Savithri Sundareswaran, Vladimir Zolotov, Min Zhou, Kaushik Gala, Rajendran Panda, "Path-Based Statistical Timing Analysis Considering Inter- and Intra-Die Correlations," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 16-21
33. Himanshu Kaul, Dennis Sylvester, David Blaauw, "Active Shielding of RLC Global Interconnects," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 98-104
34. Kanak Agarwal, Dennis Sylvester, David Blaauw, "A Library Compatible Driving Point Model for On-Chip RLC Interconnects," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 63-69
35. Bhavana Thudi, David Blaauw, "Efficient Switching Window Computation For Cross-Talk Noise," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 84-91
36. Fadi Aloul, Soha Hassoun, Karem Sakallah, David Blaauw, "Robust SAT-Based Search Algorithm for Leakage Power Reduction," IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), September 2002, pg. 167-177
37. Murat Becer, David Blaauw, Ibrahim Hajj, Rajendran Panda, "Early Probabilistic Noise Estimation for Capacitively Coupled Interconnects," ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP), April 2002, pg. 77-83
38. David Blaauw, "Signal Integrity Issues in High Performance Design," IEEE International Workshop - Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
39. Vladimir Zolotov, David Blaauw, Rajendran Panda, Chanhee Oh, Savithri Sundareswaran, "Slope Propagation in Static Timing Analysis," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 91-96
40. Supamas Sirichotiyakul, David Blaauw, Chanhee Oh, Rafi Levy, Vladimir Zolotov, "Driver Modeling and Alignment for Worst-Case Delay Noise," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 1-7
41. David Blaauw, Tim Edwards, "Generating False Path Free Timing Graphs Using Node Splitting," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), March 1999, pg. 112-117
42. David Blaauw, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2

43. Daksh Lenther, Satya Pullela, David Blaauw, Shantanu Ganguly, "Hierarchical Clock-network Optimization," ACM Physical Design Workshop, April 1996, pg. 49-54
44. John Willis, Rob Newshutz, Lance Thompson, Jeff Graves, Tom Dillinger, Jeff Snyder, Nimish Raddia, Joe Skovira, David Blaauw, Sidhartha Mohanty, Zhiyuan Li, Sandra Samelson, Matt Lin, "MinSim: Optimized, Compiled VHDL Simulation Using Networked & Parallel Computers," IEEE VHDL International User Forum, October 1993, pg. 137-144

G. Patents Issued

1. "Variation-tolerant voltage reference," Patent number 10310537, issued June 4, 2019
2. "Intraocular pressure sensor with improved voltage reference circuit," Patent number 10,285,590, issued May 14, 2019
3. "Self-oscillating switched-capacitor DC-DC converter," Patent number 9,979,284, issued May 22, 2018
4. "Floating-gate transistor array for performing weighted sum computation," Patent number 9,760,533, issued September 12, 2017
5. "Electrostatic discharge clamp circuit for ultra-low power applications," Patent number 9,716,381, issued July 25, 2017
6. "Measurement circuitry and method for measuring a clock node to output node delay of a flip-flop," Patent number 9,638,752, issued May 2, 2017
7. "Ultra Low Power Temperature Insensitive Current Source With Line and Load Regulation," Patent Number 9,639,107, issued May 2, 2017
8. "Protocol for an electronic device to receive a data packet from an external device," Patent number 9,635,147, issued April 25, 2017
9. "Integrated circuit using topology configurations," Patent Number 9,589,601 issued March 7, 2017
10. "Single Cycle Arbitration Within an Interconnect," Patent Number 9,514,074 B2 issued December 6, 2016
11. "Error recovery within integrated circuit," Patent Number 9,448,875, issued September 20, 2016
12. "Storage Device Supporting Logical Operations, Methods and Storage Medium," Patent Number 9,396,795, issued July 19, 2016.
13. "Low Power Oscillator with Charge Subtraction Scheme," Patent Number 9,385,692, July 5, 2016
14. "True random number generator," Patent Number 9,335,972, May 10, 2016
15. "Memory Circuit Including Read Voltage Boost," Patent Number 9,275,702 issued March 1, 2016
16. "Error Recovery Within Integrated Circuit," Patent Number 9,164,842 issued October 20, 2015
17. "Low Power Reference Current Generator with Tunable Temperature," Patent Number 9,147,443 issued September 29, 2015
18. "Randomized Value Generation," Patent Number 8,930,427 issued January 6, 2015
19. "Crossbar circuitry for applying an adaptive priority scheme," Patent Number 8,868,817 issued October 21, 2014
20. "Apparatus and Method for Transferring a Data Signal Propagated Along a Bidirectional Communication Path Within a Data Processing Apparatus," Patent Number 8,713,232 issued April 29, 2014

21. "Error Recovery Within Integrated Circuit" Patent Number 8,650,470 issued February 11, 2014
22. "Reference voltage generator having a two transistor design," Patent Number 8,564,275 issued October 22, 2013
23. "Crossbar circuitry for applying an adaptive priority scheme and method of operation of such crossbar circuitry," Patent Number 8,549,207 issued October 1, 2013
24. "Integrated circuit memory power supply," Patent Number 8,526,261 issued September 3, 2013
25. "Vertical interconnect patterns in multi-layer integrated circuits," Patent Number 8,381,155 issued February 19, 2013
26. "Random Number Generator," Patent Number 8,346,832 issued January 1, 2013
27. "Cache memory system for a data processing apparatus," Patent Number 8,335,122 issued December 18, 2012
28. "Stalling synchronization circuits in response to a late data signal," Patent Number 8,276,014 issued September 25, 2012
29. "Crossbar circuitry for applying a pre-selection prior to arbitration between transmission requests and method of operation of such crossbar circuitry," Patent Number 8,255,610, issued August 28, 2012
30. "Crossbar circuitry and method of operation of such crossbar," Patent Number 8,230,152, issued July 24, 2012
31. "Single Event Upset Error Detection Within an Integrated Circuit," Patent Number 8,185,812, issued May 22, 2012
32. "Error Recovery Within Processing Stages of an Integrated Circuit," Patent Number 8,185,786, issued May 22, 2012
33. "Memory Cell Structure, a Memory Device Employing Such a Memo," Patent Number 8,107,290, issued January 31, 2012
34. "Crossbar Circuitry and Method of Operation of Such Crossbar" Patent Number 8,108,585, issued on January 31, 2012
35. "Error Detection in Precharged Logic," Patent Number 8,103,922, issued on January 24, 2012
36. "Error Detection in Precharged Logic," Patent Number 8,006,147, issued on August 23, 2011
37. "Isolation Circuitry and Method for Hiding a Power Consumption Characteristic of an Associated Processing Circuit," Patent Number 7,880,339, issued on February 1, 2011
38. "Integrated Circuit Memory Access Mechanisms," Patent Number 7,864,562, issued on January 4, 2011
39. "On-chip Power Supply Voltage Regulation," Patent Number 7,839,129, issued on November 23, 2010
40. "Integrated Circuit with Error Correction Mechanisms to Offset Narrow Tolerancing," Patent Number 7,701,204, issued on April 20, 2010
41. "Error Detection and Recovery Within Processing Stages of an Integrated Circuit," Patent Number 7,650,551, issued on January 19, 2010
42. "Data Processor Memory Circuit," Patent Number 7,533, 226, issued on May 12, 2009
43. "Systematic and Random Error Detection and Recovery Within Processing Stages of An Integrated Circuit," Patent Number 7,337,356, issued on February 26, 2008

44. "Error Recovery Within Processing Stages of an Integrated Circuit," Patent Number 7,320,091, issued on January 15, 2008
45. "Data Retention Latch Provision Within Integrated Circuits," Patent Number 7,310,755, issued on December 18, 2007
46. "Error detection and recovery within processing stages of an integrated circuit," Patent Number 7,278,080, issued on October 2, 2007
47. "Address Decoding," Patent Number 7,263,015, issued on August 28, 2007
48. "Systematic and random error detection and recovery within processing stages of an integrated circuit," Patent Number 7,162,661, issued on January 9, 2007
49. "Methods for analyzing integrated circuits and apparatus therefor," Patent Number 7,149,674, issued on December 12, 2006
50. "Noise analysis for an integrated circuit model," Patent Number 7,093,223, issued on August 15, 2006
51. "Memory System having Fast and Slow Data Reading Mechanisms," Patent Number 7,072,229, issued on July 4, 2006
52. "Data Processor Memory Circuit," Patent Number 7,055,007, issued on May 30, 2006
53. "Memory System Having Fast and Slow Data Reading Mechanisms," Patent Number 6,944,067, issued on September 13, 2005
54. "Actively-Shielded Signal Wires," Patent Number 6,919,619, issued on July 19, 2005
55. "Method and Apparatus for Controlling Current Demand in an Integrated Circuit", Patent Number 6,819,538, issued on November 16, 2004
56. "Cross Coupling Delay Characterization for Integrated Circuits," Patent Number 6,799,153, issued on September 28, 2004
57. "Iterative, Noise-Sensitive Method of Routing Semiconductor Nets," Patent Number 6,480,998, issued on November 12, 2002
58. "Waveform Manipulation in Time Warp Simulation," Patent Number 6,195,628, issued on February 27, 2001
59. "Optimizing Combinational Circuit Layout through Iterative Restructuring," Patent Number 6,074,429, issued on June 13, 2000
60. "In-Transit Message Detection for Global Virtual Time Calculation in Parallel Time Warp Simulation," Patent Number 5,956,261, issued on September 21, 1999
61. "Method for Optimizing Element Sizes in a Semiconductor Device," Patent Number 5,903,471, issued on May 11, 1999
62. "Updating Hierarchical DAG Representations through a Bottom up Method," Patent Number 5,790,416, issued on August 4, 1998
63. "Complementary Network Reduction for Load Modeling," Patent Number 5,790,415, issued on August 4, 1998
64. "Simulation Corrected Sensitivity," Patent Number 5,787,008, issued on July 28, 1998
65. "Accurate Delay Prediction Based on Multi-Model Analysis," Patent Number 5,751,593, issued on May 12, 1998
66. "Apparatus and Method for the Automatic Determination of a Standard Library Height within an Integrated Circuit Design," Patent Number 5,737,236, issued April 7, 1998

67. "Integrated Circuit Design and Manufacturing Method and an Apparatus for Designing an Integrated Circuit in Accordance with the Method," Patent Number 5,689,432, issued on November 18, 1997
68. "Method and Apparatus for Designing an Integrated Circuit," Patent Number 5,666,288, issued on September 9, 1997
69. "Logic Gate Size Optimization Process for an Integrated Circuit Whereby Circuit Speed is Improved While Circuit Areas is Optimized," Patent Number 5,619,418, issued on April 8, 1997
70. "Message Sequence Number Control in a Virtual Time System," Patent Number 5,617,561, issued on April 1, 1997

VI Scholarly Addresses

A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, “The Internet of Tiny Things - IoT²: Challenges and Opportunities in mm-Scale Computing,” ECE Distinguished Lecture Series, George Washington University, December 2018
2. Plenary Keynote Address, “Unlocking New IoT Application Domains Through Ultra-Low Power mm-Scale Sensor Node Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2018
3. Invited presentation, “Low-Power Circuit Techniques for IoT Energy Harvesting,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2016
4. Plenary Keynote Address, “From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design,” IEEE Subthreshold Microelectronics Conference (SubVt), October 2012
5. Invited presentation, “Adaptive Sensing and Design for Reliability,” IEEE International Reliability Physics Symposium, May 2010
6. Invited presentation, “Architectural Techniques for Self-Adaptive Computing,” IEEE International Solid-State Circuits Conference (ISSCC), February 2007
7. Invited presentation, “Energy Optimality and Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
8. Invited presentation, “Energy Efficient Design for Subthreshold Supply Voltage Operation,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
9. Invited presentation, “Extended Dynamic Voltage Scaling for Low Power Design,” IEEE International SOC Conference, September 2004
10. Invited presentation, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001
11. Invited presentation, “Inductance 101: Analysis and Design,” ACM/IEEE Design Automation Conference, June 2001
12. Invited presentation, “Inductance Extraction and Modeling,” ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
13. Keynote address, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
14. Keynote address, “Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

VII Professional Activities

A. Professional Societies

- Fellow of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design and Test of Computers*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems (T-VLSI)*, special issue on Low Power Electronics, 1999

C. Conference and Workshop Organization

- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2018 - current
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006 – 2009
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004 - 2007
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999 - 2006
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997, 2005 – 2006
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002 - 2004
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2003
- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2002
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

D. Consulting & Advisory Boards

- **Technical Consulting and Advisory boards**
 - Member of University of Illinois at Urbana – Champaign Advisory Panel 2013 – current

- Gear Inc. 2013 – 2015
- Apache Design Automation – member of advisory board
- Nascentric, Technical Consulting, 2008
- CLK Design Automation (CLK-DA), Technical Consulting, 2005 – 2008
- **Legal Consulting**
 - Parkins Coie LLP, 2014 – 2015
 - WilmerHale, 2012 – 2013
 - Alston & Bird, 2010 – 2011
 - Weil, Gotshal & Manges, 2008 – 2010
 - WilmerHale, 2007
- F. Refereeing and Reviewing**
 - NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)
 - IEEE , IEEE T-VLSI, ACM TODAES, IEEE D&T
 - DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS