A Pressure Sensing System with ± 0.75 mmHg (3 σ) Inaccuracy for Battery-Powered Low Power IoT applications

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Abstract

This work presents an energy-efficient piezoresistive pressure sensing system for low-power IoT applications. The sensor adopts duty-cycling and sub-ranging to achieve high energy efficiency and accuracy. Fabricated in 180nm CMOS, the test chip with pressure transducer achieves state-of-art energy efficiency of 6.1 nJ•mmHg² with ± 0.75 mmHg 3 σ inaccuracy. The sensor is integrated into a wireless sensor node to demonstrate its operation at a system level.

Introduction

Pressure sensing is a common sensing modality and uses different types of sensors: capacitive, piezoresistive and piezoelectric. Piezoresistive sensors have been the most widely used due to their low cost and durability. However, they need to be powered, which is a significant disadvantage compared to other types of sensors. This is especially critical for IoT systems with a small form factor as the bridge resistance decreases with sensor size (1–10 k Ω), increasing power consumption. This problem is further exacerbated by the high internal resistance of small IoT batteries, making it impractical to directly drive the bridge from the battery. Recently, duty-cycled excitation of the bridge was proposed, where the bridge output is sampled to reduce overall current consumption compared to DC excitation [1-3]. Furthermore, [2] also samples the bridge excitation voltage and uses it as a reference for the ADC to reduce sensitivity to battery resistance change. Although this approach achieves low power consumption, the ADC directly converts the sampled bridge outputs, limiting its performance as it requires a low noise/high accuracy reference due to the ADC's small LSB ($<200 \mu V$).

This paper presents a highly duty-cycled sub-ranging Wheatstone Bridge- (WhB)-based pressure sensor for compact IoT systems. It amplifies the sampled bridge outputs and uses a ratiometric offset shift to enable sub-ranging followed by an ADC operation. The ratiometric offset shift and ADC use the sampled excitation voltage driven by an LDO. The LDO adopts an autozeroing technique that enables the use of a low-bandwidth, low-power amplifier. A fully encapsulated system integrating the proposed sensor demonstrates its usage.

Proposed Circuit

Fig. 1 shows the block diagram of the proposed sensor. The signal chain consists of an off-chip WhB followed by a 2-stage switchedcapacitor (SC) amplifier with an offset shift unit and ADC. The sensor uses a reference generator that includes an excitation voltage (V_{EX}) sampler and an LDO consisting of an autozeroing buffer. The LDO references the sampled excitation voltage (VEX SMP), and its output (V_{EX LDO}) is used in the offset shift block and ADC. Due to the bridge sensor's ratiometric nature, conversion based on the ratio of sampled voltages ((V_{INP_SMP}-V_{INN_SMP})/V_{EX_SMP}) provides the same results as DC excitation ((V_{INP}-V_{INN})/V_{EX}) if enough excitation time (t_{EX}) is given for settling. Note that the sensor's sensitivity will degrade if too much t_{EX} is given since V_{EX} will drop as charge is supplied from an on-chip decoupling capacitor (C_{decap}=~1.4 nF) to address the high battery resistance. The sensor allows oversampling as the time constant of C_{decap} voltage recovery is much less than a single conversion time (1 ms). To find the correct sub-range, the offset shift code is adjusted as needed by comparing the conversion result with a preset look-up table after each conversion.

Fig. 2. shows a detailed schematic of a 2-stage SC amplifier. As the bridge is only excited for a short period of time ($t_{EX} \le 400$ ns), a conventional SC amplifier structure requires either a power hungry, high bandwidth (≥ 17.5 MHz for 10b accuracy) amplifier or a V_{CM} reference for sampling input voltages. To avoid these, we isolate the input sampling from the amplifier. Initially, charges on the sampling capacitors (C_{S}) are purged by shorting them to V_{CM} . Then, when the bridge is excited, the bottom plates are connected to the bridge while

the top plates are shorted together. This allows the top plate to passively settle to the common mode of the input, eliminating the need for a high-speed amplifier/voltage reference. Note that this approach still provides parasitic-insensitive operation as the charge on the top plate is conserved. The $1^{\rm st}$ stage amplifier dominates the overall noise performance and uses C_S of 7.5 pF to achieve a KT/C noise <0.3 mmHg. An autozeroing capacitor ($C_{\rm OS}$) removes the amplifier's offset and 1/f noise. To mitigate the effect of amplifier noise folding, $C_{\rm OS}$ is increased to 22.5 pF, limiting the amplifier bandwidth during offset sampling [4]. The bridge resistance and C_S set the minimum settling time, which is designed to be configurable (150-900 ns in simulation, 400 ns typical) to ensure 12b accuracy across process variation.

Offset in the reference generator creates pressure error with varying battery voltage while its 1/f noise creates long-term stability issues. The reference generator employs autozeroing to mitigate these issues. To store the correct offset voltage, a high-power, high-bandwidth amplifier is typically required for output $V_{\rm EX_LDO}$ to track input ($V_{\rm EX}$) in the offset sampling phase (i.e. during tex). Instead, we propose a scheme that delays the offset sampling phase and samples the offset after $V_{\rm EX_LDO}$ is stabilized (Fig. 3). Initially, the offset storing capacitor ($C_{\rm AZ}$) is shorted to $V_{\rm EX_SMP}$ following $V_{\rm EX}$ during excitation. $C_{\rm AZ}$ remains shorted after sampling until $V_{\rm EX_LDO}$ is fully stabilized. The following phase samples and cancels the offset. Note that this process involves charge sharing between $C_{\rm S,LDO}$ and $C_{\rm AZ}$. As a result, the amount of offset reduction is set by the ratio of $C_{\rm S,LDO}$ to $C_{\rm AZ}$. This work uses 15 pF of $C_{\rm S,LDO}$ to set KT/C noise < 0.25 mmHg and uses 1.5 pF of $C_{\rm AZ}$, resulting in a 10× offset reduction.

Unlike the 1st stage, the 2^{nd} stage is not noise limited, making it a better place for the offset shift block (Fig. 4). It generates offset using a capacitive DAC and does so in a manner that is ratiometric with the reference voltage, $V_{\rm EX_LDO}$. At the start of conversion, the offset shift DAC is floating, waiting for $V_{\rm EX_LDO}$ to stabilize. Once $V_{\rm EX_LDO}$ stabilizes, its switches are configured based on a given offset code to store charge that is proportional to $V_{\rm EX_LDO}$. Then, redistribution occurs with the switches connected to $V_{\rm EX_LDO}$ or GND for a positive or negative shift, respectively. As a result, a fraction of $V_{\rm EX_LDO}$ is stored on the MSB capacitor for the offset shift. This work uses a 6b DAC with 40 fF unit capacitance to enable a minimum sub-ranging window of 200 mmHg in 0–900 mmHg pressure range. The 2^{nd} stage is capable of gain adjustment (18–49×) to accommodate bridge sensitivity variation. The following 10b SAR ADC digitizes the amplifier output with respect to $V_{\rm EX_LDO}$ to complete the ratiometric conversion.

Measurements

The proposed sensor was fabricated in 180nm CMOS and tested with a WhB pressure transducer. The sub-ranging window size was 300 mmHg with three ranges covering 0-900 mmHg. The sensor core operates from a battery voltage of 3.6–4.2 V, while the digital blocks operate at 1.2 V to save power. The sensor consumes $8.5~\mu W$ and achieves $0.3 \text{ mmHg} (1\sigma)$ resolution with an 8 ms conversion time. Fig. 5 shows the measured resolution vs. OSR. The resolution is initially thermal noise limited and eventually hits its flicker noise floor (< 0.04 mmHg). The measured average supply sensitivity is 0.49mmHg/V for 3.6–4.2 V (Fig. 6). The sensor shows stable operation over a long time (>100 days) without drift. Measured 3σ pressure sensor accuracy (24 chips) is -1.05/+2.65 mmHg after 2-pt calibration. The calibration was performed at only two points (300, 600 mmHg) to find the slope and 3 offset codes for each sub-range. After further removing systematic nonlinearity, 3σ accuracy improves to ± 0.75 mmHg. The sensor was integrated in a fully encapsulated system, which is fully functional. Table 1 compares the sensor performance with other µW piezoresistive sensors. Unlike prior arts, this work provides sensor accuracy in pressure across multiple samples with a pressure transducer.

