

Sample and Average Common-Mode Feedback in a 101 nW Acoustic Amplifier

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Abstract

We present a Sample and Average Feedback Resistor (SAFR) for accurate and programmable common-mode feedback in capacitively coupled low-power amplifiers. Using only switches, clocks, and capacitors, we reduce the variation across process and temperature by 4.4x and 226x, respectively, compared to a traditional pseudo-resistor implementation. The SAFR was implemented in a low-power audio LNA + PGA + ADC chain, achieving a resistance of 100 TΩ and HP corner programmability from 16 mHz to 4 Hz.

Introduction

Low-power medical and acoustic applications often use a capacitive-coupled amplifier (Fig. 1) with a common-mode feedback resistor. A high resistance, up to tens of TΩ, is often required to ensure a sufficiently low high-pass (HP) corner for these low-bandwidth applications and to reduce the in-band noise contribution of the resistor itself. To achieve such a high resistance, a *pseudo-resistor* [1, 2] is frequently used. However, prior pseudo-resistor configurations commonly suffer from high variation across temperature and process [3]. Efforts to address this issue include a variation-compensated design [4], duty-cycled resistor(s) [4,5], and a Gm-C DC servo loop [6]. However, these methods require either accurate pulse-width control or accurate on-chip current trimming. Furthermore, they produce only tens to hundreds of GΩ. A capacitive ladder, proposed in [8], attenuates the output; however, this also increases the output offset by the same factor. It further adds an explicit common-mode voltage source.

We present a Sample & Average Feedback Resistor (SAFR) that accurately controls the HP corner across temperature and corners with the added benefit of corner frequency programmability. The SAFR uses two stages of switches and capacitors to implement a low-pass filter in series with a switched-capacitor resistor and achieves a resistance of 100 TΩ in a 180nm CMOS implementation.

Proposed Architecture

The proposed SAFR concept consists of two stages: a low-pass pre-filtering stage followed by a switched-capacitor resistor (Fig. 1). The first switch, S_1 , samples the output on capacitor C_A in phase S_1 . This voltage is then accumulated on capacitor C_B in phase S_{1B} . The clock phases are non-overlapping with approximately 50% duty cycle, and frequency f_s is set several times higher than the signal bandwidth, allowing any injected tones to be filtered out. The first stage stores a low-pass-filtered version of the required input common-mode voltage on C_B . The first stage low-pass corner can be tuned with f_s and is set to 1.7 Hz in this work ($C_B = 9.8$ pF).

The second stage is a switched-capacitor resistor that passes the common-mode voltage from C_B to the amplifier input, thereby establishing the required input common mode. The corner frequency is determined by the switched-capacitor resistance ($R = 1/f_{fb}C_C$). The switch between capacitor C_C and the amplifier input is closed briefly (~ 100 ns) so as to not disturb the amplifier, and this duration (i.e., duty cycle) does not need to be accurately controlled. The key to obtaining a very low HP corner is to use a very low feedback frequency, f_{fb} , along with a very small capacitance, C_C . The demonstrated system uses $f_{fb} = 1.33$ Hz and $C_C = 6.2$ fF, yielding a resistance of ~ 100 TΩ. The value of the HP corner can be derived to the first order as $f_{hp} = (f_{fb}C_C)/(2\pi C_F)$ and depends only on frequency and capacitance. Since the capacitance ratio is relatively process- and temperature-invariant, and the frequency can be typically obtained from accurate sources already in the system (e.g., the ADC clock in this work), the corner is precisely controlled. Furthermore, the corner frequency can be easily and quickly programmed by changing f_{fb} . For instance, the amplifier can start up quickly using a value of f_{fb} (fast settling mode), after which f_{fb} shifts to a lower, final value. Finally, if the bandwidth of the amplifier is lowered at run time (e.g., in a low-power mode [7]), the f_s can be lowered proportionally since it doesn't set the corner (unlike in [8] where it must

remain fixed to maintain a constant corner).

Circuit Implementation

The overall architecture (Fig. 2) consists of a low-noise amplifier (LNA) followed by a programmable gain amplifier (PGA). The LNA OTA uses an inverter-based cascode topology. The output common mode is shifted by auxiliary amplifiers in the DC-servo loops to an optimal bias point for each PMOS/NMOS input pair to maximize the output range. The gain G of these gm-gm auxiliary amplifiers combines with the pre-filtering stage of the SAFR, resulting in a modified first-order corner of $f_{hp} = (f_{fb}C_C G)/(2\pi C_F)$. The use of transmission gates reduces the clock feedthrough. Since the voltage at the amplifier input is relatively stable, the impact from non-linearity of the switches is negligible. The low-pass filter in the feedback path results in a second-order transfer function from input to output. Hence, for high f_{fb} , the system shows second-order features such as peaking at the HP corner. However, in the intended applications, f_{fb} is sufficiently low (well below the signal bandwidth) to closely approximate the first-order system of the pseudo-resistor.

The SAFR trades off power consumption due to clock generation (62 nW in this work) to achieve much better control than pseudo-resistor solutions. However, clock generation can be amortized over multiple feedback loops (in this case the LNA and PGA), lowering overhead. In addition, the SAFR entails a minor trade-off in the dynamic range. Since the first stage is a low-pass filter, the voltage on C_B contains the same frequencies as the amplifier output, although strongly attenuated. For tones that are a multiple of f_{fb} , constant-phase sampling of C_B by C_C has a slight bias that results in a small mismatch at the amplifier input pair. This manifests as a DC output offset, which reduces the output dynamic range and slightly worsens THD as compared to a pseudo-resistor topology. Based on simulation, this issue can be addressed by increasing C_B and/or with a Delta Sigma modulator to break any harmonic pattern.

Measurements

The SAFR was implemented in a low-power 180nm CMOS audio amplifier chain (similar to [7]) consisting of an LNA and PGA with 10.2 kHz and 500 Hz bandwidth, respectively, and an ADC and MEMS microphone. Fig. 3 shows the measured LNA transfer curves from -40°C to 80°C for the SAFR and a pseudo-resistor implementation with matching HP corners. The SAFR shows total $1.2\times$ variation across temperature as compared to $271\times$ for the pseudo-resistor. Fig. 4 shows the programmability of the corner from 16 mHz to 4 Hz by changing f_{fb} . Fig. 5 presents the measured noise of the SAFR and a pseudo-resistor; both are flicker-noise dominated. The 16 kHz f_s tone and harmonics stem from f_s and can be easily filtered out in the antialiasing filter before the ADC. In addition, any attenuated f_s tone and harmonics passed by the filter are aliased into a single bin of the ADC output when the ADC clock is synchronized with f_s .

Fig. 6 shows the measured distribution of the HP corner across 15 chips from one wafer and across 4 chips each from 2 different wafers, demonstrating robust control across process. Fig. 7 shows the measured transfer curve for the entire chain (LNA + PGA) for different gain settings. Fig. 8 demonstrates the fast settling of the LNA, reducing it from ~ 18 s to 110 ms at the initial system startup. The amplifier core power is 70 nW, and clock generation power is 62 nW, shared over 2 amplifiers. The LNA NEF is 2.67 (based on 50% of the clock power since it is shared by the LNA and PGA). Table 1 provides the comparison table. Fig. 9 shows the die micrograph. Overall, the SAFR maintains similar amplifier specifications for noise, harmonic distortion, and performance as the pseudo-resistor version.

References

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- [2]. H. Wang *et al.*, *TCAS II*, 2018.
- [3]. P. Harpe *et al.*, *JSSC*, 2016.
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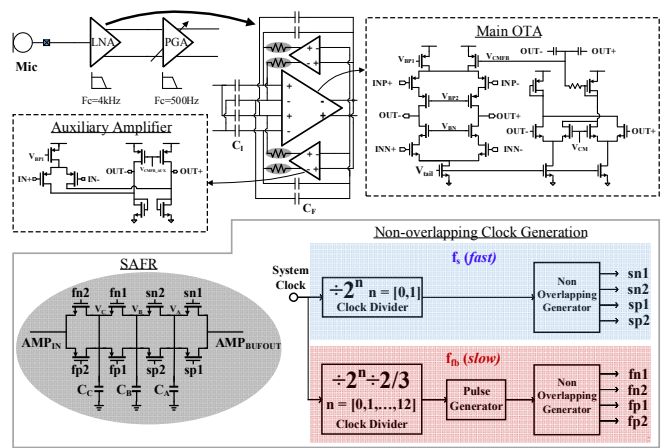
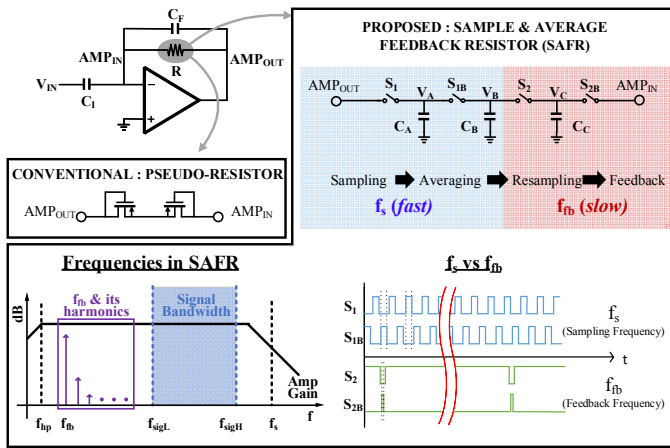


Fig. 1. Continuous-time amplifier with capacitive feedback using Pseudo-resistor and Proposed Sample & Average Feedback Resistor (SAFR) approach.

Fig. 2. Circuit diagram of the Analog Front-end consisting of LNA, PGA, SAFR and switching signal generation circuitry.

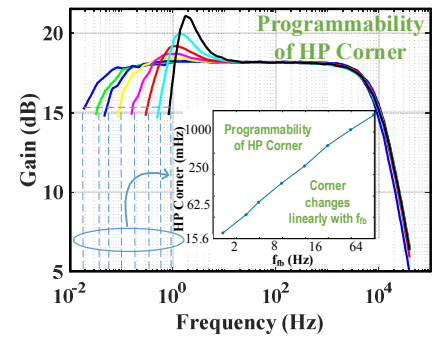
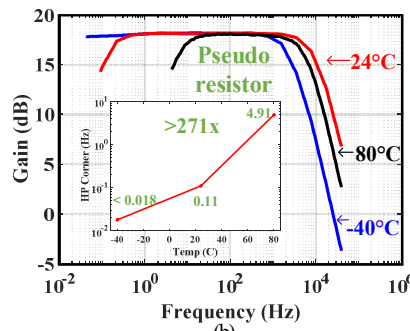
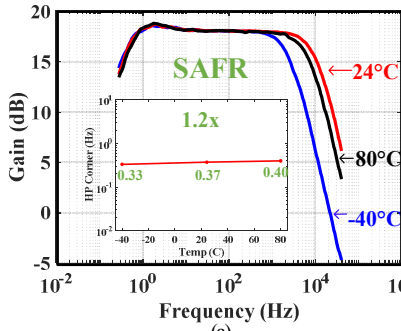
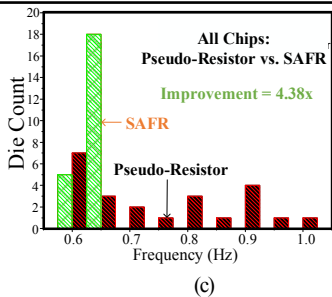
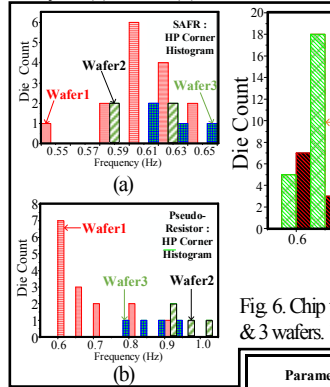
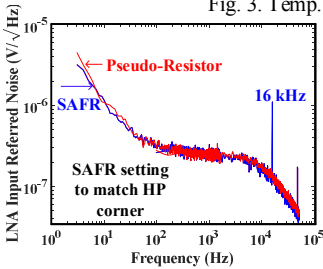


Fig. 3. Temp. Stability of (a) SAFR (b) Pseudo-resistor

Fig. 4. Programmability of HP Corner with SAFR



| Parameter | Wafer1 (15) | Wafer2 (4) | Wafer3 (4) | All (23) |
|----------------------------------|-------------|------------|------------|----------|
| Mean (μ) (Hz) | 0.698 | 0.956 | 0.849 | 0.776 |
| Std. Deviation (σ) (Hz) | 0.091 | * | * | 0.133 |
| σ/μ | 0.130 | * | * | 0.171 |

| Parameter | Wafer1 (15) | Wafer2 (4) | Wafer3 (4) | All (23) |
|----------------------------------|-------------|------------|------------|----------|
| Mean (μ) (Hz) | 0.609 | 0.602 | 0.620 | 0.610 |
| Std. Deviation (σ) (Hz) | 0.025 | * | * | 0.024 |
| σ/μ | 0.041 | * | * | 0.039 |

*Insufficient samples for computing standard deviation
 **The statistical testing was done at 50C to accelerate the testing time for measuring 46 chips. HP Corner of SAFR was matched to pseudo-resistor by changing f_{fb}

Fig. 6. Chip to chip distribution of HP corner for (a) SAFR (b) Pseudo-resistor LNAs across 23 chips (c) & 3 wafers. 15 chips from one wafer, 2 additional wafers have 4 chips each. Variation summarized in (d)

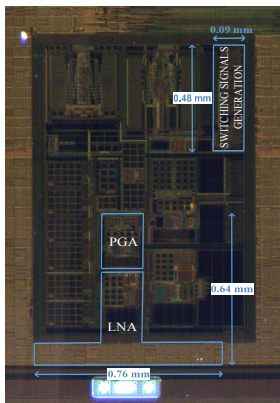
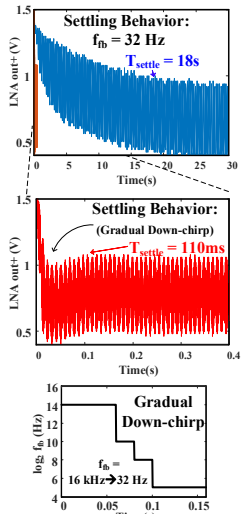
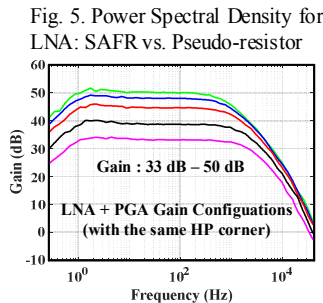


Fig. 9. Die Micrograph

Fig. 8. Settling time for SAFR with 32 Hz (standard operating mode) and with gradual f_{fb} downchip starting with 16kHz

| Parameter | This Work : LNA | | JSSC'19 [3] | ISSCC'17 [5] | ASSCC'14 [6] | ISCAS'14 [8] |
|--|---------------------------------|---------------------------------|-----------------------------|---------------------------------|-------------------------------|---------------------------|
| | SAFR | Pseudo-Resistor | | | | |
| Technology (nm) | 180 | | 180 | 40 | 180 | 180 |
| Application | Acoustic Sensing | | Acoustic Sensing | LFP/AP acquisition | EEG | Biosensors |
| Feedback Technique | | | | | | |
| Feedback Resistor Technique | SAFR | Pseudo-Resistor | DSL | Multi Rate Duty Cycled Resistor | Duty Cycled Gm-C DSL | Switched Capacitor Ladder |
| Effective Resistance | 0.43 - 108 T Ω^* | 15.7 T Ω | 106 G Ω | 90.0 G Ω | 2.65 G Ω | 0.11 - 21.2 T Ω^* |
| HP Corner | 0.016 Hz - 4 Hz* | 0.11 Hz | 1.5 Hz | 0.12 Hz | 0.60 Hz | 0.30 Hz - 60 Hz* |
| HP Corner variation: -40C to 80C | 1.2x | 271x | N/A | N/A | N/A | N/A |
| HP Corner variation: Chip to chip ($\frac{\sigma}{\mu}$) | 0.039 | 0.171 | N/A | N/A | N/A | N/A |
| Amplifier | | | | | | |
| Power | 101 nW** | 70 nW | 1 nW | 2.8 μ W | 4.266 μ W | 1.2 μ W |
| Supply Voltage | 1.4 V | | 0.6 V | 1.2 V | 1.8 V | 1.5 V |
| Input Referred Noise | 26.1 μ Vrms (till 14.6 kHz) | 28.1 μ Vrms (till 14.6 kHz) | 26 μ Vrms (till 370 Hz) | 7.1 μ Vrms (till 5 kHz) | 1.04 μ Vrms (till 100 Hz) | 17.8 μ Vrms*** |
| Bandwidth | 10.2 kHz | | 370 Hz | 5 kHz | 100 Hz | 270 Hz |
| Gain | 18.3 dB | | 32 dB | 25.7 dB | 40 dB | 36.7 dB |
| THD | 400 mVrms (output) < 0.6% | 458 mVrms (output) < 0.6% | N/A | 80 mVpp (input) < 0.015% | N/A | N/A |
| NEF | 2.67 | 2.40 | 2.10 | 4.40, 7.40 | 7.80 | 37.3*** |

* Tunable HP frequency, ** Clock generation power was split equally between LNA & PGA, *** Calculated from measured data

Table. 1. Comparison Table and Performance Summary