A 0.3-V to 1.8–3.3-V Leakage-Biased Synchronous Level Converter for ULP SoCs

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***Abstract*—This letter proposes a robust synchronous wide-range clocked level converter (LC) that converts subthreshold input signals to high I/O voltages for ultra-low power (ULP) SoCs. By biasing the circuit using nMOS leakage current, the design offers robust operation across a wide range of low- and high-supply voltages as well as PVT variations. The design was fabricated in 55-nm CMOS process and shows 60.5-fJ (V_{DDH} = 2.5 V) switching energy, marking a 2.6× improvement over prior works.**

***Index Terms*—Leakage biased, level converter (LC), low power, synchronous, wide range.**

I. Introduction

Modern ultra-low power (ULP) SoCs often employ subthreshold or near-threshold design techniques but also require higher voltage domains for RF, I/O, and other circuits. As a result, wide-range level conversion is needed to interface between the blocks in a ULP SoC. However, the design of a robust level converter (LC) that can operate at subthreshold or near-threshold voltage is challenging. Conventional DCVS-type designs suffer from severe contention between strong pull-up devices and weak pull-down devices, leading to high PVT sensitivity of delay and power and poor robustness.

Consequently, several new approaches have been proposed to achieve a robust wide-range LC. One design effectively reduces contention between pull-up and pull-down devices [1]; however, it employs dynamic operation and requires a keeper bias voltage, increasing design complexity and rendering the conversion range inflexible post-design, thereby, limiting dynamic voltage and frequency scaling (DVFS). Several other approaches employ a current-driven amplifier structure [2]–[5], which provides relatively robust operation but increases power consumption, particularly, static and instantaneous short-circuit power, especially at fast corner and high temperature. Although some works [4]–[7] show good energy and delay performances, they do not support high I/O voltages (>1.8 V), which makes robust LC design more challenging and requires thick gate-oxide transistors. At the same time, most level conversions occur at a timing boundary, i.e., after a sequential element, such as a flip-flop or latch, due to large delay spread among devices operating at different voltage domains. The aforementioned approaches are all asynchronous LCs and hence require an additional sequential element, forgoing possible efficiency improvement by integrating level conversion within a sequential element itself [8]. To address these limitations and achieve a low-power and robust wide-range synchronous LC, this letter proposes a new leakage-biased LC (LBLC) integrated with a latch [11].

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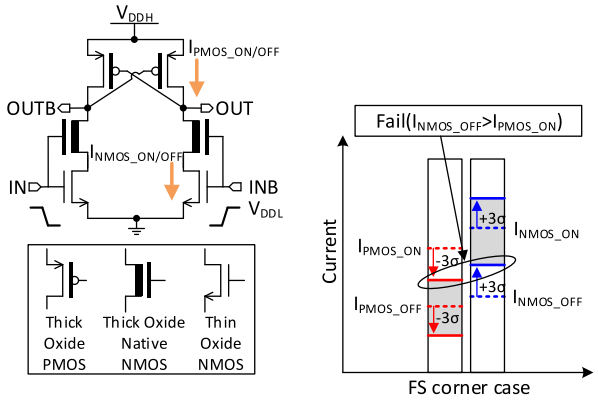

Fig. 1. DCVS-type LC and its current margin plots at FS corner.

II. Leakage-Biased Level Converter

A. Motivation

To guarantee the functionality of a conventional DCVS-type LC (Fig. 1) in subthreshold or near-threshold operation, the low-voltage domain nMOS transistors should be large enough to overcome the strength of the high-voltage domain pMOS pull-up transistors [1]. However, in the fast–slow (FS) corner, or at high temperatures, the off-state current of such large nMOS transistors may become larger than the pMOS on-current, causing functional failure. This two-sided constraint is the main challenge in designing a robust wide-range LC. Therefore, a good design should guarantee that the transistor on-current is always much larger than the off-current of complementary transistors. These requirements provide the motivation for the proposed LBLC.

B. LBLC Core Block

Fig. 2(a) shows the core block of the LBLC. The design removes contention between pMOS and nMOS using tail ($M2$) and precharge ($M11$ and $M14$) transistors that are controlled with a low-voltage domain clock signal. In an analog sense, LCs can be viewed as a specific type of comparator with input that swings between V_{DDL} and ground, and hence we can draw parallels to clocked comparators [9] (i.e., dynamic comparators) that are widely used in many applications. However, clocked comparators rely on precharge pMOS devices with sources tied to V_{DDH}, meaning that the clock must itself toggle at the higher supply voltage. This incurs a large power penalty due to high clock switching activity, which is incompatible with the subthreshold and near-threshold applications where wide-range LCs are necessary. Again taking a more analog perspective, one option would be to dc-bias the clock signal at V_{DDH} and initiate a V_{DDL} magnitude downward swing to turn on the precharge devices. However, given the high voltage tolerance requirements for the wide-range LCs, thick gate-oxide transistors are used as precharge devices, with

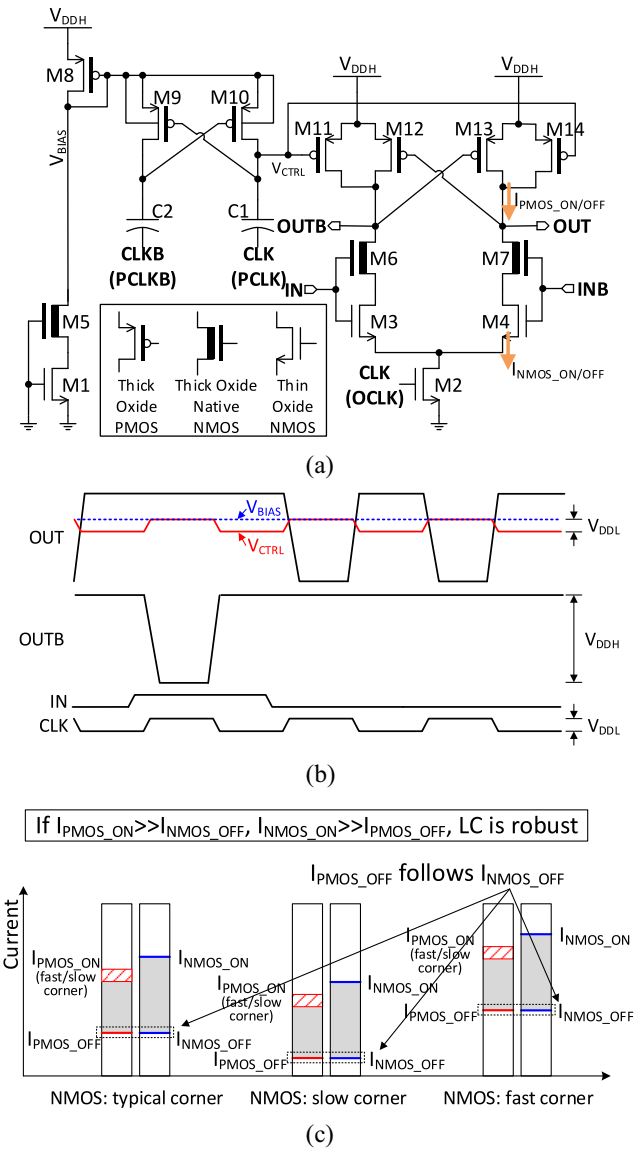

Fig. 2. (a) LBLC core block. (b) Waveform of the LBLC's signals. (c) LBLC's current margin plots indicate that $I_{\text{pMOS\_ON}} >> I_{\text{nMOS\_OFF}}$ and $I_{\text{nMOS\_ON}} >> I_{\text{pMOS\_OFF}}$ for any case. The red shaded region represents the variation in pMOS on-current caused by the difference in ON/OFF current ratio of each process corner.

threshold voltage that exceeds V_{DDL} (i.e., $|V_{\text{THP}}| > V_{\text{DDL}}$). To solve this problem, the proposed LBLC generates the bias voltage for the precharge pMOS transistors ($M11$ and $M14$) using a current mirror, which consists of $M1$, $M5$, and $M8$. Since $M1$'s leakage current is the reference (noting that $M5$ is a native device with $V_{\text{TH}} \sim 0$), V_{BIAS} is set to the value at which $M8$ conducts the same current as $M1$ leakage and varies its value according to PVT variations to ensure the robustness of the proposed LC. Fig. 2(b) shows the V_{CTRL} signal, which is dc-biased by V_{BIAS} and exhibits a V_{DDL} magnitude voltage downswing by exploiting cross-coupled $M9$ and $M10$ with ac-coupling capacitors. V_{CTRL} turns precharge devices $M11$ and $M14$ ON and OFF. Since $M11$ and $M14$ gate voltages are set to V_{BIAS} during the off state, i.e., tracking thin gate-oxide transistor leakage $I_{\text{nMOS\_OFF}}$, they can be turned on with a small V_{DDL} voltage swing despite their large threshold voltage. Also, using this structure, $I_{\text{pMOS\_OFF}}$ and $I_{\text{nMOS\_OFF}}$ remain equal across PVT, which guarantees that the nMOS and pMOS on-currents are always larger than the pMOS and nMOS off-currents, respectively, as described in Fig. 2(c). In other

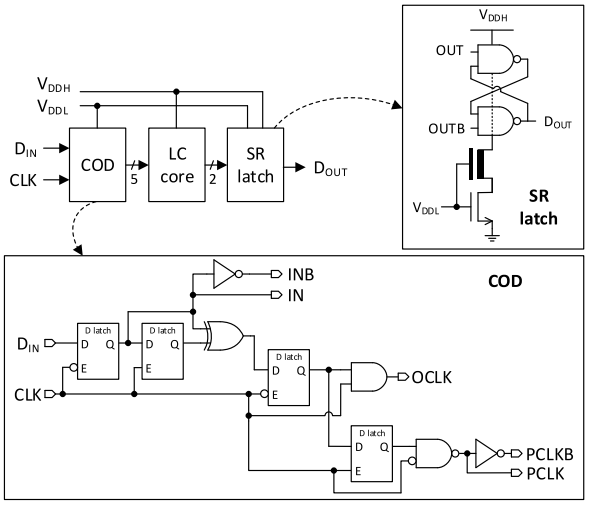

Fig. 3. Overall block diagram of LBLC, consisting of a COD, LC core, and SR latch.

words, owing to the proposed leakage biasing approach, the LBLC meets the requirements for robust LC design explained in Section II.

To ensure the junction leakages of $M9$ and $M10$ do not alter the dc-bias level of V_{CTRL}, the bodies of $M9$ and $M10$ are connected to V_{BIAS} while the bodies of all other nMOS and pMOS transistors are connected to ground and V_{DDH}, respectively. The basic operation of the proposed LBLC is as follows. Initially, CLK is low, and two complementary outputs, OUT and OUTB, are both precharged to V_{DDH}. CLK then goes high. If IN $= V_{\text{DDL}}$, then $M3$ discharges OUTB, turning on $M13$; otherwise, $M4$ discharges OUT, turning on $M12$ (INB is a complementary signal of IN). Note that thick native nMOS devices prevent breakdown in the higher transconductance thin gate-oxide nMOS transistors.

C. LBLC With SR Latch and COD Block

Since two complementary outputs, OUT and OUTB, are both high during precharge, i.e., when CLK is low, an SR latch follows the LC core block to hold the output during this precharge period as shown in Fig. 3. To prevent the SR latch, i.e., static logic gates, from wasting power during the input transition, an nMOS transistor biased by V_{DDL} is inserted so that the SR latch output slew rate matches that of the LC core block.

For the proposed LC core block to function as a level-converting flip-flop, a single negative D latch must precede it. However, due to the precharge, the LC core block consumes switching power every clock cycle even if the input does not change. This degrades the energy efficiency in low data activity scenarios. To address this, a clock-on-demand (COD) block is incorporated, as depicted in Fig. 3, and precharge is avoided in cases where the input data does not toggle. The COD generates an OCLK pulse only if the input data changes; a downward PCLK pulse then follows it in the next half clock cycle for the precharge, as shown in Fig. 4. Note that PCLK remains high during the idle state to prevent V_{CTRL} from leaking up to the value of V_{BIAS} with low PCLK and disrupting the next few precharges in cases of long idle times. In addition, since both the tail and precharge transistors are turned off during the idle state, i.e., OCLK is low and PCLK is high as shown in Fig. 4, $M8$ should have a longer length and/or smaller width than $M11$ and $M14$ to guarantee that the leakages of the precharge transistors are larger than that of the tail transistor, thereby preventing OUT or OUTB from leaking down during the idle state. An alternative way to avoid tristate

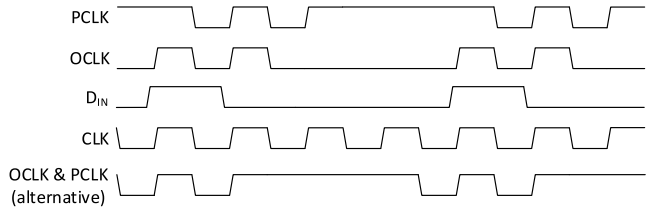

Fig. 4. Waveforms of the OCLK and PCLK signals generated from the COD block. The alternative OCLK and PCLK signals are also depicted.

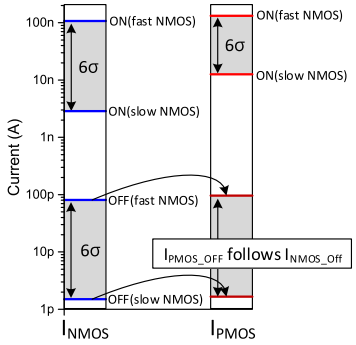

Fig. 5. Current margin plot (simulation results, temp = 25 °C).

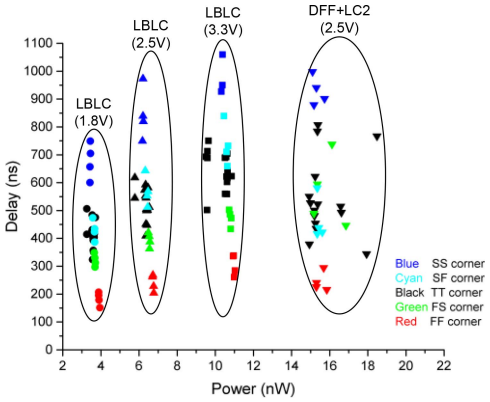

Fig. 6. Test chip delay and power distribution (freq = 100 kHz, temp = 25 °C, $\alpha = 1$).

on OUT and OUTB is by activating a precharge half clock cycle before the input data change and making clock pulses only if the input data changes as described on the bottom waveform in Fig. 4. In this case, however, an additional sequential element preceding the LC core might be required to predict the following input data. Logic gates used for COD operate in the low-voltage domain and, therefore, their power consumption is negligible compared to the high-voltage domain component of LC power. More specifically, in the worst case (activity factor $\alpha = 0.5$), the overhead of the COD block is 6%, 10%, and 20% of the total LC power for 3.3 V, 2.5 V, and 1.8 V V_{DDH}, respectively. The savings are more significant. If $\alpha = 0.25$, COD saves 45%, 42%, and 34% of the total LC power for 3.3 V, 2.5 V, and 1.8 V V_{DDH}, respectively. If $\alpha = 0.1$, the savings rise to 76%, 74%, and 68%. The COD-related area is 21% of the total LC area.

III. Simulation and Measurement Results

The current margin plot of the LBLC from the simulation is shown in Fig. 5. I_{pMOS_OFF}, i.e., the off-current of the precharge transistors, follows I_{nMOS_OFF} as expected because it is biased by the nMOS leakage current. Consequently, the proposed LBLC is able to guarantee its robustness across PVT variations.

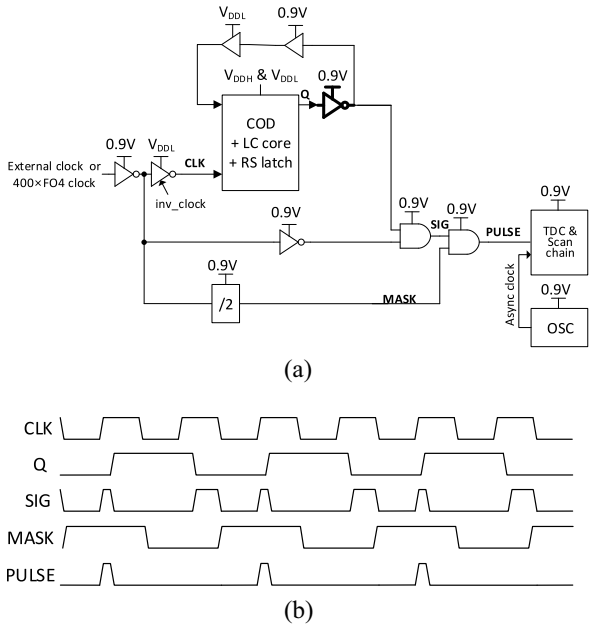

Fig. 7. (a) Test structure for the delay of LBLC. (b) Waveform of the signals generated from the test structure.

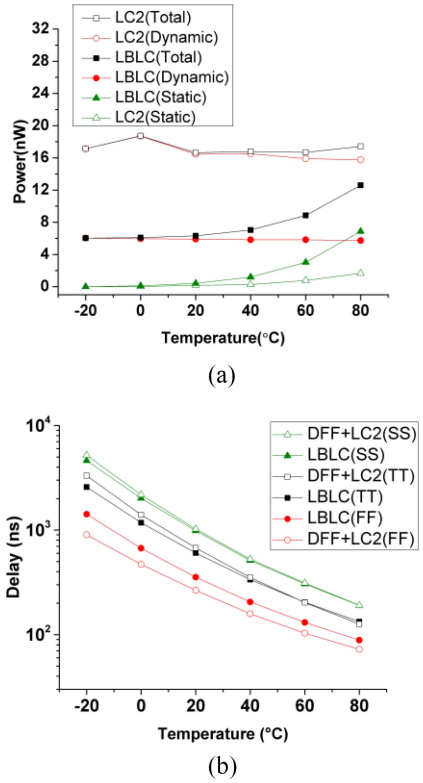

Fig. 8. Temperature sweep for (a) power (TT corner, freq = 100 kHz, $\alpha = 1$) and (b) delay (TT, SS, FF corner).

The proposed LBLC is fabricated in a 55-nm CMOS process, and its performance is verified through measurements of 31 dies (15 TT, 4 FF, 4 FS, 4 SS, 4 SF corner chips). For a fair comparison, the previously proposed LC^2 [1] (with a preceding DFF) was fabricated in the same process, which operates using 2.5 V as V_{DDH}. Fig. 6 shows the measured delay and power. The LBLC consumes 2.6× lower power than [1] on average with comparable speed

TABLE I
COMPARISON TABLE (AVERAGE OF TT CORNER CHIPS)

	Proposed LBLC	DFF+ Kim [1]	Kim [1]	Osaki [2]	Zhou [3]	Lotfi [5]
Technology	55nm	55nm	130nm	0.35μm	0.18μm	40nm
Conversion	0.3V to 1.8-3.3V	0.3V to 2.5V	0.3V to 2.5V	0.4V to 3V	0.3V to 1.8-3.3V	0.35V to 1.1V[a]
Type	LCFF	LCFF	Static	Static	Static	Static
Clk to Q delay (0.3V to 2.5V)	523ns (17.4FO4)	546ns (18.2FO4)	Delay:41.51ns (2.38FO4)	-	Delay: 168ns (1.04FO4)	Delay: 15.5ns (>1.17FO4)
Static Power	234pW (1.8V) 256pW (2.5V) 282pW (3.3V)	159pW	475pW	230pW	160pW (1.8V) 340pW (2.5V) 970pW (3.3V)	550pW (1.1V)
Energy/ Transition	33.1fJ (1.8V) 60.5fJ (2.5V) 99.5fJ (3.3V)	158fJ	229fJ	5.8pJ	39fJ (1.8V) 188fJ (2.5V) 954fJ (3.3V)	4.2fJ
Area	154μm^2	152μm^2 (/w diodes)	102μm^2	1880μm^2	153μm^2	8μm^2

[a]1.1V is not a high I/O voltage for which thick gate-oxide transistors are necessary. Accordingly, [4] was designed with thin gate-oxide transistors only, unlike the others.

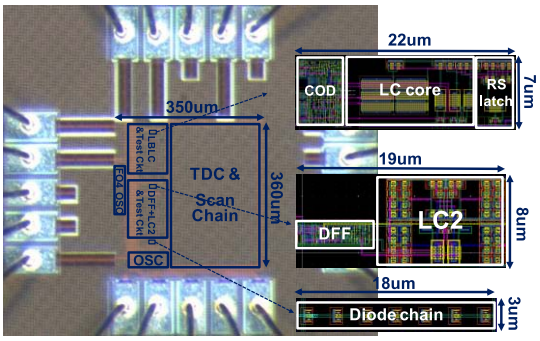

Fig. 9. Die photograph and layout of LBLC, LC^2 and its diode-chain.

and flexible V_{DDH}. The delay was measured by the stochastic time-to-digital converter (TDC) integrated with the LBLC as shown in Fig. 7(a). The nominal voltage of the low-threshold voltage (LVT) digital standard cells used in the test structure is 0.9 V. The maximum tolerance voltage of those standard cells is 1.8 V; hence, the output of the LBLC is followed by an inverter made of thick gate-oxide devices to prevent the breakdown of thin gate-oxide devices. The test structure generates a periodic pulse signal, i.e., PULSE in Fig. 7(b), the width of which indicates the *C*-to-*Q* delay of the LC. The following TDC produces a histogram of the PULSE signal by sampling and accumulating the signal at the edge of the asynchronous internal oscillator clock and then calculates the *C*-to-*Q* delay: *C*-to-*Q* delay = 2× (period of CLK) × (frequency of PULSE HIGH)/(total sample size). Note that since the delays of the logic gates in the test structure are much faster than that of LC, they are negligible in measuring the LC delay. Specifically, even the delay of *inv_clock* under V_{DDL} is less than 1% of the LC delay in the simulation. Fig. 8 shows the power and delay across temperature, with the LBLC showing similar speed as [1]. At high temperature, the LBLC's power increases rapidly due to the increasing leakage of the thin gate-oxide transistors. However, its total power is still smaller than [1] even at 80 °C with a frequency of 100 kHz. Table I compares the results obtained for the LBLC with other works, and Fig. 9 shows a test chip die photograph. Note that V_{DDH} in [5] is 1.1 V, which is lower than 1.8–3.3 V, the target V_{DDH} of the others.

IV. CONCLUSION

In this letter, a new leakage-biased level converter, i.e., LBLC, was presented. The proposed LBLC has the lowest energy/transition compared with previously proposed LCs that support high I/O voltages (>1.8 V) while also inherently supporting flexible voltage levels. Given a typical ULP 32b MCU energy/cycle of 6.4 pJ [10], the LBLC allows for 32b up-conversion to I/O voltages within 5% of this total energy budget.

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