A 67-fs$_{rms}$ Jitter, −130 dBc/Hz In-Band Phase Noise, −256-dB FoM Reference Oversampling Digital PLL With Proportional Path Timing Control

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***Abstract*—An *LC* oscillator-based reference oversampling PLL (OSPLL) is proposed in this work. An *LC* digitally controlled oscillator (DCO) with proportional path gain profile control and DCO tuning pulse timing control scheme is proposed for optimal phase noise. Designed in 28-nm CMOS process, the proposed PLL achieves 67.1-fs RMS-jitter with 5.2-mW power consumption, which translates to −256-dB FoM. The in-band phase noise of the PLL is −130 dBc/Hz at 4-GHz output frequency. The reference spur of the proposed PLL is −78 dBc.**

***Index Terms*—Digital controlled oscillator, digital PLL, frequency synthesizer, reference oversampling PLL, reference spur.**

I. Introduction

Ultralow noise frequency synthesis is critical given the ever-increasing data rates of modern communication systems. For example, 5G wireless systems [1] and ultrahigh-speed wireline transceivers [2] require sub-100-fs clock jitter to meet tight system requirements. However, it is difficult to implement frequency synthesizers with ultralow noise and spur while maintaining reasonable power consumption. Reference quadruplers [3], [4] achieved low in-band noise by boosting the reference frequency. However, [3] requires a delay line and an additional PLL for minimizing the period mismatch among the interpolated cycles which resulted in relatively high in-band noise (−110 dBc/Hz) and high power consumption (22.8 mW). The design in [4] relies on the absolute accuracy of multiple voltage references and showed a high spur (−53 dBc) even after the calibration. It also cannot utilize the largest slope point of the sinewave reference, which is desirable for low phase noise.

Recently, a reference oversampling PLL (OSPLL) was proposed which offers many advantages over reference quadruplers [5]. As shown in Fig. 1, the OSPLL loop offers much higher reference boosting ratio of *N*, which effectively cancels the feedback factor, thereby achieving low in-band phase noise. In addition, OSPLL loop bandwidth is not limited to 1/10th of FREF and can be configured to be larger than FREF, providing better digital controlled oscillator (DCO) noise filtering. The reference spur can also be very low because the loop operates at FOUT not FREF. Also, any timing skew in sampling each reference point is cancelled by a voltage in ac-coupling capacitors thereby resulting in negligible spur contribution.

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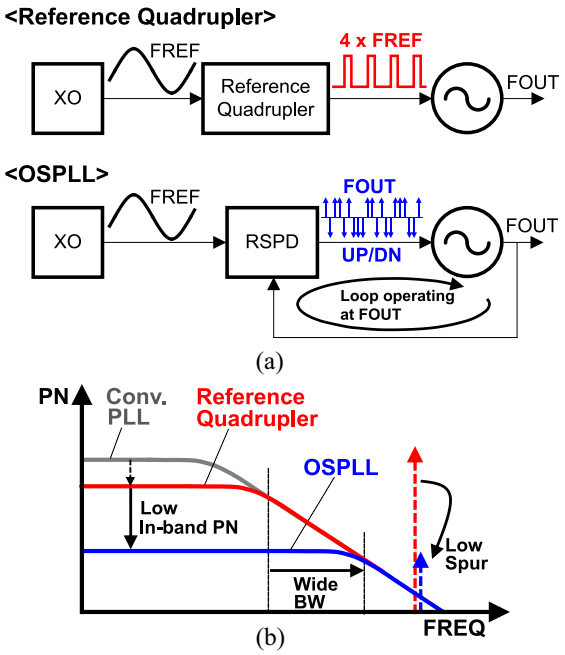

Fig. 1. Comparison of OSPLL versus reference quadrupler. (a) Block diagram. (b) Phase noise and spur improvement.

This letter presents an *LC* oscillator-based OSPLL to achieve extremely low jitter. In this letter, we propose an *LC* DCO with proportional path gain control and DCO tuning pulse timing control scheme, which enables 16-dB PLL FoM improvements compared to [5]. The proposed PLL achieves with 67.1-fs$_{rms}$ jitter, −78-dBc spur, and −130-dBc/Hz in-band phase noise at 4-GHz output frequency while consuming 5.2 mW.

II. Proposed PLL

A. Operation Concept of the Proposed OSPLL

The proposed OSPLL (Fig. 2) samples the sinusoidal reference at every FOUT cycle to obtain the phase error using time-interleaved reference-sampling-phase-detectors (RSPDs) [5]. Assuming no noise at FOUT, each of the *N* RSPDs samples an identical point of the sinusoidal FREF, as marked with a blue dot (Fig. 2, bottom). Jitter in FOUT results in a change of the sampled voltage, which represents phase error. The sampled voltage is then quantized by a comparator-based bang-bang phase detector to generate either an UP or DN signal. Note that an ac-coupling scheme is used before the comparator to remove the dc voltage level that differs for each RSPD, enabling a common reference voltage VCM to be used for all RSPDs. Since the RSPDs only detect the ac fluctuation of the phase error, an absolute locking phase is provided by a "pivot" RSPD without the ac-coupling capacitor. This ensures that Φ1 matches with

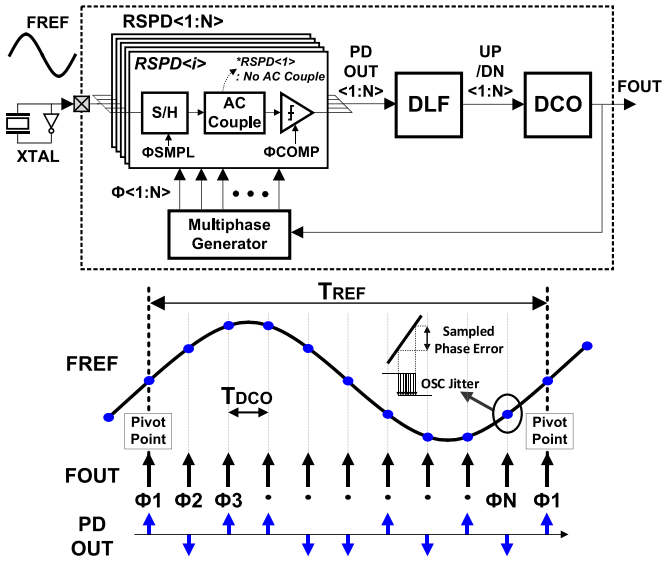

Fig. 2. Operating principle of the reference OSPLL.

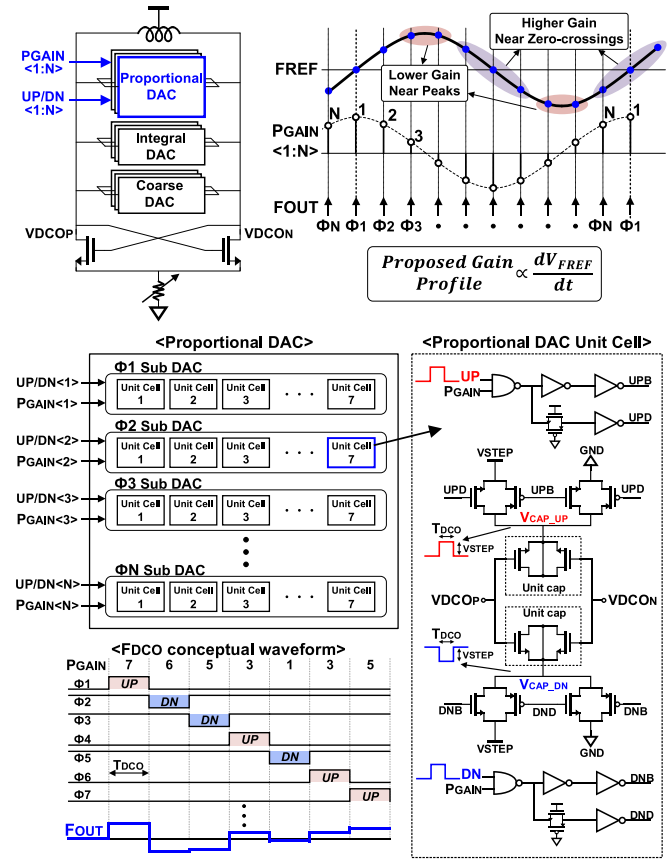

Fig. 3. Structure of the proposed DCO and the proportional DAC.

a positive VCM-crossing point of FREF. The sampling points of the other RSPDs are relatively defined to the pivot position. Therefore, any timing mismatch caused by clock buffers driving RSPDs simply moves the sampling point and does not cause an output spur due to the ac-coupling nature. The integral path of the digital loop filter only takes the output of pivot RSPD to minimize the power and area overhead. Also, all the building blocks except for the DCO and the multiphase generator operate at FREF in a time-interleaved fashion making it friendly to high-frequency applications.

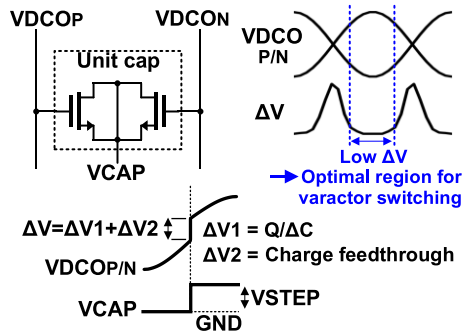

Fig. 4. DCO varactor switching noise.

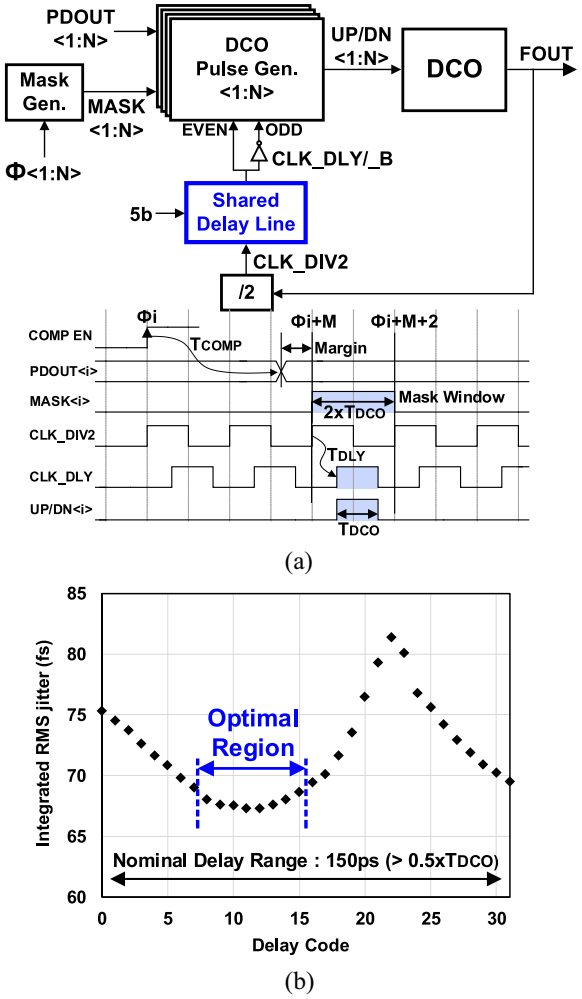

Fig. 5. Proposed DCO tuning pulse timing control using shared delay line. (a) Block diagram and timing diagram. (b) Measured PLL output jitter with delay code.

Crystal oscillators (XO), with naturally sinusoidal waveforms, are the most common reference clock source for low noise frequency synthesizers. Therefore, conventional PLLs require a reference buffer that converts the sinusoidal XO output to a square wave. This buffer incurs high power consumption while also generating noise [6]. As the proposed OSPLL directly samples the sinusoidal waveform, no reference buffer is needed, improving power and noise. Compared to [6], in which it is difficult for the crystal to directly drive the PLL due to a large time-varying impedance of the switching sampling capacitor, this work maintains constant input impedance (1 pF) so the crystal can drive it without any a buffer.

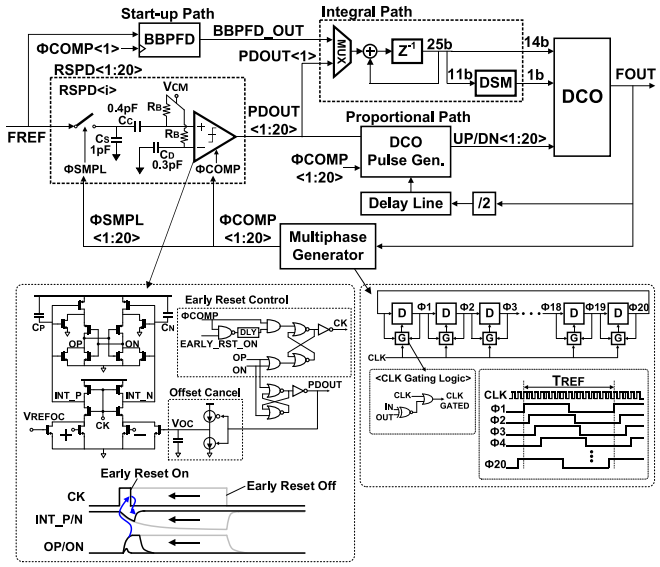

Fig. 6. Overall block diagram and schematic detail of the proposed PLL.

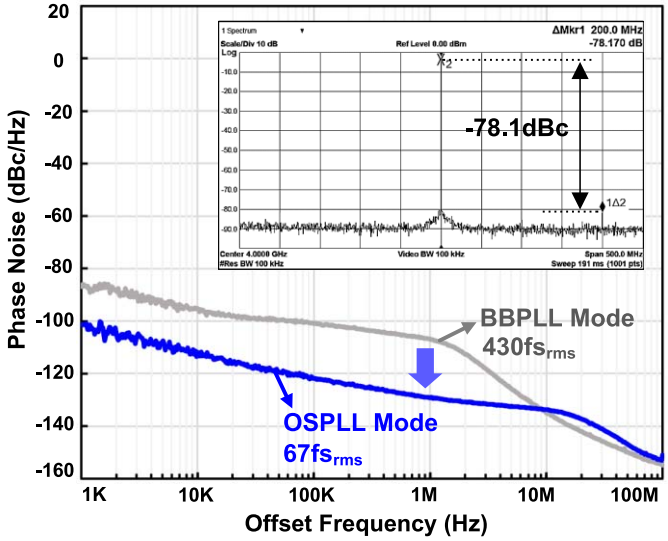

Fig. 7. Measured output phase noise plot and the reference spur and comparison with bang-bang PLL (BBPLL) mode.

B. DCO With Proportional Path Gain Profile Control

Gain from phase error to a sampled voltage depends on FREF slope where a particular RSPD samples it. The steep slope at the VCM-crossing point yields a high gain and offers excellent phase error detection (Fig. 3, top), whereas near the peak/valleys of FREF, gain is low and the sampled voltage is noise-dominated. Therefore, the proportional path gain (PGAIN<1 : N>) is implemented as quadrature to FREF to emphasize the RSPDs that sample steeper FREF points.

To implement this proportional gain profile, we propose a capacitor DACs with 3-bit gain programmability (Fig. 3, mid). The proportional path gain is predetermined at design time and it does not require any trimming. To set the unit capacitance below 10 aF for fine frequency resolution (10 KHz), we use a capacitance control scheme where the NMOS varactor bottom node switches between GND and VSTEP (Fig. 3, right). UP pulses switch the varactor bottom from GND to VSTEP, increasing DCO frequency, and vice versa for DN. Fig. 3 (bottom) illustrates how DCO frequency is controlled

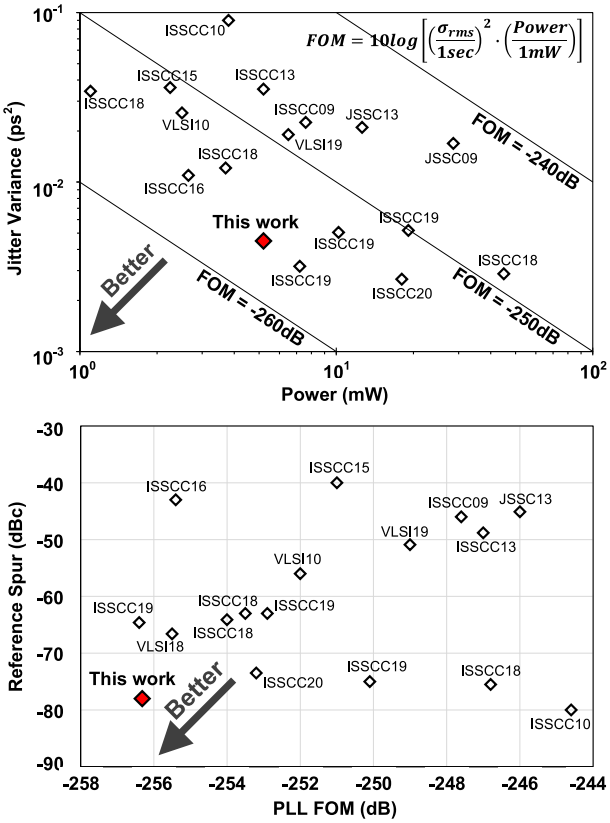

Fig. 8. Comparison with low noise integer-*N*-based frequency synthesizers.

every TDCO via UP/DN pulses which have PGAIN particular to each RSPD.

C. DCO Tuning Pulse Timing Control

The switching operation causes varactor capacitance modulation and creates PLL jitter [7]. As shown in Fig. 4, the capacitance change creates voltage fluctuation proportional to $\Delta V1 = Q/\Delta C$, where Q is the total charge in the varactors and ΔC is the capacitance change due to switching. This amplitude change then increases output jitter through the AM/PM conversion. The magnitude of Δ V1 depends on the varactor switching point. In addition, direct charge-feedthrough of the switching waveform also creates Δ V2 that disturbs the oscillator phase through the impulse sensitivity function mechanism of the *LC* oscillator [8]. These two noise creation mechanisms can be minimized by setting a proper switching time. To set the optimal timing of the proportional path control and minimize the amplitude disturbance (and thus output jitter), we use a digitally controlled delay line. We place a single shared delay line at the input of the DCO pulse generator to avoid using N delay lines and delay mismatch between UP/DN pulses, as shown in Fig. 5(a). The mask signal from the multiphase generator selects the correct UP/DN pulses. Fig. 5(b) shows the measured jitter and its timing dependency.

D. Overall Block Diagram and Circuit Details

Fig. 6 shows a detailed schematic of the proposed PLL. The design includes a start-up path that uses a conventional bang-bang phase and frequency detector (BBPFD), which is turned off during normal operation. Each RSPD samples FREF with a 1-pF sampling capacitor and biases the comparator input at VCM using a large resistance RB designed with a subthreshold transistor biased with a current reference to remove its PVT dependency. An early reset

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART LOW NOISE INTEGER-*N* FREQUENCY SYNTHESIZERS

	This Work	ISSCC 20 Mercandelli	ISSCC 19 Kim	ISSCC 19 Zhang	ISSCC 18 Turker	ISSCC 18 Sharma	ISSCC 18 Sharkia	ISSCC 16 Elkholy
Type	**OSPLL**	SPLL	SSPLL	SSPLL	CPPLL	RSPLL	SSPLL	ILCM
Process (nm)	**28**	28	65	40	16	65	65	65
Reference (MHz)	**200**	500	100	200	500	50	100	125
FOUT (GHz)	**4**	12.5	3.8	14	12.5	2.55	5	8
Int. Jitter (fs)	**67.1**	51.7	72	56.4	53.6	110	185.3	104.7
Int. Range (Hz)	**10K-100M**	1K-100M	1K-30M	1K-100M	10K-10M	10K-100M	10K-50M	10K-30M
In-band PN (dBc/Hz) (✱ Normalized to 4GHz)	**-130**	N/A	-123.6✱	N/A	-127.1✱	-121.3✱	-122.3✱	-115.6✱
Ref. Spur (dBc)	**-78.0**	-73.5	-75.0	-64.6	-75.5	-63.0	-64.1	-43.0
Power (mW)	**5.2**	18.0	19.1	7.2	45.0	3.7	1.1	2.7
FOM (dB)	**-256.3**	-253.2	-250.1	-256.4	-246.8	-253.5	-254.0	-255.4
Area (mm^2)	**0.17**	0.16	0.21	0.23	0.35	0.36	0.01	0.27

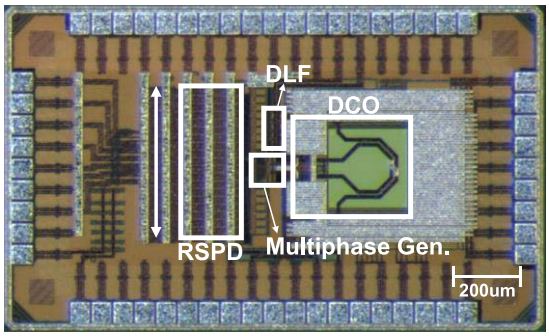

Fig. 9. Die photograph.

scheme [9] terminates comparator operation before making its full transition, reducing measured comparator power consumption by 25%. Comparator input offset is canceled by a continuous charge-pump offset cancellation loop. The output of the pivot RSPD is connected to the integral path to accurately set the DCO frequency. The multiphase generator is implemented using a ring counter that includes clock gating to reduce power when flip-flop input and output are the same.

III. MEASUREMENT RESULTS

The proposed PLL was fabricated in 28-nm CMOS, occupies 0.17 mm^2, consumes 5.2 mW, and produces a 4-GHz output frequency from a 200-MHz reference. Fig. 7 shows the measured phase noise and output spectrum plots. Measured in-band phase noise is −130 dBc/Hz and integrated jitter from 10 kHz to 100 MHz is 67.1 fs$_{rms}$, which is significantly improved from the conventional bang-bang PLL mode (430 fs$_{rms}$). The measured reference spur is −78 dBc. Table I compares the proposed PLL with state-of-the-art low jitter Integer-*N* frequency synthesizers. In-band phase noise level is normalized to 4 GHz for fair comparison. The performance of recently published designs is plotted in Fig. 8. The PLL achieves ultralow sub-100 fs jitter and low power at the same time, which translates to state-of-the-art FoM of −256.3 dB. The proposed PLL also achieves excellent reference spur while maintaining state-of-the-art FoM. Fig. 9 provides a die photograph.

IV. CONCLUSION

This letter presents a reference OSPLL with *LC* oscillator. The proportional path gain profile and DCO tuning pulse timing are optimally set for low phase noise. With the proposed technique, the PLL achieved 67.1 fs$_{rms}$ jitter and −78-dBc reference spur with 5.2 mW power consumption. The FoM of the PLL is −256.3 dB.

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