A mm-Scale Sensor Node with a 2.7GHz 1.3µW Transceiver Using Full-Duplex Self-Coherent Backscattering Achieving 3.5m Range

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***Abstract*—This paper presents a 1.3 µW backscatter-based transceiver for battery-powered millimeter-scale sensor nodes. By taking advantage of the coherence of reflected dual-side bands, it attains an optimum SNR and improved interference rejection with low-power, non-coherent binary modulation. Integrated with a 2.1×4 mm planar antenna in a complete, crystal-less sensor node, it achieves a 3.5 m communication distance with a reader transmitting 31 dBm equivalent isotropic radiated power (EIRP).**

***Keywords*— radio transceivers, low-power electronics, communication systems**

I. Introduction

Internet of Things (IoT) applications are being scaled to increasingly smaller sizes, introducing a need for mm-scale transceivers with long lifetimes. Key challenges in mm-scale IoT communication include the extremely restricted battery size (limiting instantaneous power and energy budget) and mm-scale antenna (with low radiation efficiency and hard to match impedance). A number of proposed solutions use backscatter schemes for simultaneous power and communication with a fully passive sensor. Their limiting factor, however, is typically the power transmission, restricting distance to <50 cm even with >30 dBm power from the reader [1-5]. In this paper, we propose a 1.3 µW back-scatter transceiver for an active, battery-powered light-energy-harvesting mm-scale sensor with an integrated 2.1×4 mm planar antenna. Without the requirement of wireless power delivery, the proposed active back-scatter scheme improves the uplink distance while achieving ultra-low power consumption and exploiting the coherence of dual-side bands to improve interference rejection.

To address self-interference at the reader, a typical solution modulates the back-scatter symbol with a local oscillator (LO) (Fig. 1) to shift the carrier frequency to an intermediate frequency (IF). Such IF back-scatter modulation achieves an optimal SNR when it uses multi-state (complex-valued) modulation, which results in a single sideband signal without an image [6]. However, this type of modulation increases the power consumption in the LO and also introduces the design challenge of achieving accurate complex-valued impedance matching with a mm-size antenna. A simpler and lower power approach is to use binary LO modulation, which results in dual reflected sidebands. However, the doubled bandwidth from dual sidebands invites 1.5 dB higher noise, assuming transmit and receive at the reader have a perfectly phase-aligned carrier signal, or up to 3dB if not. A second challenge is that the LO on the tag has poor phase noise and frequency stability due to the lack of a PLL or crystal due to energy and area constraints. To address this, a previous work utilized nonlinearity to generate an LO from the downlink signal, but this approach requires high input power [2], possibly limiting communication distance. A third key challenge stems from uplink interference because the reader targets a very aggressive sensitivity level of < -120 dBm and the back-scatter power is easily overwhelmed by interferers.

To address these challenges, we propose a protocol (Fig. 1) that uses binary impedance modulation (-1 and +1 reflection coefficient) to maintain low power and exploit the fact that the two sidebands are "self-coherent" when mirrored with respect to the downlink carrier signal at the reader regardless of the LO frequency uncertainty or phase noise. Since interference is in

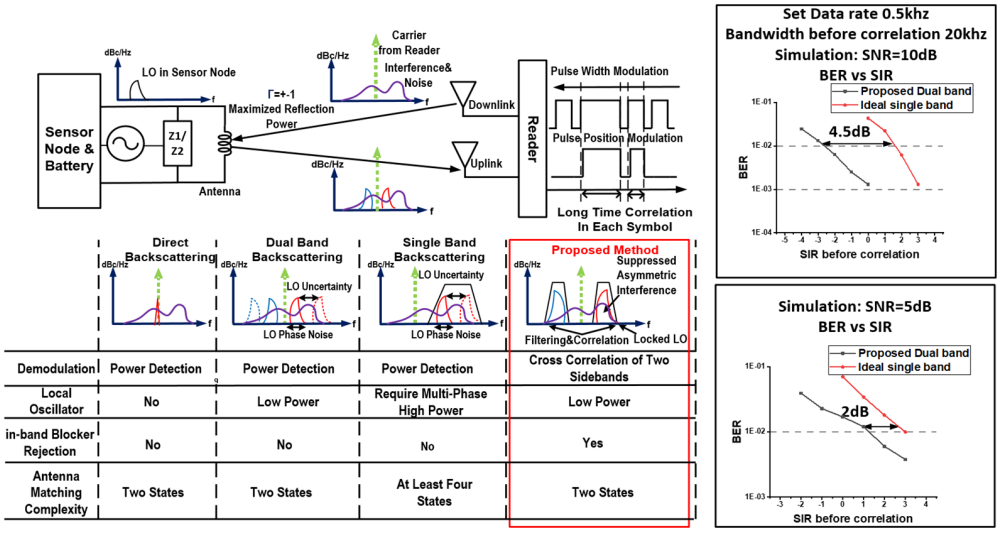

Fig. 1. System principle of self-cross-correlation backscattering-based transceiver implemented in a mm-sized sensor node

general uncorrelated between the two sidebands, our approach has the key advantage that is naturally rejects in-band interference compared to both standard dual sideband and quadrature single sideband modulation. This interference rejection ability is critical for scenarios with high receive sensitivity. The simulation in Fig. 1 shows our proposed approach achieves 4.5 and 2 dB interference tolerance gain compared to the ideal quadrature modulation at 10 and 5 dB SNR, respectively. Furthermore, by correlating the two symmetric sidebands, the proposed system limits the SNR loss to 1.5 dB even in the presence of phase mismatch between the reader transmit and receive chains.

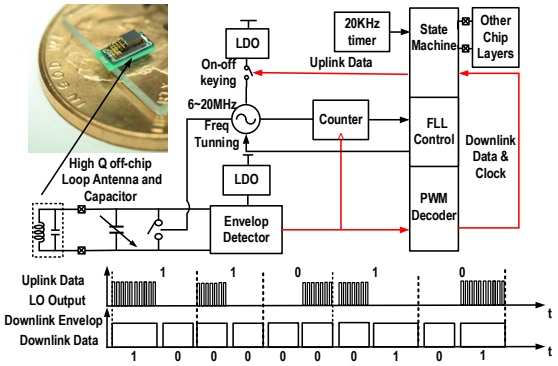

Fig. 2. Transceiver architecture including envelop detector for downlink, ring oscillator modulating cap bank for uplink and frequency locking.

II. Circuit Design

A. Overall Architecture

Fig. 2 shows the overall architecture. A 2.1X4 mm PCB loop antenna is placed below a stack of chip layers. Since the system does not have a crystal, a ring oscillator is used to generate the LO and modulates the capacitor bank with pulse position modulation (PPM) for the uplink data. The LO frequency is locked to the pulse width of the downlink signal envelope while the uplink symbol boundary is synchronized to the edge of the envelope, enabling accurate correlation timing between the two sidebands of the uplink signal within a long symbol length (>1 ms).

B. Core Circuits

The on-chip capacitor bank C1, the MOS switch M1, and the off-chip capacitance C2 are shunted together to provide a high Q matching network for the inductive loop antenna (Fig. 3). When M1 (7 µm/0.18 µm) is on, its on-resistance degrades the Q factor drastically, making the reflection coefficient (Γ) close to -1. When M1 is off, the total capacitance resonates with the antenna to boost the RF signal voltage, achieving Γ≈+1. The 6-20 MHz LO modulates M1, and the uplink data is encoded by enabling or disabling the LO using 2-PPM modulation. The transceiver uses a ~20-kHz timer (~nW) to count the pulse width from the envelope detector (ED) output to decode the downlink PWM data. While decoding downlink wakeup commands, the LO frequency is calibrated within 20 kHz using the pulse width of the downlink signal.

The tunable resistor R1 in the RO-based LO circuit (Fig. 3) shifts the DC level of the oscillator swing before it enters the buffer to keep the duty cycle of the RO close to 50%, maximizing the backscattering power in the sideband. The R1 setting was tuned only once per chip and then kept fixed. The LO has a current source with 14 tuning bits and achieves 20-kHz tuning steps for accurate, automatic locking. To reduce the stabilization time of the LDO supplying the LO when it starts up, two 10 pF capacitors store the critical voltages at nodes N1 and N2 when the LDO is turned off and reinstate them when it is re-enabled. This reduces the LDO stabilization time from 300 µs to 50 µs. The ED has a self-referenced analog output that detects the uplink signal power envelope. The source-degeneration PMOS (P1) sufficiently lowers the feedback loop bandwidth inside the ED (<100 Hz) for the low data rate (<1 KHz). The two RF inputs are fed into the gate and source of the same NMOS to maximize the conversion gain. The resistor R2 (50 kΩ) in the ED is chosen for a high conversion gain by forming a large impedance in the RF input chain but a small impedance for the DC circuit. To tune the matching network resonance, a capacitor bank is used with a 160 MHz tuning range and 15 MHz step. Two small MOS switches in each branch function as a resistor (~10 kΩ) to provide DC bias for the large MOS switch.

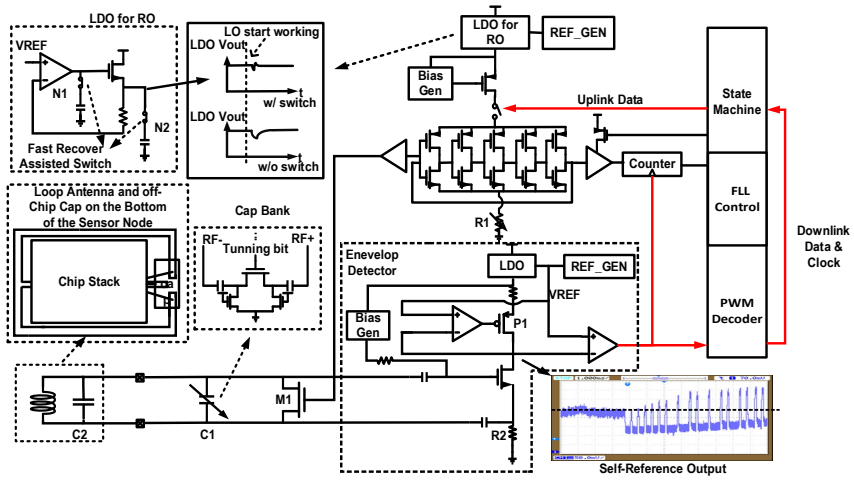

Fig. 3. Circuits of the self-reference envelop detector, cap bank, fast-recovery-LDO and ring oscillator

III. Communication Protocol

In the proposed protocol (Fig. 4), the reader first sends several (>10) fixed-width pulses, from which the sensor obtains the reference pulse width. The sensor then locks its LO based on the downlink signal and presets its control words. After receiving the preamble, the sensor simultaneously receives downlink data and back-scatters uplink data. For each sideband, the reader applies a 30-kHz-wide bandpass digital filter. The LO phase noise and frequency locking resolution set the filter bandwidth. The reader performs cross-correlation of the two filtered signal sidebands over the exact symbol duration to maximize the SNR and filter out uncorrelated interference. The reader then decodes the data based on the correlation result. Since the uplink symbol timing is synchronized to the downlink signal, the reader can adjust the data rate based on the link distance and quality of the backscattering signal. Multiple mm-scale sensors can backscatter simultaneously by configuring different LO frequencies on each sensor.

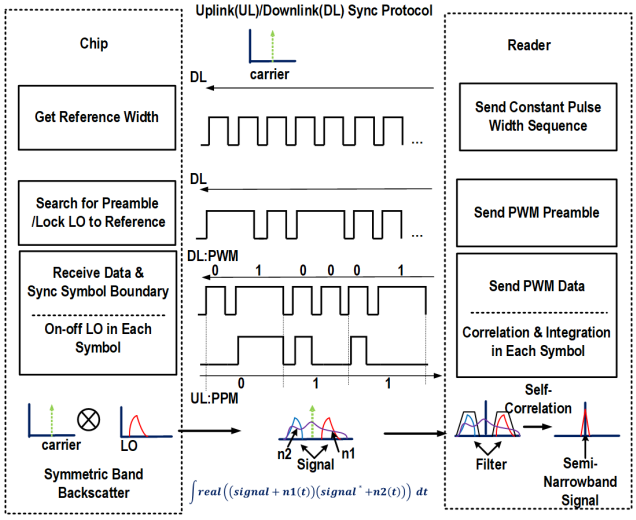

Fig. 4. Adaptive reference width PWM, full-duplex, uplink to downlink synchronization communication protocol.

IV. Measurement Result

The transceiver chip (1.3×2.0 mm) is fabricated in 0.18 µm CMOS and integrated into a complete 2.1×4×1 mm stacked sensor system, including a 2.1×4 mm loop antenna PCB, a thin-film battery chip layer, an energy harvester, PV cells, a power management unit and a processor to form a complete, autonomous and fully functional sensor node. The high Q loop antenna achieves a radiation efficiency of -24 dB at a carrier frequency of 2.7 GHz (simulation). Fig. 5 shows the system photo and chip micrograph.

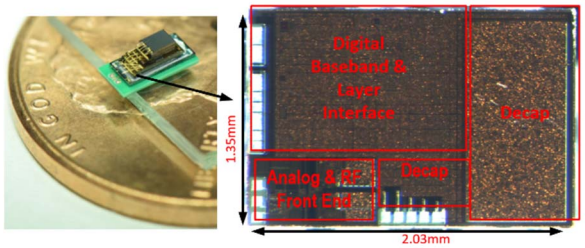

Fig. 5. Sensor node picture and die micrograph

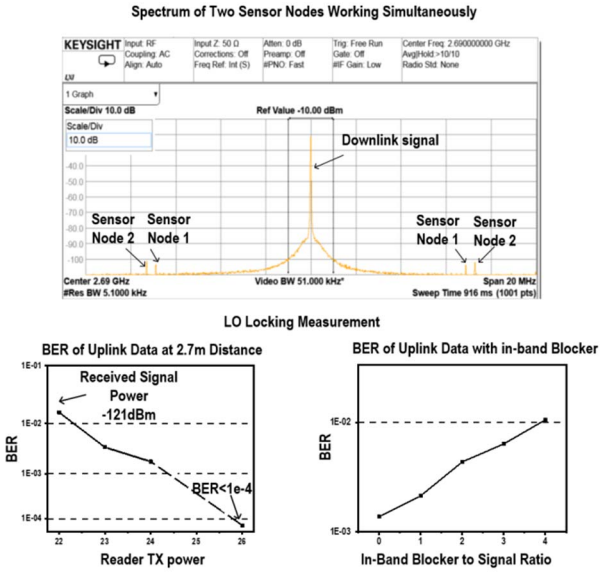

Fig. 6. Spectrum of sensor nodes and BER measurements

The spectrum in Fig. 6 shows two sensor nodes configured with different LO frequencies transmitting uplink messages to one reader simultaneously. The reader is implemented on a commercial software radio (USRP) for TX and RX. The BER vs. the reader TX power is measured in an anechoic chamber. The 12 dBi gain TX antenna and 1.5 dBi RX antenna of the reader are placed 2.7 m (limited by the chamber dimension) from a fully functional and completely wireless, battery-operated sensor node. The sensor achieves a BER=1.8×10^{-3} with a reader transmitting 24 dBm EIRP and a data rate of 250 bps. In this configuration, the sensor node EIRP is -60 dBm. Measurement in a building hallway at a distance of 3.5 m showed an uplink BER of $<10^{-3}$ with a 31 dBm EIRP reader. The proposed double sideband correlation demodulation achieves a BER of 1.1×10^{-3} in the presence of an in-band white-Gaussian blocker in one of the sidebands with a blocker-to-signal power ratio of 0 dB and an uplink received signal power of -101 dBm, which is far superior than that achieved by conventional backscatter schemes.

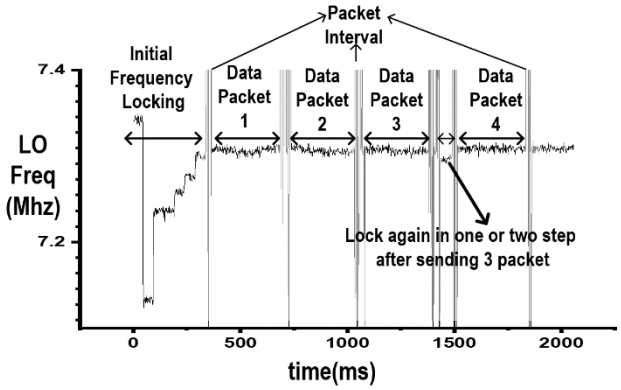

Fig. 7. LO locking measurement

Fig. 7 shows automatic LO locking when the sensor node is configured to lock its LO frequency every 3 uplink data packets (measured at the reader during baseband processing). Except

Table 1. Performance summary and comparison to other recent mm-scale transceivers

	This Work	M.Tabesh JSSC 2015 [1]	B.Z ISSCC 2018 [2]	S. Pellerano JSSC 2010[3]	H.Dagan JSSC 2014 [4]	W. Biederman JSSC 2013[5]	L.X.Chuo ISSCC 2017 [7]
Technology	180nm	65nm	65nm	90nm	180nm	65nm	180nm
Frequency	2.48G	24G(DL)/60G(UL)	5.8G	47G	24G	1.5G	915M
Radio Type	Battery-assisted Backscatter	Wireless Harvest Active Transmit	Wireless Harvest Backscatter	Wireless Harvest Backscatter	Wireless Harvest Backscatter	Wireless Harvest Near field coupling	Battery-assisted Active Transmit
Antenna	Planar Off-Chip Loop	Two On-Chip Dipole	On-Chip Inductor	Off-Chip (0dB Gain)	Two On-Chip Dipoles	On-Chip Inductive	3D Magnetic Off-Chip Loop
Reader EIRP	23dBm* / 31dBm** (1.5dBi GainAntenna for the Receiver)	45dBm	32.4dBm (near field)	30dBm	27.5dBm (17.5dBi Gain Antenna for the Receiver)	17dBm (near field)	N/A
Dimension	2.1x4x1mm^3	3.7x1.2mm^2	116µmx116µm	1.3x0.95mm^2 (w/o antenna)	3.74x1.86mm^2	500umx250um	3x3x3mm^3
Power Consumption	DL: 0.77µW UL&DL:1.28µW	UL:11mW (active)	N/A	19µW (Stand by)	39.5µW (Including Memory)	10.5uW (4 Channels)	UL:2mW DL:1.85mW
Modulation	DL:PWM UL:2-PPM	DL:Pulse-Pause Mod UL:M-PPM	DL:<4%ASK UL:HIML	UL:PWM	DL: Pulse Interval Mod UL: Machester Code ASK	DL:PPM UL:Miller Code ASK	DL:2-PPM UL:M-PPM
Data Rate	DL: 0.25~2Kb/s UL:0.125~1Kb/s	DL:6.5Mb/s UL:1.2-12Mb/s	DL:5Mb/s UL:4kb/s	UL:5-50Kb/s	N/A	DL:1Mb/s UL:1Mb/s	DL:7.8~62.5Kb/s UL:0.03~30Kb/s
Measured Distance	DL:3.3m* / 4.5m** UL:2.7m* /3.5m**	DL:50cm UL:50cm	DL:1mm UL:0.7mm	UL:1.8cm (calculation)	DL:20cm UL:20cm	DL:1mm UL:1mm	UL:20m (NLOS)

* Measured in the anechoic chamber. Distance is limited by the chamber dimension and the reader EIRP is reduced to match the distance
** Measured in a building hallway. The reader EIRP is set to 31dBm for the maximum distance

for the first iteration, frequency locking takes only 1-2 steps. The measured waveform of the ED and LO shown in Fig. 8 demonstrate the synchronization between the LO on-off status and the ED rising edge. It shows the duplex operation of the PWM downlink and PPM uplink. Table 1 summarizes the comparison to other recent mm-scale transceivers.

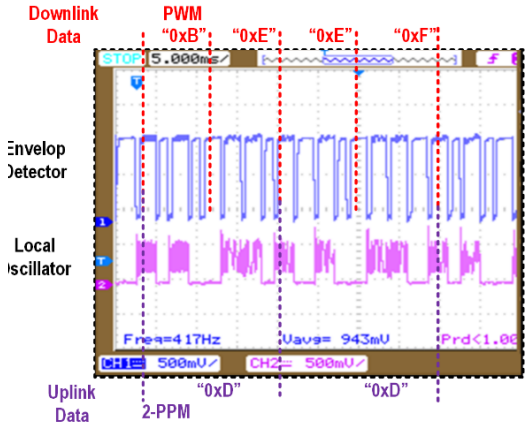

Fig. 8. Time domain measurement of envelop detector and local oscillator in the chip

V. Conclusion

In this paper, we demonstrated a 1×2.1×4 mm fully stand-alone radio system that integrates an antenna, battery, back-scatter transceiver, power management unit, and processor. The proposed system addresses key challenges for mm-scale transceivers such as the extremely constrained power and energy budget and antenna size, severe inband interference, and the need for crystal-less LO generation and timing synchronization. The proposed back-scatter transceiver synchronizes uplink timing and locks its LO frequency to the downlink signal. The proposed dual sideband self-coherent modulation together with a customized reader achieves 0 dB inband interference-to-signal power ratio tolerance. The fully integrated standalone mm-scale system with 1.28 µW active power achieves a 2.7 m/3.5 m communication range with a reader transmitting 23/31 dBm EIRP at a data rate of 250 bps.

References

[1] M. Tabesh, N. Dolatsha, A. Arbabian and A. M. Niknejad, "A Power-Harvesting Pad-Less Millimeter-Sized Radio," in IEEE Journal of Solid-State Circuits, vol. 50, no. 4, pp. 962-977, April 2015.

[2] B. Zhao, N. Kuo, B. Liu, Y. Li, L. Iotti and A. M. Niknejad, "A 5.8GHz power-harvesting 116µmx116µm "dielet" near-field radio with on-chip coil antenna," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 456-458.

[3] S. Pellerano, J. Alvarado and Y. Palaskas, "A mm-Wave Power-Harvesting RFID Tag in 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 8, pp. 1627-1637, Aug. 2010.

[4] H. Dagan et al., "A Low-Power Low-Cost 24 GHz RFID Tag With a C-Flash Based Embedded Memory," in IEEE Journal of Solid-State Circuits, vol. 49, no. 9, pp. 1942-1957, Sept. 2014.

[5] W. Biederman et al., "A Fully-Integrated, Miniaturized (0.125 mm²) 10.5 µW Wireless Neural Sensor," in IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 960-970, April 2013.

[6] V. Iyer, V. Talla, B. Kellogg, S. Gollakota, and J. R. Smith, "Inter-Technology Backscatter: Towards Internet Connectivity for Implanted Devices," in Proc. ACM SIGCOMM, Florianopolis, Brazil, 2016, pp. 1–14A.

[7] L. Chuo et al., "7.4 A 915MHz asymmetric radio using Q-enhanced amplifier for a fully integrated 3×3×3mm3wireless sensor node with 20m non-line-of-sight communication," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 132-133.