27.2 14.1-ENOB 184.9dB-FoM Capacitor-Array-Assisted Cascaded Charge-Injection SAR ADC

Kyojin Choo, Hyochan An, Dennis Sylvester, David Blaauw

University of Michigan, Ann Arbor, MI

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365863

IoT sensors are in rising demand and they often require low power, yet high precision measurements. Under constrained energy, Nyquist-rate SAR ADCs are typically used for readout as they are energy efficient and easy to multiplex across many sensors. However, achieving high precision (>14b) in SAR ADCs is challenging as all factors limiting performance (resolution, mismatch, and noise) must be simultaneously addressed with minimal energy impact. In this paper, we present an energy-efficient, capacitor-array-assisted cascaded charge-injection SAR ADC (c-ciSAR) with 17b nominal resolution (14.14b ENOB) that achieves a 184.9dB Schreier FoM (SFoM) and 4.32fJ/conv with a 1V supply in 0.18µm CMOS. The ADC deploys a combination of techniques to improve resolution, mismatch, and noise performance while remaining energy-efficient, namely: 1) hybridization of a capacitor-array DAC (CDAC) with charge-injection-cell (ci-cell) based DACs (ciDACs) to achieve high resolution and flexible programmability; 2) direct analog DAC mismatch compensation and repeated LSB decisions that leverage flexible programmability; 3) a noise-efficient charge-domain pre-amplifier for comparator (1.66 NEF) and SNR extended ci-cell; and 4) ±2·VDD signal sampling with pre-sampling MSB decision.

Flexible DAC operability is useful for overcoming noise and mismatch limits [1,2], yet previous demonstrations showed limited programmability, or consumed high power. In this paper, we propose an energy-efficient and highly programmable hybrid DAC that merges CDAC and ciDACs [3,4] (Fig. 27.2.1). A ci-cell outputs a packet of charge each time it is activated (by pulsing *activate*$_{p/n}$) and is reset after each activation, allowing it to be reused. Leveraging this reusability, a ciDAC becomes flexible, compact, and resilient against mismatch. Augmenting a CDAC (coarse 9b) with two stages of ciDAC (fine 4b ciDAC1 and finer 3b ciDAC2) results in a 16b c-ciDAC (Fig. 27.2.1). The two DAC structures complement each other in several ways. First, the large CDAC capacitance results in a high division ratio for the ciDACs through the bridge capacitor, achieving fine voltage resolution (25uV LSB), and conversely, relaxing the noise requirement for the ciDACs. Second, ciDAC gain control (by varying *bias*) provides an easy means to compensate gain errors. Third, and most important, the ciDACs' fine voltage steps, repeatable activation, and programmability enables direct (analog) detection and compensation of CDAC mismatch errors (unlike traditional digital calibration) and repeated LSB decisions to improve noise.

Figure 27.2.2 shows how ciDACs are used to detect and compensate CDAC mismatch error in the charge-domain. For mismatch compensation, each flip of a capacitor in the CDAC is accompanied by a predetermined number of ciDAC activations to cancel excess, or lack of, charge. For mismatch detection during calibration, each CDAC capacitor is flipped with all smaller binary weighted capacitors flipped to the other direction (+1 redundant CDAC LSB capacitor). The number of ci-cell activations is then swept to determine the value that yields zero net charge movement. These compensation values are stored into a look-up table and are called up during ADC operation. As ci-cells are reusable, the calibration process is achieved without extra DAC hardware. Also, as ci-cell operations are inherently accumulating, ciDACs control is simplified. The technique can reduce harmonic distortion to <15uV$_{rms}$ in measurement (target THD+N <57uV$_{rms}$).

Noise presents another critical performance bottleneck. To provide first-order reduction, the 9b differential CDAC is designed with 16fF unit capacitors (2×8pF as whole). Further improvements rely on suppressing noise from the comparator, resistors from CDAC, and charge-injection operation of the ciDAC. We also leverage ciDAC programmability to reduce comparator and resistor noise through repeated LSB decisions (RLD) (Fig. 27.2.2). Without incurring extra DAC hardware, this feature offers two accuracy benefits: 1) it implements redundant decisions to recover from decision errors from previous bits; 2) it averages comparator and resistor noise, making the DAC voltage level follow the statistical mean value of the noise-affected signal. Note that the sub-square-root nature of this noise reduction can quickly increase the energy needed to achieve >14b ENOB noise performance (<57uV$_{rms}$). Therefore, the technique is augmented with a highly energy-efficient comparator circuit.

For this circuit, we introduce an energy-efficient charge-domain preamplifier topology (Fig. 27.2.3). By setting the bias voltage such that the input pair operates in the sub-threshold region, the noise efficiency improves due to the increase in g_m/I_D from BJT-like operation. The capacitor current source implements this concept naturally, as it places the input pair in the sub-threshold regime as time progresses while initially providing high-g_m for gain. As an added benefit, the slow operation in the sub-threshold region filters out fast noise from the CDAC resistors. The input pair is relatively small (W/L = 16/0.5µm, each) to prevent non-linear gate capacitance and CDAC-state dependent kickback noise from distorting ADC results. Both the source and drain of the input transistors are reset to high voltage (VDD) to un-correlate the interface trap states for each decision. From simulation, when the preamplifier consumes 150fJ, its input-referred noise is 87uV$_{rms}$, which maps to an NEF of 1.36. Including 60fJ from the comparator (2.7 NEF), the complete comparator achieves 1.66 NEF, marking a ~1.6× improvement over the comparator alone. Comparator and resistor noise is suppressed to 17uV$_{rms}$ (estimated from measurement) with an optimal preamplifier bias setting and repeated LSB decisions (15 LSB decisions).

To reduce noise in the ciDAC itself, we developed an SNR *extended* ci-cell (Fig. 27.2.3). In ci-cells, SNR is determined by the ratio between the signal charge (∝ voltage swing on *i_s*) and 2·kTC noise charge. However, because the voltage swing is, in practice, limited to a fraction of VDD (~100mV) and the capacitor is just 22fF, the SNR of single ci-cell activation is ~40dB (~1% noise per ciDAC1 LSB). Hence, if there are many ci-cell activations (e.g., up to 600 activations in ciDAC1 for mismatch compensation) noise charge can accumulate and raise the noise floor (+18uV$_{rms}$). Hence, to improve the intrinsic SNR of single ci-cell activation, we increase the voltage swing by driving the other side of the internal capacitor against its natural (rising) flow using an inverter. As noise charge is still fixed at 2·kTC, SNR is boosted by ~4×.

To further improve the noise performance, we adopt ±2·VDD signal sampling [5]. However, this requires duplication of the CDAC, which increases area and energy, and also complicates mismatch compensation. Instead, we perform the MSB decision prior to the DAC sampling the input signal, as shown in Fig. 27.2.4. Then, the decision is quickly applied to offset the CDAC for ±2·VDD signal sampling without a duplicated CDAC. As signal bandwidths in IoT sensors are low, applying the MSB decision within a short time (1% of conversion time) bounds the error from signal change to be within a correctable range through redundancy (±4% FS, supports up to 1.27× Nyquist rate input).

Figure 27.2.5 shows the measured FFT result of the ADC at Nyquist rate. The SFDR with and without direct mismatch compensation exhibits >12dB difference. With repeated LSB decisions, THD+N is lowered to less than 2.1 LSB$_{rms}$ (<52uV$_{rms}$, including ~30uV$_{rms}$ input buffer noise). The ADC achieves 14.14b ENOB at Nyquist rate, translating to a SFoM of 184.95dB and a WFoM of 4.32fJ/conv (Fig. 27.2.6). The ADC has a higher SFoM than oversampling ADCs and the highest ENOB among high SFoM Nyquist-rate ADCs in the comparison table. Energy consumption is dominated by digital operations (>54%, based on simulation) and can be reduced in more advanced process nodes. Figure 27.2.7 provides the chip photograph.

References:

[1] T. Morie et al., "A 71dB-SNDR 50MS/s 4.2mW CMOS SAR ADC by SNR enhancement techniques utilizing noise," *ISSCC*, pp. 272-273, Feb. 2013.
[2] A. AlMarashli et al., "A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s," *IEEE JSSC*, vol. 53, no. 5, pp. 1493-1507, May 2018.
[3] K. D. Choo et al., "Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Application," *ISSCC*, pp. 96-98, Feb. 2019.
[4] K. D. Choo et al., "Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based-DAC", *ISSCC*, pp. 460-461, Feb. 2016.
[5] S. Hsieh and C. Hsieh, "A 0.4V 13b 270kS/s SAR-ISDM ADC with an Opamp-Less Time-Domain Integrator," *ISSCC*, pp. 240-241, Feb. 2018.
[6] X. Tang et al., "A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier," *ISSCC*, pp. 162-164, Feb. 2020.
[7] C.-C. Liu and M.-C. Huang, "A 0.46mW 5MHz-BW 79.7dB-SNDR Noise-Shaping SAR ADC with Dynamic-Amplifier-Based FIR-IIR Filter," *ISSCC*, pp. 466-467, Feb. 2017.
[8] J. Liu et al., "A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-Order Mismatch Error Shaping," *ISSCC*, pp. 158-160, Feb. 2020.
[9] M. Zhang et al., "A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques," *ISSCC*, pp. 66-67, Feb. 2019.
[10] T.-C. Hung et al., "A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme," *ISSCC*, pp. 256-258, Feb. 2020.
[11] Y. Chae et al., "A 6.3uW 20bit Incremental Zoom-ADC with 6 ppm INL and 1uV Offset," *IEEE JSSC*, vol. 48, no. 12, pp. 3019-3027, Dec. 2013.
[12] P. Harpe et al., "An Oversampled 12b/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR," *ISSCC*, pp. 194-195, Feb. 2014.
[13] A. ElShater et al., "A 10mW 16b 15MS/s Two-Step SAR ADC with 95dB DR Using Dual-Deadzone Ring-Amplifier," *ISSCC*, pp. 70-72, Feb. 2019.

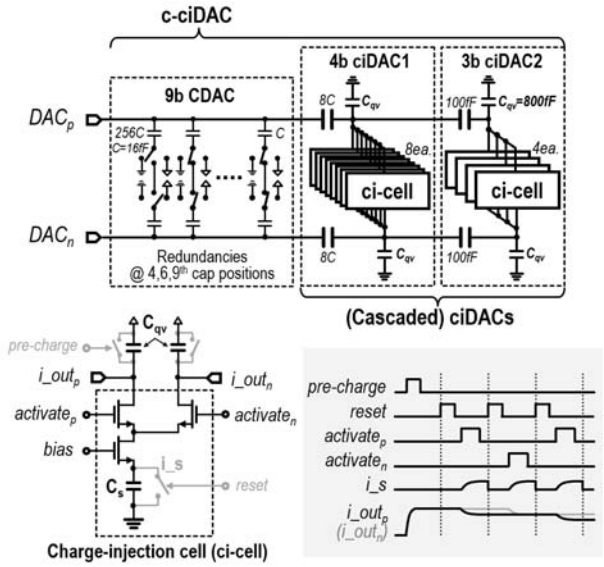

Figure 27.2.1: (Top) The proposed c-ciDAC structure, and (bottom) simplified charge-injection cell (ci-cell) and operation.

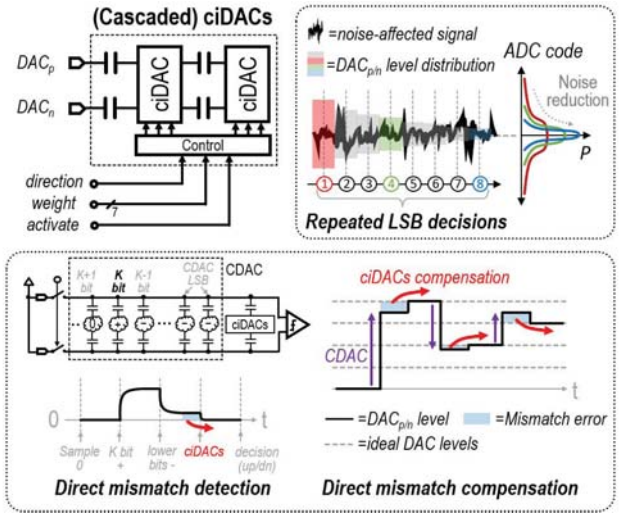

Figure 27.2.2: Cascaded ciDACs operation takes in three inputs (direction, weight, and activation pulse). It can easily be programmed to support direct (analog) mismatch detection/compensation and repeated LSB decisions without extra DAC hardware. Inherent accumulation of ci-cell operations further simplifies control.

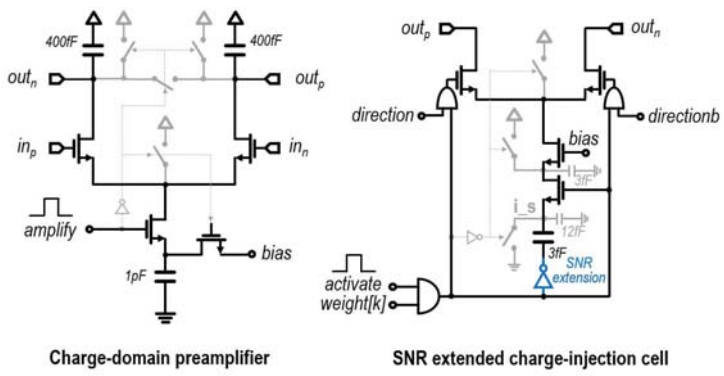

Figure 27.2.3: (Left) Energy-efficient charge-domain preamplifier, and (right) SNR-extended charge-injection cell.

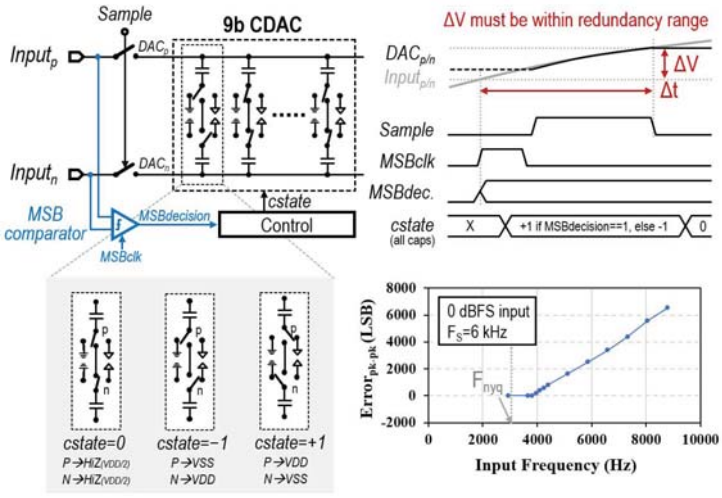

Figure 27.2.4: Pre-sampling MSB decision for ±2·VDD sampling. Δt between MSB decision and signal sampling is set to ~1% of the conversion time for ΔV to be within a correctable range through redundancy (±4%FS, correctable up to 1.27× Nyquist rate).

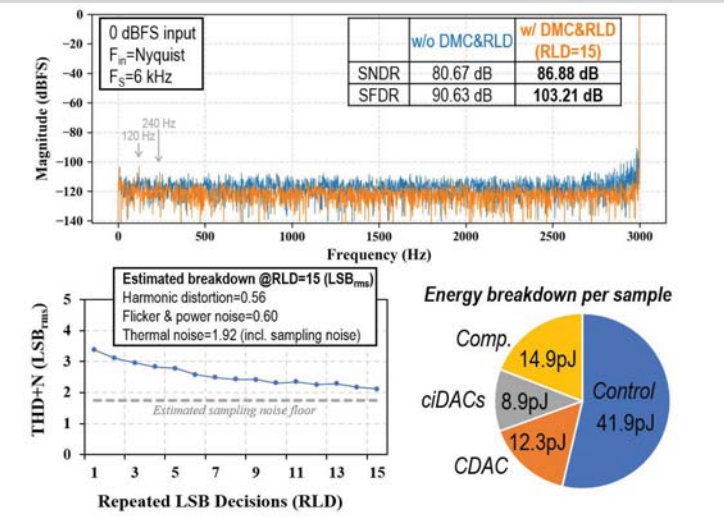

Figure 27.2.5: Measured FFT result with and without direct mismatch calibration (DMC) and repeated LSB decision (RLD) technique. With repeated LSB decision technique, THD+N approaches the sampling noise floor. Also, (simulated) energy breakdown by sub-block is shown at bottom right.

		This work	ISSCC 2020 [6]	ISSCC 2017 [7]	ISSCC 2020 [8]	ISSCC 2018 [5]	ISSCC 2018 [9]	ISSCC 2020 [10]
Structure		c-ciDAC SAR ADC	NS-SAR	NS-SAR	NS-SAR	SAR	Pipelined SAR	Pipelined SAR
Ov. / Nyq.		Nyquist	Oversampling			Nyquist		
Tech	nm	180	40	30	40	90	65	28
Resolution	bits	17	-	10	-	13	13	14
VDD	V	1.0	0.8/1.1	1.0	1.1	0.4	0.6	1.1
$F_{s,nyq}$ (2·BW)	kS/s	6.0	1250	10000	80	270	20000	100000
SNDR @Nyq.	dB	86.88	83.8	79.74	90.5	73.6	71.0	71.7
ENOB	bits	14.14	13.6	12.9	14.7	11.9	11.5	11.6
Power	uW	0.468	107.0	460	67.4	0.63	82.0	700
WFoM	fJ/conv	4.32	6.8	5.8	30.8	0.60	1.4	2.2
SFoM	dB	184.95	181.5	180.1	178.2	186.8	181.9	180.2
Core area	mm^2	0.348	0.037	0.0049	0.061	0.059	0.053	0.018

SFoM = SNDR + $10\cdot\log_{10}$(BW/Power), WFoM=Power/$F_{s,nyq}/2^{ENOB}$

Figure 27.2.6: Performance summary and comparison with state-of-the-art high-SFoM ADCs.

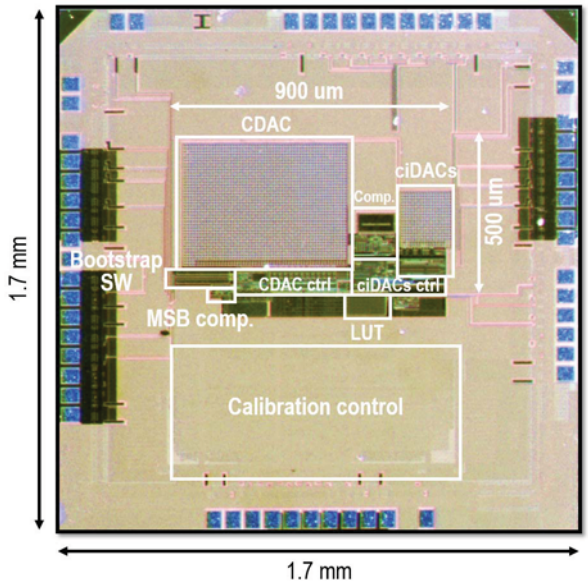

Figure 27.2.7: Chip photograph of the c-ciSAR ADC in 0.18µm CMOS.

978-1-7281-9549-0/21/$31.00 ©2021 IEEE