A 184nW, 121μg/√Hz Noise Floor Triaxial MEMS Accelerometer with Integrated CMOS Readout Circuit and Variation-Compensated High Voltage MEMS Biasing

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Abstract

We present a triaxial MEMS accelerometer readout circuit (RoC) with 40× signal gain using a high MEMS bias voltage, reducing power by eliminating the need for a chopped AFE chain. The proposed RoC achieves a 121μg/√Hz input referred noise and 1.5g dynamic range at 184nW per-axis power, while maintaining <1% non-linearity and a mechanical full-scale of >20 g, improving FoM by 15.6×.

Introduction and Proposed Approach

MEMS capacitive accelerometers are critical in IoT due to their miniaturized volume [1][7]. Prior RoCs [5][6] employ low noise amplifiers and input signal chopping to reduce thermal and flicker noise, respectively, and/or generate a feedback signal to the MEMS sensor to achieve higher acceleration sensitivity [2][3] (Fig. 1). However, the fundamental power/noise trade-off makes it difficult to achieve both < μW power and <5 mg input noise in these approaches.

Instead of reducing RoC noise (and subsequently increasing power), we propose raising the MEMS signal amplitude by increasing the MEMS bias voltage, thereby improving the power/noise trade-off and removing the need for power hungry chopping (Fig. 2). Further, at a high bias the effect from the electrostatic force reduces proof-mass stiffness and increases MEMS mechanical sensitivity. This increases the signal super-linearly with bias voltage, but reduces the proof-mass's dynamic range and risks electrostatic pull-in [8]. This is exacerbated by inherent MEMS mismatch from manufacturing variations. Hence, we also introduce a companion high voltage generation chip (HVC) designed to generate the MEMS bias voltages with high differential voltage precision. To raise the maximum bias voltage (and hence signal), HVC applies an automatically determined bias voltage skew to achieve post-fabrication electrostatic mismatch cancelation (EMC), maintaining linearity and dynamic range.

Circuit Implementation

Fig. 3 shows that the MEMS sensing element is modeled as a differential capacitor bridge created by the gaps between the proof-mass and fixed electrodes. We apply ± DC bias voltages (V_{B+} and V_{B-}) to the fixed electrodes, and a differential MEMS voltage signal (V_{IN+} and V_{IN-}) is generated once the capacitance changes with proof-mass displacement due to acceleration. This signal is amplified by the RoC to produce either a 1-bit signal in a 1.2V V_{DD} motion detection (MD) mode or a 2V V_{DD} full resolution analog output in full functionality (FF) mode. The RoC chip is eutecticly bonded to the MEMS sensing element to minimize signal loss due to interconnect parasitics. Since V_{IN+} and V_{IN-} are proportional to V_{B+} and V_{B-} (ignoring the MEMS sensitivity increase), the MEMS signal can be raised above the flicker and thermal noise floors by increasing bias voltage, eliminating the need for power hungry signal chopping and large amplifier bias currents. The low-noise amplifier (LNA) and programmable-gain amplifier (PGA) are carefully designed in terms of sizing and gain settings to mitigate added flicker noise due to the non-chopping signal path. LNA/PGA output common modes are shifted by auxiliary amplifiers to bias the input pairs for maximum dynamic range.

The HVC chip generates a fine-grained V_{B+} and V_{B-} pair to achieve electrostatic balance on the proof-mass. As shown in Fig. 4, V_{B+} and V_{B-} are generated with two Dickson charge pumps. V_{B+} is capacitively sampled and divided by 20 (due to comparator voltage limits), then compared with a reference voltage V_{CM} to provide feedback to control the charge pump operation. However, error on V_{CM} manifests as 20× larger on V_{B+}, so it only serves as a coarse control of the bias voltages. For fine control of ΔV_B ($|V_{B+}|$ - $|V_{B-}|$), which determines the intentional bias voltage skew on proof-mass and cancels out the electrostatic force mismatch due to MEMS fabrication or circuit non-ideality, we sample the average of V_{B+} and V_{B-} using capacitive charge sharing. Using a comparator, we then force V_{B-} to follow V_{B+} with an absolute voltage difference of ΔV_B. To generate a precise V_{CM} and ΔV_B, HVC first generates an internal bias voltage V_{2P0} [9], and then buffers it and applies it across a 128-step poly-resistor divider with ~35mV resolution and 44dB PSRR. Ripple on V_{B+} and V_{B-} could be 100s of mV due to charge pump operation and voltage sampling, impacting proof-mass displacement and inducing common-mode noise. We address this by separating the "clean" bias voltage nodes (CV_{B+}, CV_{B-}) from "dirty" ones (DV_{B+}, DV_{B-}) through a large-time-constant (~0.1s) RC network. Before sampling, DV_{B+} and DV_{B-} pre-charge the parasitic capacitors (phase Φ_2) to approximately the correct voltage, and then CV_{B+} and CV_{B-} are sampled with much reduced charge movement (phase Φ_3). This reduces ripple on CV_{B+}/CV_{B-}, and the voltage is further filtered with another RC network (for pull-in voltage spike protection) to generate final bias voltages $V_{B+/-}$.

Measurement Results

The RoC was fabricated in a MEMS-integrated 180nm CMOS process and the companion HVC in HVBCD 180nm. A shaker table (The Modal Shop Inc. 2075E) generates 3 axes accelerations, but only z-axis results are shown due to page constraints. RoC bandwidth is selected as 5−200Hz, targeting motion detection applications, and can be extended by changing RoC feedback resistor design. Fig. 5 shows measured HVC bias outputs (V_{B+}/V_{B-}) from cold startup until steady state, precisely suppressing ΔV_B within 0.1% of full scale. As the bias voltage ramps up, the output signal increases proportionally and stabilizes at 56dB SNDR in FF mode. At the same condition, MD mode detects input accelerations down to 3mg.

An important question is how to set the value of V_{B+} and V_{B-} to achieve maximum signal increase while maintaining sufficient MEMS dynamic range. Fig. 6 shows accelerometer sensitivity for all V_{B+}/V_{B-} combinations at >20V for a typical chip sample (#1), showing an optimal 1.2V ΔV_B. Maintaining ΔV_B=1.2V, we then increase V_{B+} along the red dotted line at zero g until the pull-in point (zero mechanical full-scale) and then back off from this point to guarantee > 20g peak-to-peak mechanical dynamic range (see also Fig. 9). Note that at > 20g the mechanical dynamic range greatly exceeds the accelerometer full-scale (±1.5g in FF mode and much lower in MD mode) and does not limit accelerometer performance. We tested 30 samples from 5 different wafers in this way and Fig. 7 shows the resulting distribution of ΔV_B. Fig. 8 shows the distribution of the resulting sensitivity in three cases where: 1) EMC is optimally applied to each sample (red); 2) a batch level EMC ΔV_B and back-off value are used, reducing testing to a minimum (blue); 3) no EMC is applied (black). Optimal EMC yields the highest mean sensitivity of 784mV/g (1.65× increase over no EMC). Batch level EMC incurs a sensitivity penalty of 24% at 596mV/g from optimal EMC but remains 25% better than no EMC. Finally, to characterize accelerometer reliability in case a large acceleration causes pull-in, we also performed a long-term, repeated pull-in test showing no degradation in accelerometer functionality after >10K pull-ins.

Compared to a MEMS with a typical bias of 4V, the proposed RoC achieves 40× gain in sensitivity (optimal EMC) at 775mV/g output sensitivity and 0.6% linearity error. It also achieves 121μg/√Hz and 165μg/√Hz noise floors for FF and MD modes, while consuming 110nW and 22.4nW, respectively. Dividing the 223nW HVC power across the triaxial MEMS units, the RoC and HVC chips consume a total of 184nW in FF mode and 96nW in MD mode per axis. Table 1 compares the accelerometer performance with prior work, showing a 15.6× FOM (Noise × Power / √BW) improvement over prior art.

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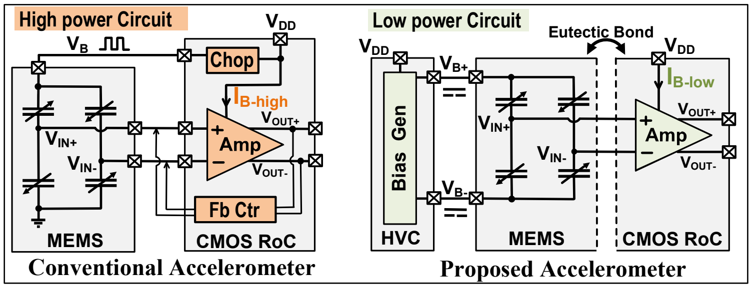


Fig. 1. System diagram of a conventional (left) and proposed (right) MEMS accelerometer.

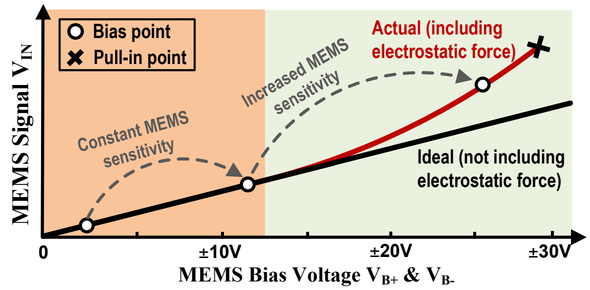


Fig. 2. MEMS signal amplitude with different bias voltages.

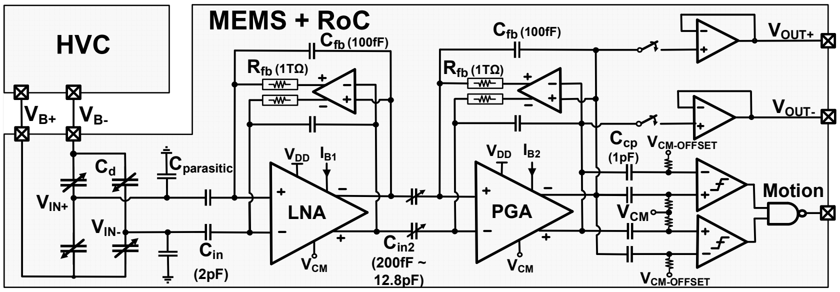
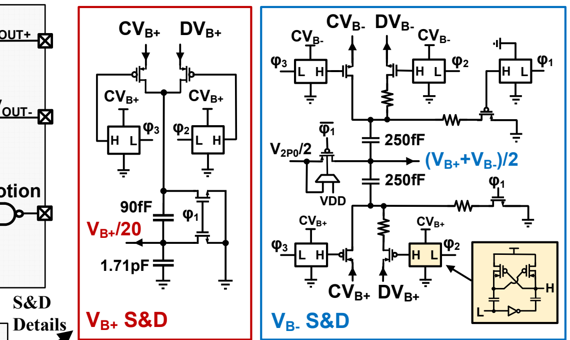


Fig. 3. MEMS & RoC Circuit with transistor-level schematic for the LNA/PGA.



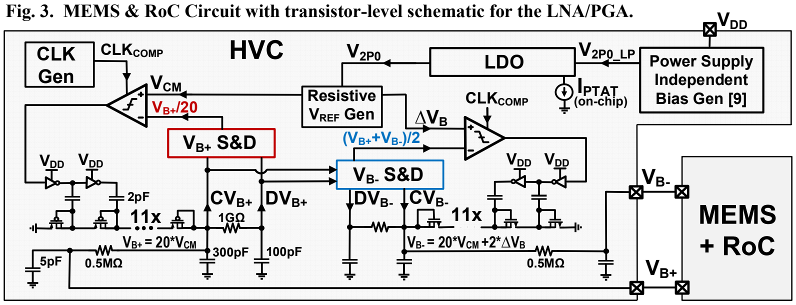


Fig. 4. HVC schematic with transistor-level circuit for the capacitive sampler and divider (S&D).

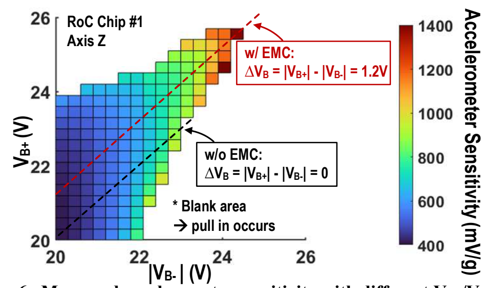


Fig. 6. Measured accelerometer sensitivity with different V_{B+}/V_{B-}.

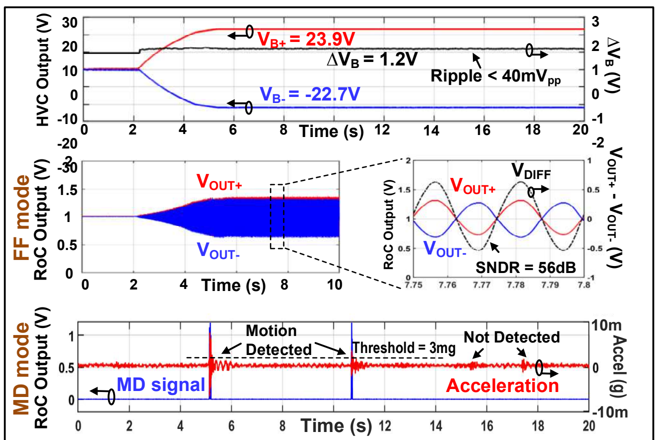


Fig. 5. Measured HVC and RoC transient waveform in MD and FF mode.

Table. 1. Performance summary and Comparison with prior works.

	This work		[2] JSSC'15	[3] JSSC'12	[5] JSSC'17	[6] VLSI'18	[4] ADXL362
	MD Mode	FF Mode					
RoC Technology	0.18μm		0.5μm	0.35μm	0.35μm	0.18μm	-
CMOS chip area (mm^2)	2.88 (RoC) 4.55 (HVC)		7.80	6.66	6.00	1.14	-
Number of Axis	3		1	1	1	1	3
Integrated MEMS	Yes		No	No	No	No	Yes
Sensing Mechanism	Capacitive		Capacitive	Capacitive	Silicon oscillating	Capacitive	Capacitive
Input Full-scale (g)	N/A	± 1.5	± 1.2	± 1.15	± 20	± 8	± 8
Bandwidth (Hz)	200 *		300	200	40 **	50	50
Input referred noise floor (μg/√Hz)	165	121	0.2	2	0.4	970	550
Supply voltage (V)	1.2(RoC) 2.4 (HVC)	2 (RoC) 2.4(HVC)	7.0	3.6	1.5	1.0	2.0
Power Per Axis (μW)	0.096 ***	0.184 ***	23000	3600	4370	0.181	1.2
FoM **** (μW·μg/Hz)	1.13	1.59	266	509	276	24.8	93.3

* High-Pass corner is 5Hz but could be extended to lower frequency if needed.
** Estimated with the noise spectrum figure. *** Including the power consumed by HVC for generating high voltage biases. **** The same FoM as in [2], which is Power × Noise floor ÷ √ BW.

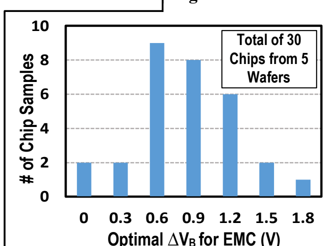


Fig. 7. Distribution of optimal ΔV_B.

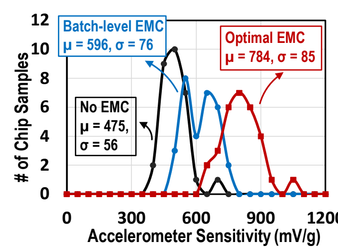


Fig. 8. Distribution of accel sensitivity.

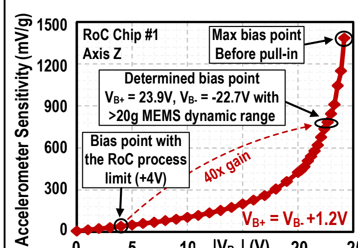


Fig. 9. Measured sensitivity with $1.2V\Delta V_B$.

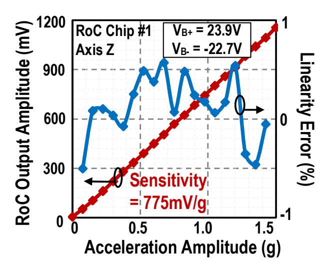


Fig. 10. Measured accelerometer linearity within ±1.5g full scale.

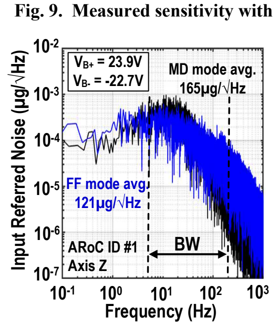


Fig. 11. Measured RoC input-referred noise in MD and FF mode.

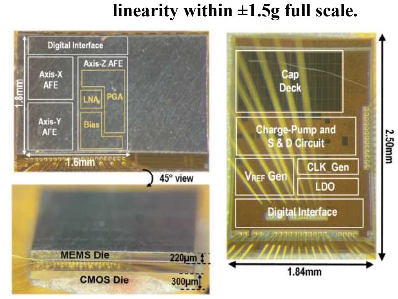


Fig. 12. Die photo of The RoC (left) and HVC (right) chip.