A 192 nW 0.02 Hz High Pass Corner Acoustic Analog Front-End with Automatic Saturation Detection and Recovery

Rohit Rothe, Minchang Cho, Kyojin Choo, Seokhyeon Jeong, Dennis Sylvester, David Blaauw
University of Michigan, Ann Arbor (Email: rohitro@umich.edu)

Abstract

We present an acoustic analog front-end with a 100Ω feedback resistance that is robust to PT variation (1.8× deviation across 40 to 80°C and 0.035× σ/µ across 16 measured samples) and achieves a 3.3× reduction in input referred noise (IRN). It eliminates an input frequency and phase dependent systematic offset introduced by a similar previous technique [5] and introduces automatic saturation detection and feedback resistance modulation for fast amplifier restabilization, yielding 10× improvement in artifact recovery time. The technique was implemented in a 192 nW LNA + PGA + ADC chain.

Introduction

IoT sensors are increasingly common, and their analog front-ends require very low power, making capacitively coupled amplifier topologies a popular choice (Fig. 1). These amplifiers typically rely on a feedback resistor to provide a common-mode input voltage and input offset cancellation. For applications with in-band frequencies in the Hz range, a major design challenge is to provide a sufficiently low high-pass (HP) corner for the signal path. In addition, the feedback resistor noise is low-pass filtered at this same corner, making it advantageous to further lower the corner to 10 – 100 mHz. This can achieve a lower input referred noise (IRN) or trade resistor noise for higher thermal amplifier-noise and lower power. Given the frequent use of small feedback capacitors (~10 fF) to reduce input impedance and increase amplifier bandwidth, feedback resistances in the 10s of Ω are often required. This high resistance should be achieved concurrently with: 1) a process and temperature (PT) stable corner, 2) small area (eliminating standard passive resistors) and, importantly, 3) unity feedback gain at DC since attenuation at DC increases input offset at the output. Achieving these goals has garnered significant attention recently [4-6] but a robust technique remains elusive. Further, what is often overlooked is that such low corner frequencies yield extremely long stabilization times and slow recovery from amplifier saturation (e.g., in audio applications from wind or abrupt pressure differentials).

The most common feedback resistor approach uses pseudo-resistors [1] that suffer from very high PT variation (Fig. 1). Capacitive ladder [2] and duty-cycled resistors [3] have not demonstrated Ω resistances, while the latter requires precise pulse length generation. Recently, a switched resistor ladder [4] and switched capacitor technique [5] achieve Ω resistances but [4] attenuates feedback at DC, while [5] has phase dependent sampling bias, both increasing output offset.

Proposed Delta Sigma Modulated Feedback Injection

The proposed structure leverages a “sample and average” feedback structure [5] that achieves Ω resistance in a PT robust manner. The structure first generates an averaged output voltage Voa (Fig. 1) using a sampling clock fs, higher than the signal bandwidth, and then injects this voltage at the amplifier input using a small capacitor Co with feedback frequency fs that is below the signal bandwidth. We observe, however, that if the input frequency fi is an integer multiple of fs, the two voltages sampled on Co will be 180° out of phase, leading to a consistent, phase-dependent output offset (Fig. 1) of up to 157 mV in our measured results.

To address this issue, we augment the frequency domain averaging of the 1st stage of the feedback structure with time domain averaging in the 2nd stage. We generate two feedback frequencies fi and fs using a counter-based frequency divider, clocked by fi, and with a period-time resolution of fs (1/16k = 62.5 us) by counting to x1 and x2, respectively (Fig. 3). We then select between these two frequencies using a 1-bit 2nd-order delta sigma modulator (DSM). Hence, the injection frequency jumps between fi and fs with the DSM ensuring the desired feedback frequency is achieved on average. Since the DSM is clocked by fi (~16 Hz) it is implemented using thick-oxide, HVT devices to reduce its leakage-dominated power (< 22 nW, simulated). By selecting x1 and x2 as co-prime, we guarantee that the minimum frequency that exhibits constant phase sampling is fi. This means that multiplicity between fi and any input signal frequency within the amplifier bandwidth is infeasible (fi > amplifier bandwidth). Hence, the sampled and injected values of Voa and VS will be properly averaged in time over multiple cycles, thereby eliminating the source of the offset.

Proposed Automatic Saturation Detection and Recovery

The low high-pass corner results in long amplifier stabilization times (~sec), making it vulnerable to abrupt, in-band pressure changes that saturate operation, e.g., wind or door closures. To detect amplifier saturation we compare VS and Voa, which are low pass versions of the differential output and already available in the feedback structure — this removes the danger of false triggering when directly observing amplifier outputs (Fig. 3). During saturation, these nodes drift from common mode to opposite rails. Since they are low-pass filtered, we use low bandwidth comparators to reduce power. The comparators have an offset of Voa (40 mV in our design) and check for Voa > Vao + Vao and Voa > Vao + Vao. When a comparator triggers (two comparators per LNA, PGA), the feedback frequency clock divider switches to a high frequency mode (programmable from 250 Hz – 4 kHz here) and rapidly drives the amplifier back to stable operation as soon as the artifact ends. The same mechanism enables fast initial startup, greatly reducing amplifier initialization time, important in duty-cycled applications.

The LNA OTA uses an inverter-based cascode topology (Fig. 2). Auxiliary amplifiers in the DC-servo loops shift output common modes to an optimal bias point for each input pair, maximizing output range.

Measurements

Fig. 4 shows measured PGA output offset vs. input phase with and without DSM at 32 Hz fs with a fixed 16 Hz fi. DSM reduces phase dependent offset by ~90× from 157 mV to 1.7 mV and worst-case offset from 89.4 mV to 12.7 mV. We also measured transfer curves with and without DSM and confirmed that the HP corner is unaffected. Fig. 5 shows measured operation during saturation detection and recovery for a typical chip under two scenarios. In the first, we play a loud (75 dB A SPL) 200 Hz tone while in the second we open the acoustic chamber door, generating a low frequency in-band pressure wave. Recovery time is reduced by ~10× with diminishing returns on stabilization speed for fast feedback frequencies higher than 1 kHz.

Fig. 11 shows the 180° CMOS die photo and system design, consisting of a MEMS microphone, wire-bonded to the LNA, PGA, and ADC. Fig. 8 shows acoustically measured frequency response for 9 tones using a plane-wave tube. By reducing the corner from 40 Hz (typical low-end of audio bandwidth) to 20 mHz, integrated IRN reduces by 3.3× from 90 to 27 μV (Fig. 6). The noise spectrum shows spikes at the fi tone (16 kHz) and its harmonics, which are aliased to a single ADC frequency bin as the ADC clock is synchronized with fi.

Fig. 7 shows measured LNA transfer curves from ~20°C to 80°C. The total 1.8× variation in feedback resistance across temperature is a major improvement over the 271× variation observed in our baseline pseudo-resistor implementation. Measured LNA core power and clock generation power are 75.6 nW and 92.4 nW, respectively. The LNA NEF is 2.6 (accounting for 50% of clocking power as it is shared by the LNA and PGA). Table 1 provides results for 16 measured die. This method provides a reliable Ω-level resistance without attenuation in the feedback path, is robust across temperature and process, and can detect amplifier saturation and enable rapid stabilization recovery.

References

Fig. 1. Input signal frequency & phase dependent offset in [5] (right) and proposed technique (top left).

Fig. 3. Feedback-clock generation with saturation detection and fast restabilization and DSM for phase dependent offset elimination.

Table 1. Comparison Table and Performance Summary.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>180</td>
</tr>
<tr>
<td>Application</td>
<td>Acoustic Sensing</td>
<td>Biomimics</td>
<td>Acoustic Sensing</td>
<td>Acoustic Sensing</td>
</tr>
</tbody>
</table>

**Fig. 4. Measured PGA offset as a function of input signal phase with proposed DSM time averaging ON and OFF (f_s = 32Hz).**

**Fig. 7. Temperature Stability.**

**Fig. 8. Acoustically measured freq response (input = 80 dBFSPL).**

**Fig. 9. Plane-Wave Tube used to measure acoustic frequency response.**

**Fig. 10. Analog Front-end noise sensitivity level test.**

**Fig. 11. Die Photo. Chip integrated using chip on board (COB) with MEMS microphone.**

* Clock generation power split equally between LNA & PGA. ** Timable HP corner (measurement of lower limit was limited by instrument). * Calculated from measured data. ** DSM OFF measurement is like implementation in [5]. * * Saturation detection & recovery not present - using slowest HP corner to calculate the stabilization time.