A 192 nW 0.02 Hz High Pass Corner Acoustic Analog Front-End with Automatic Saturation Detection and Recovery

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Abstract

We present an acoustic analog front-end with a 100TΩ feedback resistance that is robust to PT variation (1.8× deviation across –40 to 80°C and 0.035× σ/μ across 16 measured samples) and achieves a 3.3× reduction in input referred noise (IRN). It eliminates an input frequency and phase dependent systematic offset introduced by a similar previous technique [5] and introduces automatic saturation detection and feedback resistance modulation for fast amplifier restabilization, yielding 10× improvement in artifact recovery time. The technique was implemented in a 192 nW LNA + PGA + ADC chain.

Introduction

IoT sensors are increasingly common, and their analog front-ends require very low power, making capacitively coupled amplifier topologies a popular choice (Fig. 1). These amplifiers typically rely on a feedback resistor to provide a common-mode input voltage and input offset cancellation. For applications with in-band frequencies in the Hz range, a major design challenge is to provide a sufficiently low high-pass (HP) corner for the signal path. In addition, the feedback resistor noise is low-pass filtered at this same corner, making it advantageous to further lower the corner to $10 - 100$ mHz. This can achieve a lower input referred noise (IRN) or trade resistor noise for higher thermal amplifier-noise and lower power. Given the frequent use of small feedback capacitors (~10 fF) to reduce input impedance and increase amplifier bandwidth, feedback resistances in the 10s of TΩ are often required.

This high resistance should be achieved concurrently with: 1) a process and temperature (PT) stable corner, 2) small area (eliminating standard passive resistors) and, importantly, 3) unity feedback gain at DC since attenuation at DC increases input offset at the output. Achieving these goals has garnered significant attention recently [4-6] but a robust technique remains elusive. Further, what is often overlooked is that such low corner frequencies yield extremely long stabilization times and slow recovery from amplifier saturation (e.g., in audio applications from wind or abrupt pressure differentials).

The most common feedback resistor approach uses pseudo-resistors [1] that suffer from very high PT variation (Fig. 1). Capacitive ladder [2] and duty-cycled resistors [3] have not demonstrated TΩ resistances, while the latter requires precise pulse length generation. Recently, a switched resistor ladder [4] and switched capacitor technique [5] achieve TΩ resistances but [4] attenuates feedback at DC, while [5] has phase dependent sampling bias, both increasing output offset.

Proposed Delta Sigma Modulated Feedback Injection

The proposed structure leverages a "sample and average" feedback structure [5] that achieves TΩ resistance in a PT robust manner. The structure first generates an averaged output voltage V_B (Fig. 1) using a sampling clock f_s, higher than the signal bandwidth, and then injects this voltage at the amplifier input using a small capacitor C_c with feedback frequency f_b that is below the signal bandwidth. We observe, however, that if the input frequency f_{in} is an integer multiple of f_b, the two voltages sampled on C_c will be 180° out of phase, leading to a consistent, phase-dependent output offset (Fig. 1) of up to 157 mV in our measured results.

To address this issue, we augment the frequency domain averaging of the 1st stage of the feedback structure with *time domain* averaging in the 2nd stage. We generate two feedback frequencies f_{b1} and f_{b2} using a counter-based frequency divider, clocked by f_s and with a time-period resolution of f_s ($1/16k = 62.5$ us) by counting to x_1 and x_2, respectively (Fig. 3). We then select between these two frequencies using a 1-bit 2nd-order delta sigma modulator (DSM). Hence, the injection frequency jumps between f_{b1} and f_{b2} with the DSM ensuring the desired feedback frequency is achieved on average. Since the DSM is clocked by f_b (~16 Hz) it is implemented using thick-oxide, HVT devices to reduce its leakage-dominated power (< 22 nW, simulated). By selecting x_1 and x_2

as co-prime, we guarantee that the minimum frequency that exhibits constant phase sampling is f_s. This means that multiplicity between f_b and *any* input signal frequency within the amplifier bandwidth is infeasible (f_s > amplifier bandwidth). Hence, the sampled and injected values of V_{BP} and V_{BN} are properly averaged in time over multiple cycles, thereby eliminating the source of the offset.

Proposed Automatic Saturation Detection and Recovery

The low high-pass corner results in long amplifier stabilization times (~sec), making it vulnerable to abrupt, in-band pressure changes that saturate operation, e.g., wind or door closures. To detect amplifier saturation we compare V_{BP} and V_{BN}, which are low pass versions of the differential output and already available in the feedback structure – this removes the danger of false triggering when directly observing amplifier outputs (Fig. 3). During saturation, these nodes drift from common mode to opposite rails. Since they are low-pass filtered, we use low bandwidth comparators to reduce power. The comparators have an offset of V_{th} (140 mV in our design) and check for $V_{BP} > V_{BN} + V_{th}$ and $V_{BN} > V_{BP} + V_{th}$. When a comparator triggers (two comparators per LNA, PGA), the feedback frequency clock divider switches to a high frequency mode (programmable from 250 Hz – 4 kHz here) and rapidly drives the amplifier back to stable operation as soon as the artifact ends. The same mechanism enables fast initial startup, greatly reducing amplifier initialization time, important in duty-cycled applications.

The LNA OTA uses an inverter-based cascode topology (Fig. 2). Auxiliary amplifiers in the DC-servo loops shift output common modes to an optimal bias point for each input pair, maximizing output range.

Measurements

Fig. 4 shows measured PGA output offset vs. input phase with and without DSM at 32 Hz f_{in} with a fixed 16 Hz f_b. DSM reduces phase dependent offset by ~90× from 157 mV to 1.7 mV and worst-case offset from 89.4 mV to 12.7 mV. We also measured transfer curves with and without DSM and confirmed that the HP corner is unaffected.

Fig. 5 shows measured operation during saturation detection and recovery for a typical chip under two scenarios. In the first, we play a loud (75 dBA SPL) 200 Hz tone while in the second we open the acoustic chamber door, generating a low frequency in-band pressure wave. Recovery time is reduced by ~10× with diminishing returns on stabilization speed for fast feedback frequencies higher than 1 kHz.

Fig. 11 shows the 180nm CMOS die photo and system design, consisting of a MEMS microphone, wire-bonded to the LNA, PGA, and ADC. Fig. 8 shows acoustically measured frequency response for 9 tones using a plane-wave tube. By reducing the corner from 40 Hz (typical low-end of audio bandwidth) to 20 mHz, integrated IRN reduces by 3.3× from 90 to 27 uV$_{rms}$ (Fig. 6). The noise spectrum shows spikes at the f_s tone (16 kHz) and its harmonics, which are aliased to a single ADC frequency bin as the ADC clock is synchronized with f_s.

Fig. 7 shows measured LNA transfer curves from $-20°$C to $80°$C. The total 1.8× variation in feedback resistance across temperature is a major improvement over the 271× variation observed in our baseline pseudo-resistor implementation. Measured LNA core power and clock generation power are 75.6 nW and 92.4 nW, respectively. The LNA NEF is 2.6 (accounting for 50% of clocking power as it is shared by the LNA and PGA). Table 1 provides results for 16 measured die. This method provides a reliable TΩ-level resistance without attenuation in the feedback path, is robust across temperature and process, and can detect amplifier saturation and enable rapid stabilization recovery.

References

[1] D. Djekic *et al.*, *JSSC*, 2018. [2] N. Verma *et al.*, *JSSC*, 2010.
[3] H. Chandrakumar *et al.*, *ISSCC*, 2017.[4] X. Meng *et al.*, *ISCAS*, 2014.
[5] R. Rothe *et al.*, *VLSI*, 2020. [6] P. Harpe *et al.*, *JSSC*, 2015.
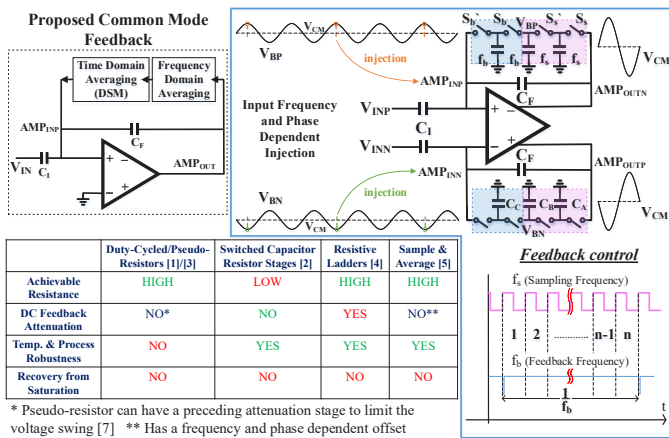[7] C. Deepu *et al.*, *JSSC*, 2015.

Proposed Common Mode Feedback

Fig. 1. Input signal frequency & phase dependent offset in [5] (right) and proposed technique (top left).

	Duty-Cycled/Pseudo-Resistors [1]/[3]	Switched Capacitor Resistor Stages [2]	Resistive Ladders [4]	Sample & Average [5]
Achievable Resistance	HIGH	LOW	HIGH	HIGH
DC Feedback Attenuation	NO*	NO	YES	NO**
Temp. & Process Robustness	NO	YES	YES	YES
Recovery from Saturation	NO	NO	NO	NO

* Pseudo-resistor can have a preceding attenuation stage to limit the voltage swing [7] ** Has a frequency and phase dependent offset
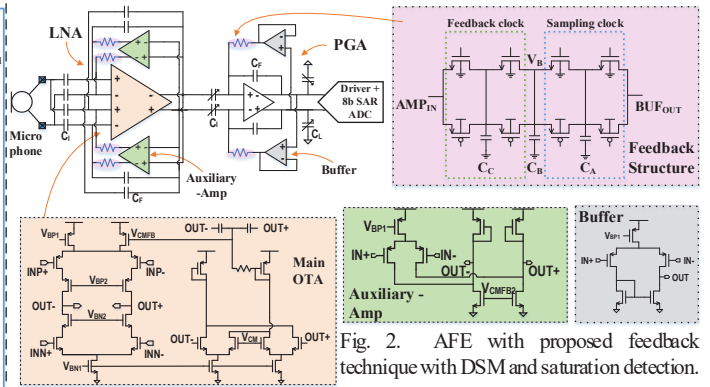
Fig. 2. AFE with proposed feedback technique with DSM and saturation detection.
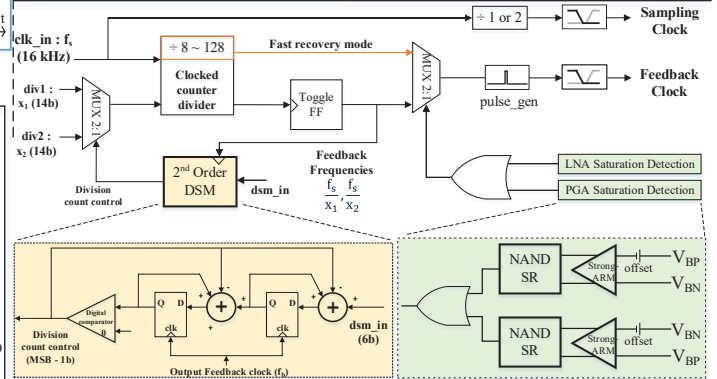
Fig. 3. Feedback-clock generation with saturation detection and fast restabilization and DSM for phase dependent offset elimination.
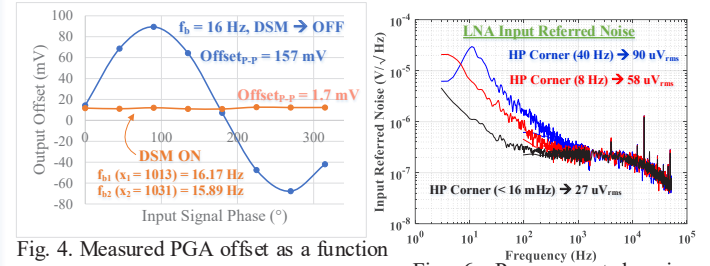
Fig. 4. Measured PGA offset as a function of input signal phase with proposed DSM time averaging ON and OFF (f_{in} = 32Hz).

Fig. 5. Fast recovery from loud tone and pressure wave.

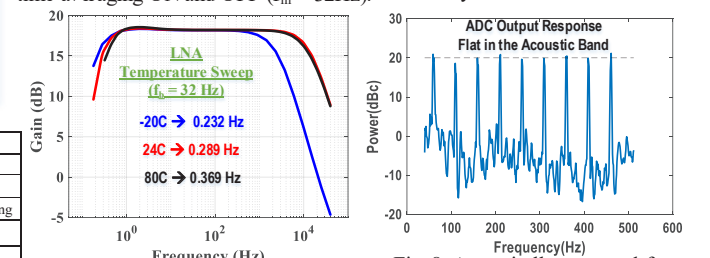Fig. 6. Power spectral noise density for LNA with different f_b.
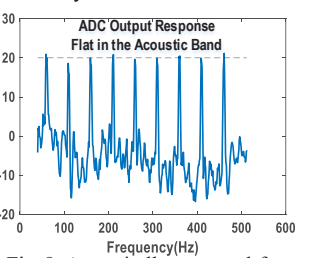
Fig. 7. Temperature Stability.

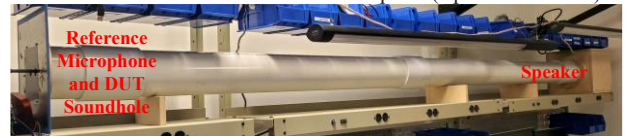Fig. 8. Acoustically measured freq. response (input = 80 dBcSPL).

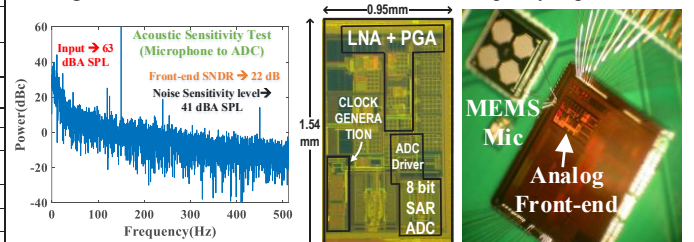Fig. 9. Plane-Wave Tube used to measure acoustic frequency response.

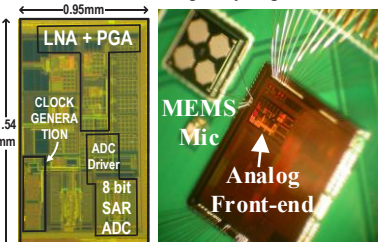Fig. 10. Analog Front-end noise sensitivity level test.

Fig. 11. Die Photo, Chip integrated using chip on board (COB) with MEMS microphone.

Table. 1. Comparison Table and Performance Summary.

Parameter	This Work		ISCAS'14 [4]	VLSI'20 [5]	JSSC'15 [6]
	LNA	LNA + PGA			
Technology (nm)	180		180	180	180
Application	Acoustic Sensing		Biosensors	Acoustic Sensing	Acoustic Sensing
DC Common Mode Feedback					
Feedback Technique	DSM enabled feedback injection		Switched Capacitor Ladder	Capacitive sample & average	DC Servo Loop
Effective Resistance	0.34 – 100 TΩ *²		0.11 – 21.2 TΩ	0.43 – 108 TΩ	106 GΩ
HP Corner	0.02 – 5 Hz *²		0.30 Hz – 60 Hz	0.016 – 4 Hz	1.5 Hz
HP Corner var.: -40°C to 80°C	1.8x		N/A	1.2x	N/A
HP Corner var.: chip to chip (σ/μ)	0.035 (16 chips measured)		N/A	0.041	N/A
Nominal Output Offset	35 mV (16 chips average)		N/A	N/A	N/A
Phase Dependent Offset	DSM OFF → 157 mV *⁴ DSM ON → 1.7 mV		N/A	N/A	N/A
Stabilization Time	0.27 s		3.33 s *⁵	62.5 s *⁵	0.66 s *⁵
Amplifier					
Power	119 nW *¹	186.2 nW	1.2 μW	101 nW	1 nW
Supply Voltage	1.4 V		1.5 V	1.4 V	0.6 V
Input Referred Noise	27.3 μVrms (till 16 kHz)	22.3 μVrms (till 4 kHz)	17.8 μVrms *³	26.1 μVrms (till 14.6 kHz)	26 μVrms (till 370 Hz)
Bandwidth	13.9 kHz	4.2–7.8 kHz	270 Hz	10.2 kHz	370 Hz
Gain	18.1 dB	18.1 – 28.2 dB	36.7 dB	18.3 dB	32 dB
NEF	2.6	5.0	37.3 *³	2.7	2.1

*¹ Clock generation power split equally between LNA & PGA, *² Tunable HP corner (measurement of lower limit was limited by instrument), *³ Calculated from measured data, *⁴ DSM OFF measurement is like implementation in [5], *⁵ Saturation detection & recovery not present – using slowest HP corner to calculate the stabilization time