An Analog-Assisted Digital LDO With Single Subthreshold Output pMOS Achieving 1.44-fs FOM

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***Abstract*—This letter describes an analog-assisted digital LDO that cascades a conventional digital LDO structure with a single, large output pMOS biased in subthreshold to enable fast response to output voltage droop. By digitally controlling the gate voltage of the output pMOS, the operating regime of the output transistor is decoupled from the input voltage. In addition, a 2-pF capacitor between the output voltage and the gate of the output pMOS creates a high-pass path to boost the output current when voltage droops occur. The proposed design is fabricated in 28-nm CMOS, and it enables a uniform transient response over an input voltage range of 0.5−0.9 V. The measured voltage droop when load current changes from 10 to 60 mA (1-ns edge time) is 110 mV at input voltages of both 0.5 and 0.9 V, resulting in a speed FOM of 1.44 fs.**

***Index Terms*—Analog-assisted (AA), digital LDO, fast transient response, subthreshold.**

I. Introduction

Digital low-dropout regulators (DLDOs) are popular due to their process scalability and low-voltage operation [1], [2]. Conventional DLDOs [1] regulate output voltage by digitally changing the number of "on" output switches at the rate of the sampling clock frequency. During a load step, the current supplied by the output switches can be boosted in two ways: 1) drain current of each switch rises due to the $|V_{DS}|$ increase associated with the voltage droop on the output voltage and 2) the number of "on" switches increases. These two ways are limited by the operating regime of the "on" switches and the sampling clock frequency of the digital control loop, respectively. For modern high-performance mobile applications with rapid power mode transitions (e.g., 10 s of mA/ns), conventional DLDOs require multi-GHz sampling rates and nF-range stabilizing output capacitors to reduce voltage droop [3], incurring large power and area overheads. Recently, analog-assisted (AA) DLDOs [4]–[6] were introduced to circumvent this tradeoff between power or output capacitance and transient response. AA-DLDOs augment a slow digital control loop with a high-speed, high-pass analog loop that improves transient response while retaining low-power consumption.

One type of AA-DLDO uses a droop detector [6] that is built with standard logic cells to trigger the high-speed path, and the logic threshold and delay related to this path dictate the transient response. At low input voltage (V_{IN}), the transient response of this configuration degrades compared to its response at high V_{IN} due to the increased droop detector delay. The other type of AA-DLDO adds an analog high-pass path [4] to the conventional digital loop as shown in Fig. 1. It couples the voltage droop on V_{OUT} to the gate of the output transistors ($|V_{GS}|$), rapidly boosting output current when V_{OUT} drops. Because "on" output transistors/switches have $|V_{GS}| = V_{IN}$, the amount of the boosted output current is highly sensitive to V_{IN}. At high input voltages (with stronger inversion of output transistors, or larger $|V_{GS}| - |V_{TH}|$ before the load step), these designs suffer from significantly slower response. To address these issues, we propose a new AA-DLDO topology that provides a fast transient response across an input voltage range of 0.5–0.9 V.

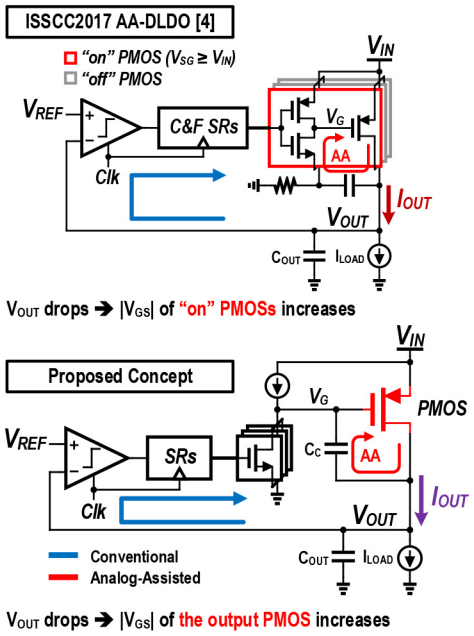

Fig. 1. Proposed concept of AA-DLDO with single-output pMOS.

Instead of digitally modulating the number of output devices, our approach digitally controls the bias condition of a single large output device as depicted in Fig. 1. The AA loop with a coupling capacitor always acts on a single large transistor. This output stage configuration is conceptually similar to charge-pump-based LDOs [7], [8], but the proposed architecture and the design consideration of the output stage are different. First, the proposed high-level design concept is to cascade a slow conventional digital LDO structure with an analog output stage with inherently fast response to voltage droop, which combines to provide both high gain and fast transient response across a wide range of input voltage. Second, the proposed design combines a bias current and an array of digitally controlled pull-down switches to set the gate voltage of the output pMOS, and the digital loop controls the number of the "on" switches instead of the "on" time of the charge-pumps in [7] and [8]. These two points above make the proposed architecture compatible with existing digital control schemes in DLDOs, and more complicated digital controls could be introduced to further improve the performances, which is an advantage over the charge-pump-based LDOs [7], [8]. Third, to the best of our knowledge, we are the first to bring up the observations

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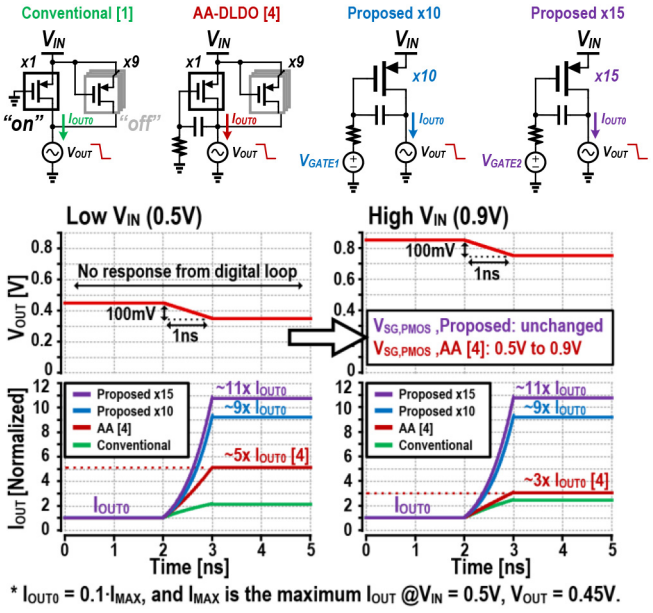

Fig. 2. Simulated dI_{OUT}/dV_{OUT} for low and high V_{IN}.

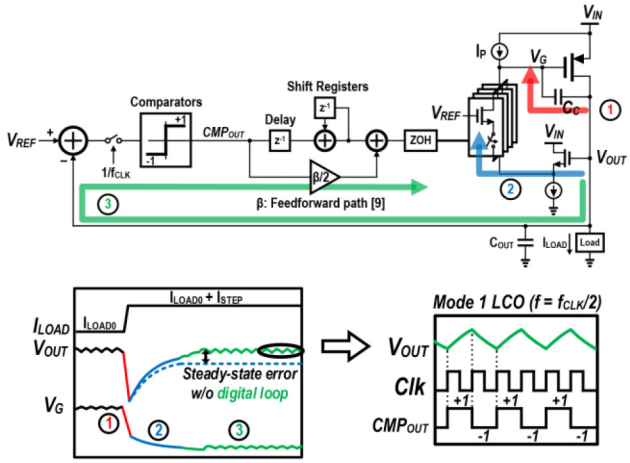

Fig. 3. Architecture of the proposed DLDO.

that the transient responses in the conventional DLDOs and previous AA-DLDOs degrade at high/low V_{IN}. These observations motivate us to use a single large output pMOS and bias it at weak inversion (particularly at the start of a large load step) for higher transconductance compared with that at strong inversion. This configuration decouples the operating regime of the output pMOS (e.g., weak or strong inversion) from the input voltage and enables fast transient response across a V_{IN} range of 0.5–0.9 V. This design consideration of the output stage and its advantage are first discussed in this letter. Finally, the proposed design changes the gate voltage of the output pMOS by digitally control the impedance of the pull-down switches at a certain bias current, and the ripple due to LSB switching can be reduced without a relatively large capacitance at the pMOS gate or V_{OUT} that is required in the charge-pumped-based LDOs [7], [8] due to charge domain operation ($V = Q/C$).

To reduce either the voltage droop at V_{OUT} or the required output capacitance during a rapid load step, the output stage should offer high dI_{OUT}/dV_{OUT}, while the digital loop is unable to respond due to its slow sampling clock. In the simulation of output stages as shown in Fig. 2, given a V_{OUT} profile that drops 100 mV with 1-ns edge rate, the output current I_{OUT} increases from I_{OUT0}, which is its value before the load step. This simulation shows the inherent responses of the three types of the output stages to a fixed voltage droop. In the conventional DLDO, I_{OUT} increases instantaneously when voltage droop occurs due to the $|V_{DS}|$ increase. Since the output switches are typically in the linear region and a typical design targets $\leq$100 mV droop, the boosted I_{OUT} due to $|V_{DS}|$ change is about $2-3\times I_{OUT0}$. A traditional AA architecture [4] yields a $3-5\times$ increase of the output current as output switch $|V_{GS}|$ increases when voltage droop occurs at V_{OUT}, and this has less impact at high input voltages (V_{IN} = 0.9 V). Please note that because the initial output current I_{OUT0} (before a large load step) is assumed to be small compared to the maximum load current, for conventional [1] and AA-DLDO [4], only one-tenth of the pMOS switches are "on" during the transient event. With the same total size of the output pMOS ($\times$10) and initial output current I_{OUT0}, the proposed structure provides a 9$\times$ current increases over an input voltage range of 0.5–0.9 V as shown in Fig. 2, which could be improved to 11$\times$ by biasing the output pMOS at weaker inversion with larger sizing ($\times$15 instead of $\times$10). This shows the potential of improved transient response with the new structure compared to the previous works including the charge-pump-based DLDO [8].

The proposed AA-DLDO is fabricated in 28-nm CMOS and limits output droop to 110 mV at both $V_{IN} = 0.5$ V and $V_{IN} = 0.9$ V upon a load current step of 50 mA (from 10 to 60 mA) in 1 ns with a total on-chip capacitance of 2 pF, leading to a speed FOM of 1.44 fs, which is comparable to the state of the art.

II. Circuit Design Details

Fig. 3 shows a more detailed diagram of the proposed architecture. One challenge associated with the proposed structure is reducing the voltage ripple at V_G of the output device, which can be high due to LSB switching and limit cycle oscillation (LCO). The nMOS array in this design conducts a designed current (I_P) of several μA, in the absence of a large capacitor at V_G to filter the ripple. A reasonable number of nMOS must be "on" in order to avoid a large ripple due to a single LSB switching. To increase the number of "on" nMOS devices needed to conduct a designed bias current, we must increase the on resistance of each nMOS. To achieve this, we bias the nMOS in the array with the reference voltage (V_{REF}) and V_{OUT} instead of V_{IN}, as shown in Fig. 3. $|V_{GS}|$ of an nMOS in this array is at least 200 mV smaller than V_{IN}, which enables $>$150$\times$ larger on resistance than the on resistance with $|V_{GS}| = V_{IN}$. To mitigate the ripple due to uncontrolled LCO, we include a feedforward path with a coefficient of $\beta/2 > 1$ in parallel with the bidirectional shift registers (SRs), which forces the LCO to mode 1 ($f_{LCO} = 0.5\, f_{CLK}$) [9]. Hence, after the proposed AA-DLDO reaches steady-state operation, the comparator output alternates between $+1$ and -1. The feedforward path cancels out the function of SRs, and the DLDO acts as a relaxation oscillator with a controlled ripple profile. The simulated peak-to-peak ripple at V_{OUT} with noise is less than 4 mV when $I_{LOAD} = 1$ mA.

There are three feedback loops in the proposed design, and Fig. 3 presents the response at V_{OUT} and V_G during a transient response. Loops 1 and 2 provide a transient response in high and medium frequency ranges, respectively, while loop 3 suppresses the steady-state error owing to its high dc gain. The feedforward path of $\beta/2$ introduces a left-half-plane zero in steady state which cancels the effect of the pole introduced by the SRs, and the stability of the proposed design in steady state can be evaluated with the structure in Fig. 4. It is similar to a unity-gain buffer with V_{REF} as input and V_{OUT} as output, while C_C (2 pF) between V_{OUT} and V_G acts as a compensation capacitor. The pole at V_G is the dominant pole and the pole at V_{OUT} is the high-frequency pole. The simulated phase margin (Fig. 4) exceeds 75° with a load current of 100 μA and an output capacitor of 1 nF as the worst case. Please note that at the same I_{LOAD} in Fig. 4, current source load at V_{OUT} would result in

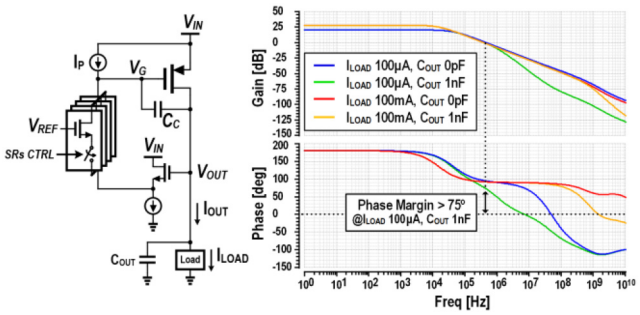

Fig. 4. Simulated Bode plot of the proposed design in steady state ($V_{\mathrm{IN}} = 0.9$ V and $V_{\mathrm{OUT}} = 0.85$ V).

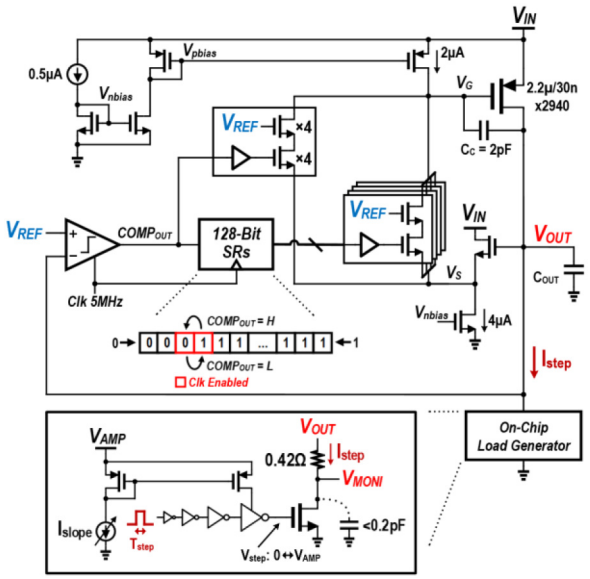

Fig. 5. Proposed digital LDO and on-chip load generator for testing.

a higher output impedance compared with the case with resistive load, which pushes the pole at V_{OUT} to lower frequency and reduces the phase margin. However, because the impedance of the output pMOS is typically much smaller than the resistive load or current source load in low-dropout operation, the performance differences due to current source load or resistive load is negligible.

Fig. 5 provides circuit details of the proposed AA-DLDO with an on-chip load generator (for testing purposes). Clock gating is implemented in the bidirectional SRs, and only the two neighboring SRs with different stored values are enabled during each clock period. The feedforward path driven by the comparator output uses $\beta = 4$ to provide enough margin for PVT variations. Fig. 6 presents the simulated transient responses with and without C_C/Loop 2, which shows the contribution of Loop 1 and Loop 2 to the transient responses. In the case without Loop 2, because we use low bias current (2 μA) for the switch array and clock frequency is too high compared with responses at V_G, the SRs would accumulate more zeros or ones than necessary [8]. After introducing Loop 2, the feedback from V_{OUT} to the sources of the nMOS switches reduces the gain of turning on/off one switch and accelerate responses at both V_G and V_{OUT}, which prevents the oscillatory behavior in the case without Loop 2 and reduces the settling time. Loop 2 also makes the source voltage of the nMOS switches (V_S) follow V_{OUT}. Because V_{OUT} changes with V_{REF}, this configuration reduces the sensitivity of the switch impedance to V_{REF} variations.

Though there are only pull-down switches at V_G, when overshoot happens at V_{OUT} due to load change, the overshoot at V_{OUT} will be coupled to V_G instantaneously through C_C, which reduces the

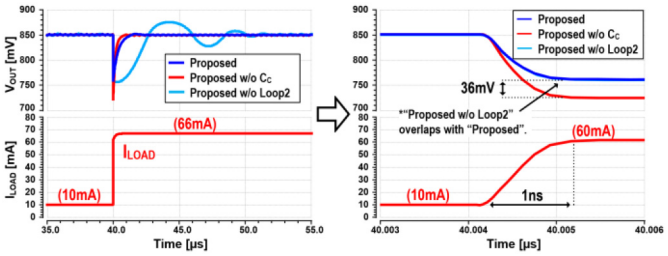

Fig. 6. Simulated load transient responses at $V_{\mathrm{IN}} = 0.9$ V and $V_{\mathrm{OUT}} = 0.85$ V w/ and w/o C_C/Loop2 for a load step from 10 to 60 mA with 1-ns edge time.

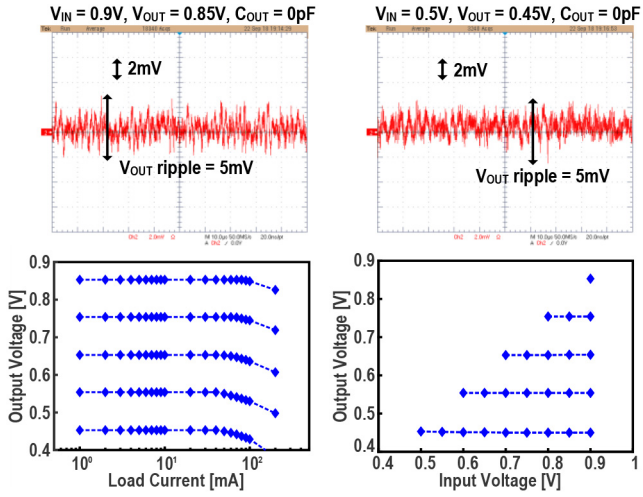

Fig. 7. Measured output ripple ($I_{\mathrm{LOAD}} = 1$ mA), load regulation (50-mV dropout voltage), and line regulation ($I_{\mathrm{LOAD}} = 10$ mA).

output current until the overshoot stops. Hence, the proposed architecture presents fast responses to both voltage droop and overshoot at V_{OUT}. There is a tradeoff between the response speed and settling speed in the proposed output stage: 1) a large gate impedance is desirable to achieve a fast response, which means small bias current and 2) to achieve fast settling speed, a large bias current is required to charge the capacitor C_C, which results in large static power.

It is challenging to generate an external load step with a 1-ns edge and feed it through PCB traces and bonding wires to the DLDO because of parasitic inductances and capacitances. We instead designed an on-chip load generator circuit (Fig. 5, bottom) in which both the load step amplitude and edge time are tunable through V_{AMP} and I_{slope}. When there is a rising/falling edge at the input of the inverter chain, the gate voltage of the nMOS for load generation (V_{step}) changes between 0 and V_{AMP}, which generates load step at V_{OUT}. An on-chip metal resistor (0.42 Ω) between V_{OUT} and V_{MONI} is used to measure the load current change (I_{step}) to characterize the load current profile.

III. Measurement Results

The test chip was fabricated in 28-nm CMOS. Fig. 7 shows the measured output ripple at $I_{\mathrm{LOAD}} = 1$ mA and $V_{\mathrm{IN}} = 0.9$ V/0.5 V, as well as load regulation and line regulation. The proposed DLDO can output 0.45–0.85 V with a 50-mV dropout voltage, and the maximum load current is 100 mA. Fig. 8 presents the measured transient response at $V_{\mathrm{IN}} = 0.5$ V/0.9 V. With 4-pF total capacitance (2 pF from C_C and 2 pF from the probe capacitance), when the load current changes from 10 to 60 mA with 1-ns edge time (observable), the measured voltage droop is 110 mV at both $V_{\mathrm{IN}} = 0.5$ V and $V_{\mathrm{IN}} = 0.9$ V. The load current step is measured with the on-chip

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

	This work	ISSCC'20 [6]	JSSC'20 [8]	ISSCC'19 [10]	ISSCC'18 [5]	ISSCC'17 [4]	JSSC'17 [3]
CMOS Technology	28nm	28nm	65nm	14nm	28nm	65nm	65nm
Architecture	AA-DLDO	AA-DLDO	Charge-Pump DLDO	Modular Hybrid LDO	NMOS-DLDO	AA-DLDO	Async. DLDO
Supply Voltage [V]	0.5-0.9	0.5-1	0.5-1	1-1.2	0.4-0.55	0.5-1	0.6-1
Output Voltage [V]	0.45-0.85	0.45-0.95	0.45-0.95	0.7-0.85	0.35-0.5	0.45-0.95	0.55-0.95
Load Range [mA]	0.1 to 100	up to 160-480	0.001 to 105	up to 530	0.5 to 20.5	0.2 to 13	up to 500
Area[mm^2]	0.03	0.049	0.04	0.262	0.0055	0.03	0.158
f_{CLK} [MHz]	5	-	1	-	4	10	N. A.
C_{TOTAL} [nF]	0.004*	0.004*	0.042	4	0.024	0.1	1.5
I_Q [µA]	5.9-8.2	7.7-241	4.9	31.1-53.5	0.81	3.2	300
Droop [mV]	110	112	185	133	117	105	50
ΔI_{LOAD} @t_{EDGE}	50mA @1ns	430mA @2ns	100mA @1ns	508mA @<0.5ns	20mA @3ns	10mA @1ns	100mA @2ns
ΔI_{LOAD}/ns	50mA/ns	215mA/ns	100mA/ns	>1000mA/ns	6.7mA/ns	10mA/ns	50mA/ns
Ripple [mV]	≤5**	-	<15**	-	-	-	5
FOM* [fs]**	1.04-1.44	0.41	3.8	64	5.7	230	2250

* Total capacitance including probe capacitance **Meas. across the whole load range *** FOM=(C_{TOTAL}·V_{DROOP}/ΔI_{LOAD}) · (I_Q/ΔI_{LOAD}). Smaller value is better.

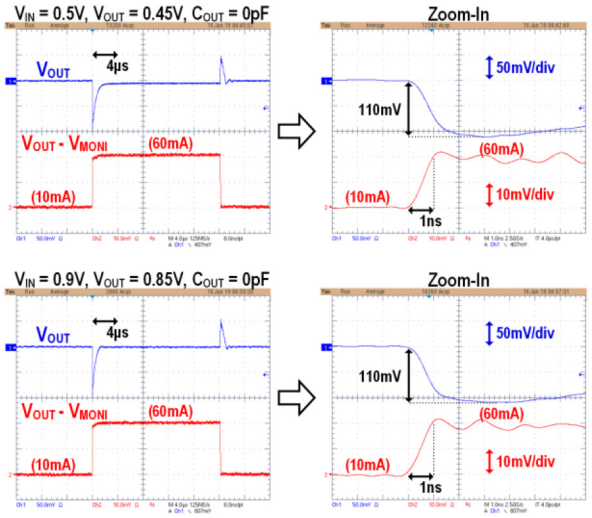

Fig. 8. Measured load transient responses at $V_{IN} = 0.5$ and 0.9 V for a load change from 10 to 60 mA with 1-ns edge time.

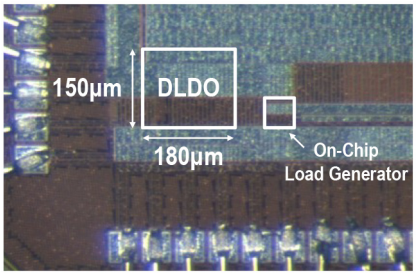

Fig. 9. 28-nm CMOS chip micrograph.

metal resistor (0.42 Ω) between V_{OUT} and V_{MONI} in Fig. 5. Because the operating regime of the output pMOS is decoupled from the input voltage (V_{IN}), the proposed design provides a fast transient response at both low and high input voltage, which is a key advantage of this structure and makes the design suitable for varying input voltages. In this chip, $C_C = 2$ pF is used (68.5% coupling efficiency from V_{OUT} to V_G), which is comparable to the parasitic capacitance at the gate of the output pMOS, V_G. This choice of small C_C translates to a good FOM but degrades the AA-loop gain and transient response. By using a larger C_C (10 pF) to mitigate voltage division due to parasitic capacitance at V_G, larger load steps (up to 90 mA) can be accommodated.

Table I summarizes test chip performances and compares them to state-of-the-art digital LDO designs. The proposed design realizes a 1.44-fs FOM, which is comparable to the state of the art. Fig. 9 presents the chip micrograph, including the AA-DLDO core and on-chip load generator.

ACKNOWLEDGMENT

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