

# An Open-Source and Autonomous Temperature Sensor Generator Verified With 64 Instances in SkyWater 130 nm for Comprehensive Design Space Exploration

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**Abstract**—This letter presents an open-source framework for autonomous generation of tapeout-ready temperature sensors. This framework uses a leakage-based digital temperature sensor design as the template. A cell-based design methodology is employed to allow full synthesizability and compatibility with computer-aided designs (CADs) flow and advanced technology nodes. Furthermore, the generator automates the design flow end-to-end in Python and supports designing completely with open-source CAD tools. Verified with 64 instances in SkyWater 130 nm, the generator also enables low-effort silicon-proven design space exploration that unveils the characteristics of leakage-based digital temperature sensors, with the most efficient one achieving 9.7 pJ-K<sup>2</sup> FoM,  $-0.67/0.74$  °C  $3\sigma$  inaccuracy, 130-nW power, and 24-mK resolution. To the best of our knowledge, this work is the world's first open-source silicon-proven generator for temperature sensors.

**Index Terms**—Circuit generator, leakage-based temperature dependency, open source, synthesizable design, temperature sensor.

## I. INTRODUCTION

Ultra-low-power, area-efficient, and accurate temperature sensors are critical for applications ranging from the environmental temperature sensing in ultracompact IoT nodes to arrayed on-chip thermal monitoring for detecting local hot spots in high-performance processors. Various approaches have been reported. Bipolar junction transistor (BJT)-based sensors [1], [2] provide high accuracy and a wide temperature range. Still, they are incompatible with sub-1V supply voltages in advanced technology nodes. At the same time, popular alternatives like resistor-based sensors [3], [4] suffer from high area overhead from passive devices, such as resistors and capacitors. Diode-based sensors [5] have been proposed to be compatible with sub-1V supply and advanced technology nodes. However, the requirement for an analog-to-digital converter (ADC) leads to power and area overhead. Addressing those limitations, leakage-based temperature sensors [6], [7] are promising candidates, which are compact, relatively low power, and compatible with advanced technology nodes due to their highly digital architecture. However, a fully custom design methodology for those sensors still causes high design effort incompatible with the highly automated computer-aided design (CAD) flows for digital designs today. Moreover, for under-development technology nodes such as the SkyWater 130 nm with open-source process design kit (PDK) [8], [9],

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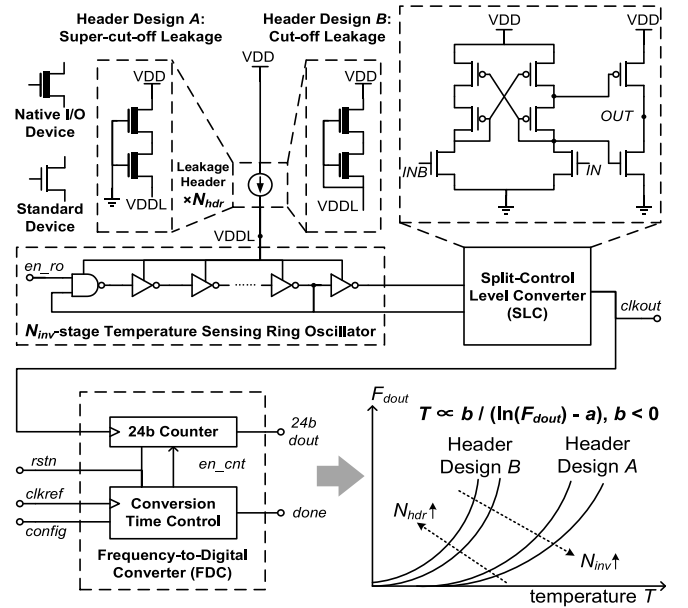


Fig. 1. Template temperature sensor design.

the incomplete and inaccurate information in PDK can cause high unreliability in modeling leakage-based temperature dependency [7] through simulation, where process variations can induce 20× variation in leakage [10]. To still deploy temperature sensors in that case, low-effort and silicon-proven design space exploration are desired as an alternative to inaccurate simulation for the ground truth of performance results.

This letter presents an open-source framework for the autonomous generation of tapeout-ready temperature sensors to minimize design effort and enable low-effort silicon-proven design space explorations. To the best of our knowledge, this work is the world's first open-source silicon-proven generator for temperature sensors verified with a fully open-source PDK. Source code and documentation of the generator are available on: <https://github.com/idea-fasoc/OpenFASOC>.

## II. LEAKAGE-BASED DIGITAL TEMPERATURE SENSOR

Fig. 1 shows the leakage-based digital temperature sensor used as the template for the generator framework, which is based on the designs [6], [7] that use ring oscillator (RO) as the temperature sensing element and employ leakage-based temperature dependency. The leakage header using stacked native I/O devices serves as a voltage regulator to generate VDDL with high tolerance against supply variations. The use of only one RO as a sensing element makes the

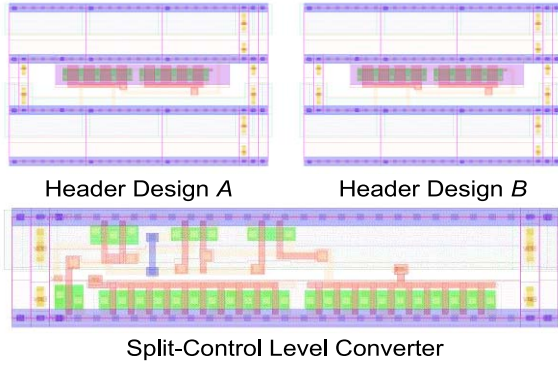


Fig. 2. Layout of AUX cells in SkyWater 130 nm.

sensor inherently immune to inter-RO mismatches. Intra-RO mismatches of delay cells can also be averaged and mitigated due to their randomness. The direct temperature-to-frequency dependency relaxes the requirement on the temperature stability of external clock reference. A 2-point calibration is used to generate linear outputs, which can be applied per chip to also address interdie process variations. Beyond existing works, two types of headers are supported in this work for various applications: 1) design *A* generates super-cut-off leakage and low RO frequency, which trades off higher quantization noise for lower power and 2) design *B* generates cut-off leakage and higher RO frequency, which trades off higher power for lower quantization noise.

The temperature sensing RO is designed in a gate-level netlist with standard cells to enable synthesizability. A wide-range split-control level converter (SLC) up-converts low-swing RO output. The frequency-to-digital converter (FDC) uses a 24b counter for high precision and is designed purely in register transfer level (RTL). Conversion time is controlled through the reference clock and external configurations.

Fig. 2 shows the layouts of leakage headers and SLC in SkyWater 130 nm. Designed as auxiliary (AUX) cells following standard cells' layout rules, they can be incorporated into the CAD flow and placed automatically following the standard cells grid, which enables a fully synthesizable design. Except for the AUX cells, designs of all other elements in the template are technology portable, while the AUX cells only require one-time customization for each technology node.

### III. GENERATOR FRAMEWORK

Fig. 3 shows the proposed generator framework. Building blocks of the design flow are integrated and automated using Python, which provides general accessibility. The generator supports standard commercial and open-source CAD tools, such as the OpenROAD [9], [11] project. For well-developed technology nodes where simulation is accurate, the generator is primarily used for minimizing design effort, and design-agnostic specifications, such as temperature range and optimization target are taken as input. For under-development technology, the generator can be used for silicon-proven design space exploration, where specific design parameters are taken as input, such as the number of headers  $N_{hdr}$  and the number of RO stages  $N_{inv}$ .

As is shown in Fig. 3 (top right), when taking in design-agnostic inputs, the generator first performs a grid search over the design space to find the optimized instance with performance data estimated from preliminary simulation results. Generated or input design parameters are then used to create a synthesizable Verilog HDL description of the complete design and CAD-vendor-agnostic constraints for synthesis and automatic placement and routing (APR). With a cell-based design methodology, AUX cells are treated equivalently as standard cells,

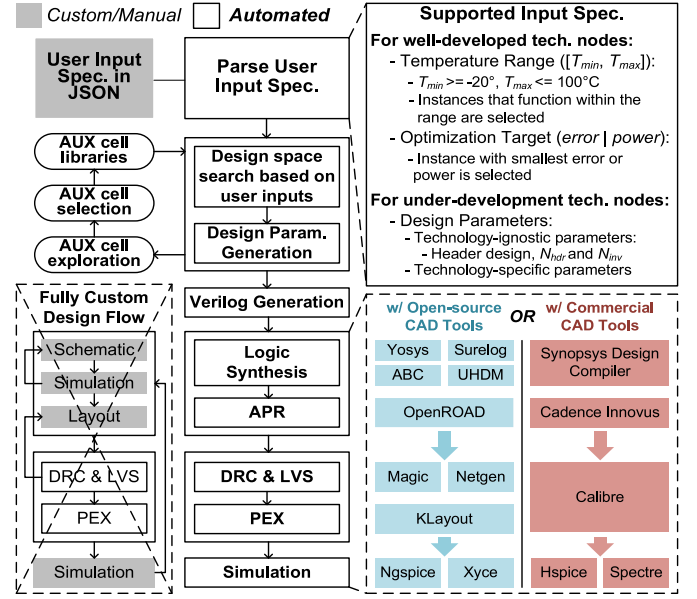


Fig. 3. Proposed temperature sensor generator framework.

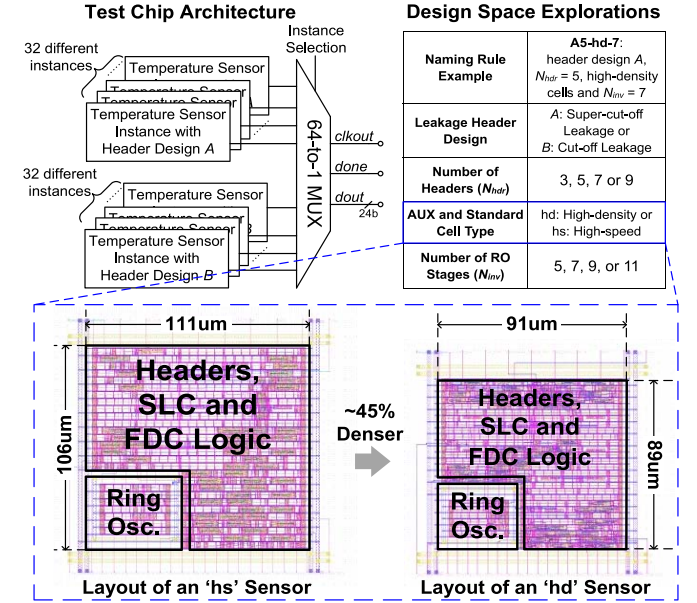


Fig. 4. Architecture of the test chip and design space.

and the temperature sensor design is then synthesized, placed, and routed in the same way as purely digital designs without the need for any APR specifications from users.

The layout of the generated design is then signed off through design rule check (DRC) and layout versus schematic (LVS). Finally, the transistor-level design is simulated with parasitic extraction (PEX), and the generator creates summarized performance results. Excluding tool-relevant post-PEX simulations, generating a tapeout-ready design takes only around 20 min, drastically reducing design effort and time consumption compared to full custom design methodology.

### IV. TEST CHIP ARCHITECTURE

Fig. 4 shows the test chip architecture that explores the temperature sensor's design space, which experiments with different leakage

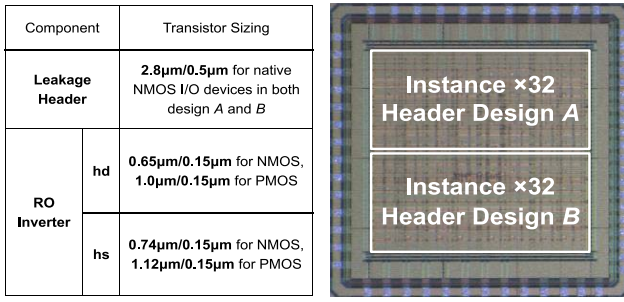


Fig. 5. Transistor sizing and die micrograph of the test chip.

header designs, the number of leakage headers  $N_{hdr}$ , number of RO stages  $N_{inv}$ , and AUX/standard cell type. Sensor instances can be implemented in either the high density (hd) or high speed (hs) standard cells, specific to the SkyWater 130 nm PDK. While “hs” instances can have higher RO frequencies, “hd” instances can be denser. Shown in Fig. 4 bottom, a “hs” instance can have a 45% area overhead over an “hd” instance with the other design parameters kept the same.

The test chip was fabricated through the 1st free Google-SkyWater 130-nm shuttle. For comprehensive design space exploration of a technology node at its early stage development, the design space was exhausted through generating sensor instances with specific design parameters given as inputs to the generator. As a result, 64 temperature sensor instances were generated and placed in the test chip, which can be multiplexed through external selection and tested individually. Fig. 5 shows transistor sizing for key building components and the die micrograph of the test chip.

## V. MEASUREMENT RESULTS

The chips are measured at 1.8-V supply with a 32.768-kHz reference clock frequency. Fig. 6 shows the inaccuracy measurement results of representative instances with different header designs, where each instance is measured across eight chips. For each instance, 2-point calibrations are applied per chip, and a third-order fixed-parameter systematic error correction (SEC) is applied across eight chips to remove nonlinearities. While instances of header A show decent linearity across temperature ranges, a solid quadratic nonlinearity is observed on instances of header B. Instances of header B show better accuracy and robustness under the  $-40\text{ }^{\circ}\text{C}$ – $80\text{ }^{\circ}\text{C}$  range, making them more suitable for low-temperature applications, while instances of header A have better accuracy for higher temperature ranges.

Fig. 7 shows relative inaccuracies, resolutions, and powers for all instances of reasonable accuracy across eight chips after calibration over  $0\text{ }^{\circ}\text{C}$ – $120\text{ }^{\circ}\text{C}$ . Pre-SEC inaccuracies are shown to highlight the differences in raw nonlinearity. Instances of “hd” cells show higher reliability and lower powers. With the same 31.25-ms conversion time, instances of “hs” cells and header A show the best resolutions. Though instances of “hd” cells and header A have the lowest powers, they also have the worst resolutions on average, possibly due to their lowest RO frequencies and high quantization noise. Across eight chips, instances of header A has a  $\pm 62\%$  power variation around mean power, while instances of header B has a  $\pm 36\%$  variation, showing better tolerance against process variations.

Table I summarizes measurement results for representative instances of each temperature range and comparisons with state-of-the-art leakage-and-FDC-based temperature sensors. Supply sensitivity at  $20\text{ }^{\circ}\text{C}$  is shown in the table, while the one at  $80\text{ }^{\circ}\text{C}$  high temperature is  $9.74\text{ }^{\circ}\text{C}/\text{V}$  for B3-hd-11,  $1.69\text{ }^{\circ}\text{C}/\text{V}$  for A9-hd-7, and

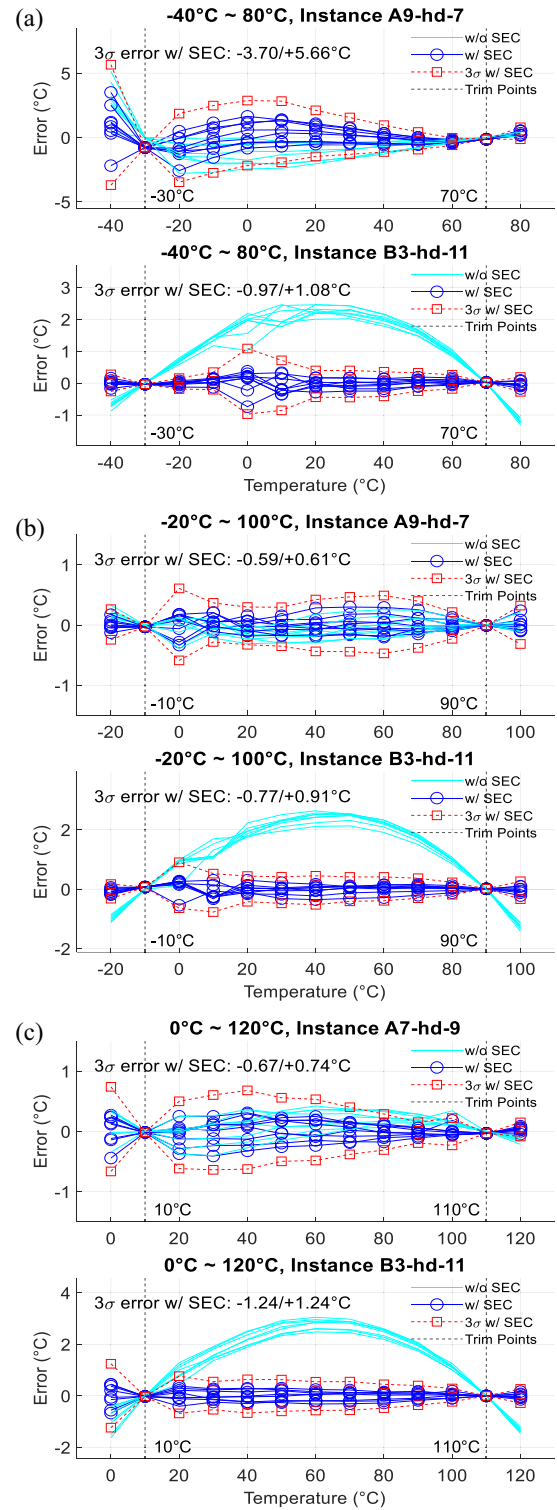


Fig. 6. Inaccuracies for representative instances: (a)  $-40\text{ }^{\circ}\text{C}$ – $80\text{ }^{\circ}\text{C}$ ; (b)  $-20\text{ }^{\circ}\text{C}$ – $100\text{ }^{\circ}\text{C}$ ; and (c)  $0\text{ }^{\circ}\text{C}$ – $120\text{ }^{\circ}\text{C}$ .

$1.73\text{ }^{\circ}\text{C}/\text{V}$  for A7-hd-9. Supply sensitivity can be mainly caused by the drain-induced barrier lowering (DIBL) effect in the headers, where supply variations lead to changes in drain-source voltage and leakage. RO frequency at  $20\text{ }^{\circ}\text{C}$  is 6.06 MHz for B3-hd-11, 3.61 kHz for A9-hd-7, and 2.44 kHz for A7-hd-9. Overall, instances of “hd” cells show better performance. Of all instances, “A7-hd-9” achieves the best  $9.7\text{ pJ}\cdot\text{K}^2$  FoM at 125-ms conversion time and 1.8 V, with



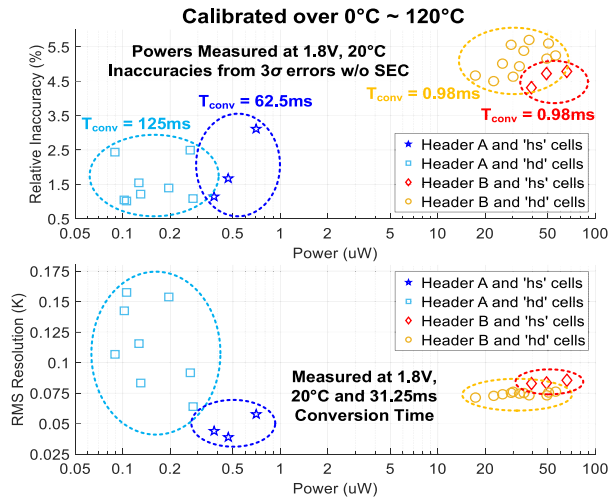


Fig. 7. Measurement results scattered for different instances.

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON

	This Work			JSSC '20	CICC '19	CICC '18	ISSCC '17
	B3-hd-11	A9-hd-7	A7-hd-9	[12]	[13]	[14]	[7]
Technology	SkyWater 130nm (Open-source PDK)			55nm	65nm	180nm	180nm
Generator-based Design	Yes			No	No	No	No
Supply Voltage (V)	1.8V			0.8 ~ 1.3	0.9	0.8 ~ 1.4	1.2
Area ( $\mu\text{m}^2$ )	8099			1770	13000	65000	8865
Temperature Range ( $^{\circ}\text{C}$ )	-40 ~ 80	-20 ~ 100	0 ~ 120	-40 ~ 125	-20 ~ 100	-20 ~ 80	-20 ~ 100
Conversion Time (ms)	0.98	125	125	1.31	34.3	840	8
Inaccuracy ( $^{\circ}\text{C}$ )	-0.97/1.08 (3 $\sigma$ )	-0.59/0.61 (3 $\sigma$ )	-0.67/0.74 (3 $\sigma$ )	-0.7/0.7 (3 $\sigma$ )	-2.7/1.8 (Min/Max)	-0.7/1.3 (Min/Max)	-0.22/0.19 (3 $\sigma$ )
Relative Inaccuracy	1.71%	1.00%	1.18%	0.85%	3.75%	2.00%	0.35%
Supply Sensitivity ( $^{\circ}\text{C}/\text{V}$ )	5.71	1.03	1.55	2.53 ~ 5.22	Not Reported	4.6	0.13
Power ( $\mu\text{W}$ )	17.33	0.25	0.13	9.3	0.00064	0.0013	0.075
Energy/Conv. (nJ)	16.92	31.38	16.25	12.2	0.022	11	0.6
Resolution (mK)	78	21	24	16	250	110	73
Resolution-FoM ( $\mu\text{J}/\text{K}^2$ )	101.9	13.4	9.7	3.1	1.4	140	3.2

−0.67/0.74  $^{\circ}\text{C}$  3 $\sigma$  inaccuracy, 130-nW power, and 24-mK resolution. The measured powers include on-chip instance multiplexing, so the reported numbers are very pessimistic. Still, performances of generated instances are comparable to prior arts with either more advanced technology nodes or much lower supply voltages, validating the fact that the proposed generator reduces design effort and time and provides decent post-silicon temperature sensing performance.

## ACKNOWLEDGMENT

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