RRAM-DNN: An RRAM and Model-Compression Empowered All-Weights-On-Chip DNN Accelerator

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***Abstract*— This article presents an energy-efficient deep neural network (DNN) accelerator with non-volatile embedded resistive random access memory (RRAM) for mobile machine learning (ML) applications. This DNN accelerator implements weight pruning, non-linear quantization, and Huffman encoding to store all weights on RRAM, enabling single-chip processing for large neural network models without external memory. A four-core parallel and programmable architecture adapts to various neural network configurations with high utilization. We introduce a customized RRAM macro with a dynamic clamping offset-canceling sense amplifier (DCOCSA) that achieves sub-microampere input offset. The on-chip decompression and memory error-resilient scheme enables 16 million (M) 8-bit (decompressed) weights on a single-chip using 24 Mb RRAM. The proposed RRAM-DNN is the first digital DNN accelerator featuring 24 Mb RRAM as all-on-chip weight storage to eliminate energy-consuming off-chip memory accesses. The fabricated design performs the complete inference process of the ResNet-18 model while consuming 127.9 mW power in TSMC-22 nm ULL CMOS. The RRAM-DNN accelerator achieves peak performance of 123 GOPs with 8-bit precision, exhibiting measured energy efficiency of 0.96 TOPs/W.**

***Index Terms*— Deep learning, deep neural network (DNN) ASIC, machine learning (ML) hardware, mobile, model compression, non-volatile memory, resistive random access memory (RRAM).**

I. Introduction

DEEP neural network (DNN) algorithms, first introduced in the early 1960s [1], are the cornerstone of modern artificial intelligence (AI) because they achieve unprecedented accuracy on various computer vision and machine translation tasks. The next wave in the AI revolution is the deployment of these DNNs on mobile platforms to perform challenging tasks under real-world constraints. However, existing hardware and infrastructure cannot provide satisfying performance and energy efficiency for emerging deep-learning-based applications because of their excessive computation and large memory footprints in state-of-the-art DNN models. For object recognition with the ImageNet data set [2], these DNN models [3]–[5] typically comprise more than ten million parameters and require more than 10 GOP per inference, which translates to more than 50 MB on-chip storage and 300 GOPS throughput for real-time 30 frames/s operation. They consume >100 W of power with general-purpose graphics processing units (GPGPUs), which cannot be integrated on mobile platforms due to their excessive power consumption and form factor. Therefore, there is a growing demand for high-performance, energy-efficient, and re-configurable DNN processors for mobile and embedded AI applications [6]–[17].

A. Prior Work and Limitations on ML Algorithms and ASICs

To address these challenges, various approaches using both machine learning (ML) algorithms and efficient hardware designs have been proposed to reduce the complexity of the DNN inference and to improve the energy efficiency, thereby maintaining accuracy for applications.

Iandola *et al.* [6] and Sandler *et al.* [7] propose to re-architect the neural network models and leverage efficient building blocks to reduce both the model size and the number of multiply-and-accumulate (MAC) operations. However, despite the dramatic complexity reduction, these approaches create new DNN layers with novel memory-access and challenging computation requirements that are not well-optimized with existing hardware [17]. Alternative approaches such as [8], [9] reduce the model complexity with pruning, quantization, entropy coding, and/or low-rank approximation of weights. However, their real-time energy-savings and performance gains are limited because of the inefficiency of running unstructured sparse models on the hardware. For example, [18] reports >1 W power consumption for real-time inference using compressed DNNs.

In parallel with improving DNN models, many digital ASICs [10]–[17] were proposed recently to accelerate deep

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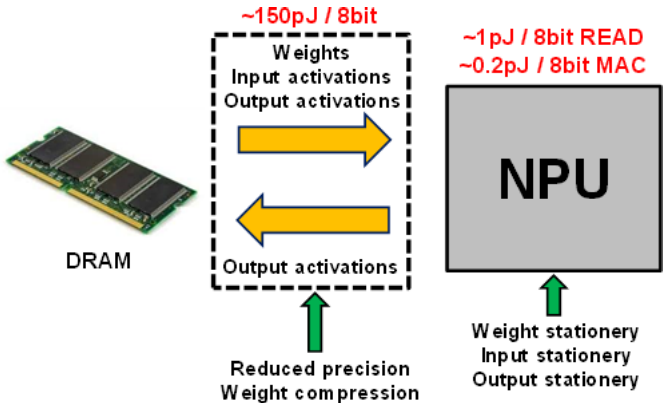

Fig. 1. Conventional system-level dataflow of NPU.

learning on mobile platforms. Various optimization techniques are explored in these designs, including dataflow optimizations [10]–[12], precision reduction [11], [13], [14], sparsity awareness [15], [16], and bit-serial operation [11]. Combining these techniques onto silicon implementations, state-of-the-art DNN processors achieve more than 100 GOPS performance and ∼2 TOPS/W efficiency during inference.

However, as shown in Fig. 1, most of these digital ASICs adopt a DRAM-neural processing unit (NPU) -style processing architecture for loading and computing DNN models [19]. The weights and input activations (IAs) are transferred on chip for processing while computed output activations (OAs) are transferred back to the large off-chip DRAM for temporary storage. While the processing on the NPU is extensively optimized through various techniques [11]–[16] (Fig. 1), transferring data on/off the NPU to the DRAM becomes a major bottleneck in the overall system because of the frequent and extremely high-energy data access to external DRAMs. In fact, transferring a byte from DRAM consumes $>3000\times$ more power than performing an 8-bit MAC calculation [10]. To relieve this problem, [10]–[12] propose to integrate dedicated weight and activation buffers and optimize the dataflow to reduce the data transfer to external DRAMs. Additionally, [14] proposes to leverage data compression technique to reduce the bandwidth to the DRAM. These methods significantly reduce the data access overhead to the DRAM but do not completely solve the problem.

To reduce the off-chip data/parameter accesses, a few prior designs [12], [13] attempt to store all parameters on chip. However, [13] suffers from very limited on-chip memory capacity (only ∼100 kB of weights are stored), which is insufficient to support large applications with >10 M weights. The design [12] achieves high capacity (7.68 MB on-chip weights and 96 MB SRAM stack) at the expense of high system power (3.3 W) due to the large SRAM stack and inductive inter-die communication.

B. Prior Work and Limitations on Non-Volatile Memories

Although embedded Flash memory has been deployed in micro-controllers as non-volatile storage for code and data [20], [22], technology scaling poses a substantial challenge with regard to the use of such charge-based Flash, SRAM, and DRAM [21]. The reduced capacity to hold sufficient charge on the floating gate of Flash memory, the internal capacitive node of SRAM, and the cell capacitor of DRAM degrade the performance, reliability, and noise margin, limiting their applications. As possible solutions, emerging non-charge-based non-volatile memories have been proposed, such as resistive random access memory (RRAM) [22]–[24], MRAM [25], [26], and PCRAM [27]. Among them, RRAM is a promising candidate for wide adoption to ML/DNN applications as it has logic-process compatibility and a large on–off ratio between the high resistance state and low resistance state for potential multi-level operations [24]. Various DNN accelerators employing Computation-In-Memory (CIM) techniques on RRAM have been proposed [28], [29]. However, due to limited computing precision, these CIM accelerators are not readily scalable to high-accuracy DNNs. And to date, there have been few designs that leverage RRAM's higher density and low standby power for all-on-chip parameter storage in large-scale digital DNN accelerators (versus a general-purpose non-volatile microcontroller [23]).

In this article, we present the first digital DNN accelerator featuring 24 Mb RRAM for all-on-chip weight storage to eliminate energy-consuming off-chip weight accesses, thereby reducing the overall system operating power. The design employs a four-processing element (PE) architecture in 22 nm ULL CMOS technology with 24×1 Mb custom-designed embedded RRAM banks. Using pre-compressed DNN models with an on-the-fly weight decompression mechanism, we achieve on average ∼1.5 b/weight for AlexNet, 3.2 b/weight for ResNet-18, resulting in a maximum total capacity of 16 M weights on chip. Highly parallelized and mesh-connected MAC arrays in the PE enable various workload mapping schemes to support DNN layers with different memory and compute characteristics. To reliably read and write to the RRAM, we propose a dynamic clamping offset-canceling sense amplifier (DCOCSA) that achieves sub-microampere input-sensing offset and a Write-Verify scheme for reliable programming. Combined with a mesh-connected MAC array architecture and 8 Mb shared SRAM, the proposed DNN accelerator operates at 120 MHz at 0.8 V digital VDD, achieving 0.96 TOPS/W [30].

The remainder of this article is organized as follows. Section II describes the overall architecture as well as the design details of the RRAM-DNN chip. Section III explains the dataflow and mapping of heterogeneous ML workloads onto the architecture. Section IV describes the compression of the DNN model. Section V explains the circuits of the custom-designed RRAM. Section VI shows the measurement results, and Section VII concludes this article.

II. Overall Architecture

Fig. 2 shows the overall architecture of the RRAM-DNN chip. The design consists of four PEs connected to a shared bus and a global shared memory. Each PE has its local memory for buffering the input–output activations, dedicated 6 Mb RRAM memory banks for non-volatile parameter storage, MAC array units for highly parallelized processing, and instruction memory for controlling the layer functions. In the

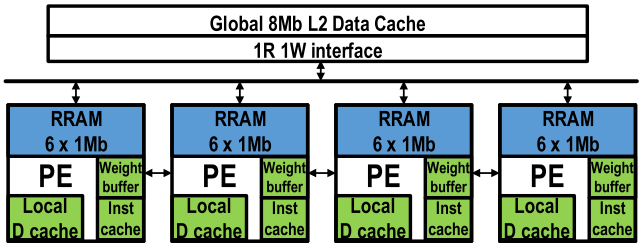

Fig. 2. Overall architecture of the RRAM-DNN chip.

architecture, each PE has both read/write access to its own local memory as well as read access to its neighboring PEs' local memories. The global shared memory is 8 Mb, and it supports parallel write and read access if the accesses are pre-partitioned to different memory banks. Due to the large chip size and the heterogeneous memory hierarchy, different memories in the architecture have different access latencies. The local memories including the input and weight buffers achieve 1 cycle access latency. Accessing neighboring PE's memories and the global memory incur access latencies of 2 cycles and 4 cycles, respectively. Moreover, the shared global memory coalesces multiple accesses by broadcasting data to all or a subset of four PEs when their read addresses are identical. In simulation, broadcasting data to coalesced requests results in $\sim 4\times$ latency reduction when multiple PEs are fetching the same IA from the global shared memory.

During the execution of a layer function, a PE first loads a block of IAs from the global shared memory to its local memory following user-defined memory partitioning. The PE's neighbors can share its IA because of the local connectivity between PEs. The PE then processes the layer function on the block of inputs with local stored weights. After all OAs are computed, the PE moves the output block back to the shared global memory. Each PE may process different data and execute different instructions, which can lead to a variable processing latency. Therefore, synchronization is necessary to ensure correct layer operations when the PEs are collaborating. The proposed design can be programmed to synchronize all or a subset of four PEs.

A. Detailed Architecture of the PE

Fig. 3 details the design of a single PE. Inspired by Li *et al.* [31], the PE architecture exploits parallelism and data reusability across different input dimensions to improve energy efficiency. Each PE has a mesh of 128 8-bit multiply/32-bit accumulate MAC units in four clusters (each with a grid of 4×8 MAC units). Each MAC also contains 32-bit flipflops to locally store processed partial sums. In total, four PEs have 512 MAC units on chip, enabling massive parallel processing for compute-intensive CNN operations. Moreover, each PE processes four input channels (IC), four output channels (OC), and eight IAs in parallel to maximize the data reusability in the MAC array. Each PE has its own private 6 Mb RRAM for parameter storage. During the CNN operation, weights are first read from the RRAM, decompressed through the decompression engine, and transferred to small 2-bank, 4-kB interleaved weight buffers for frequent local accesses.

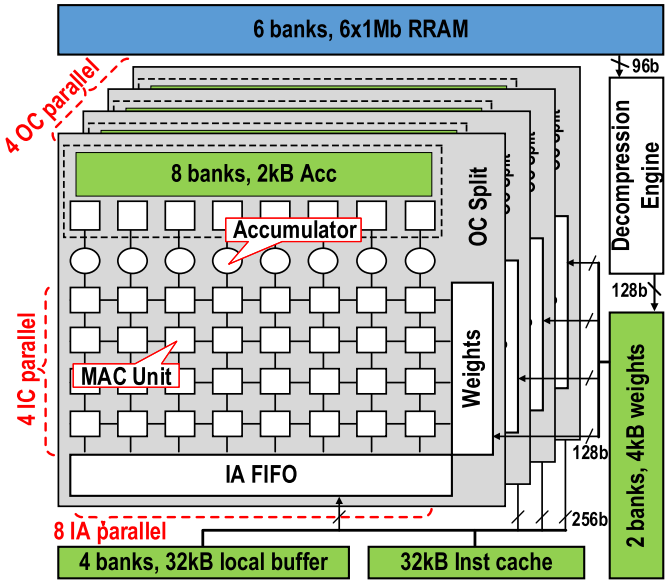

Fig. 3. Detailed architecture of the PE.

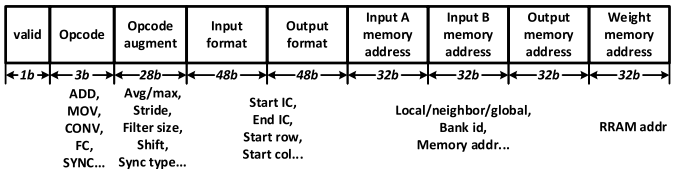

Fig. 4. ISA of the proposed RRAM-DNN accelerator.

The MAC array processing and weight decompression occur concurrently (pipelined) to maximize throughput. Accessing the small 4 KB weight memory provides 128 bit/cycle memory access bandwidth with high access energy efficiency. The 4-bank, 32 kB local buffer stores input and output activation with 256 bit/cycle access bandwidth. The high data bandwidth from both the weight buffer and local buffers ensures the full utilization of the 128 MAC units.

B. Instruction Set Architecture

To control the processing of MAC units for hundreds of cycles without explicit instruction decoding in each cycle, 256-bit Very long Instruction Word (VLIW) instructions are used. Moreover, the instructions are stored in the 32 kB instruction memory of each PE so that it can be programmed independently to control the processing sequence and synchronization of the DNN algorithm if necessary. Offset (direct) addressing with respect to each PE's own base address is used in the instruction set architecture (ISA) for arithmetic operations within a PE, including CONV, ADD, and POOL, to reduce the bit-width of the instructions. Non-offset global direct addressing is used when the data are moved from/to the global memory. Fig. 4 details the ISA of the proposed RRAM-DNN processor. The proposed ISA supports not only various layer functions such as convolution, pooling, matrix multiplication, and ReLU, but also flexible layer partition schemes such as the number of split input and OC. Data concatenation and scaling can also be achieved through MOV (move), ADD (addition) instructions.

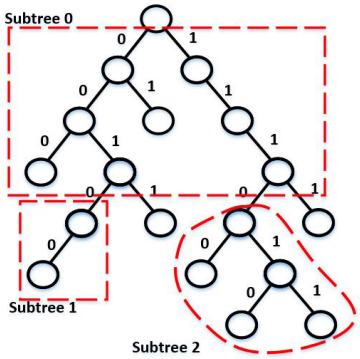

Fig. 5. Parallel Huffman decoder using full subtrees.

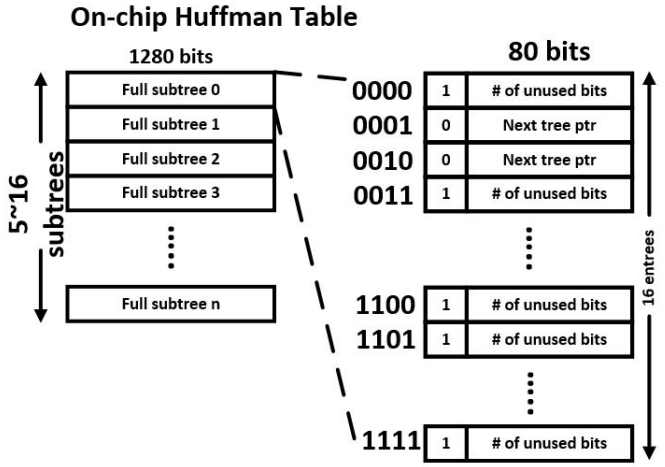

Fig. 6. On-chip Huffman table for decompression.

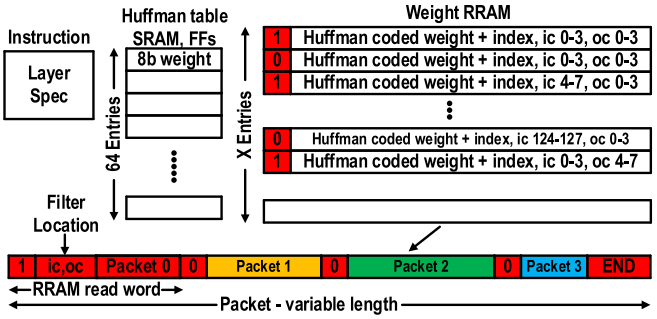

Fig. 7. On-chip compressed weight storage in RRAM.

C. Decompression Engine

The weight compression algorithm is adopted from [8]. During the training, unimportant weights are pruned to zero and all non-zero weights are non-uniformly quantized to 64 levels. To compress each weight, we use the Huffman encoded weight value (one of 64 levels) as well as the run length of the non-zero weight position. This algorithm compresses each weight to bit on average with negligible accuracy degradation for ResNet-18 [5]. Each PE is equipped with a decompression engine to decode the compressed weights stored in the RRAM. Each decompression engine contains two programmable Huffman tables: one for weight values and the other for run-length positions. These tables share a parallel lookup table (LUT)-based decoder. Decompressing Huffman encoded weight values and run-length positions to meet the processing bandwidth of the PE is challenging. On the one hand, decompressing the Huffman encoded 96-bit in a single cycle requires a logic with very long critical paths (>10 ns) due to inter-bit dependence in the compressed bit sequence. On the other hand, if the Huffman decoding was performed in series with single bit per cycle throughput, an entire weight packet would cost $>$ 250 cycles to process. Decompression throughput needs to be balanced with the throughput of the MAC array which takes 72 cycles for processing eight rows of 3×3 kernel. Therefore, instead of traversing a binary Huffman tree sequentially by advancing a single bit per clock cycle, we decode 4 bits in parallel to improve the performance (Fig. 5) per cycle. This requires storing all possible 4-bit subtrees (Fig. 6), which are stored in each PE and programmed through the PE programming interface. The critical path of decompressing 4 bits in parallel is 3 ns. Note that the layer-dependent nonuniform weight quantization and pruning requires reprogramming of these Huffman tables/trees for each DNN layer. We minimize the programming overhead by programming multiple PEs simultaneously when they share the same table.

D. RRAM Weight Storage and Static Error Resiliency

The compressed weights for convolutional layers are stored in the RRAM as packets shown in Fig. 7. Each packet has a variable length (because each weight length is variable) and is split into multiple RRAM words. Each packet contains a layer specification, Huffman coded weight values, and run-length codes for 4 input and 4 OC. The layer specification consists of the kernel offset and location for weights. We insert this specification information for every packet to make the system resilient to RRAM word errors. Since each weight and packet has variable length, a single RRAM word error can cause catastrophic decompression failure for subsequent packets. The proposed packet specification enables faulty word mitigation by repeating the same packet (including the specification) twice if the first packet was written on a faulty RRAM word(s). In that case, the second packet overwrites the first faulty packet during the decompression process. We assume RRAM word error locations are static and identifiable before programming the chip.

III. Dataflow of the Proposed RRAM-DNN Core

The proposed architecture and ISA support flexible mapping of heterogeneous DNNs for efficient hardware execution. This section discusses the various energy-efficient dataflows that are supported in the proposed architecture. The evaluations of different dataflows are performed with a python-based cycle accurate simulator, modeling the behavior of the designed four-PE system. The simulator pre-allocates weights and activations onto the PEs and computes corresponding memory addresses based on a given partitioning scheme. Then, the simulator profiles the chip behavior/execution trace for evaluation/verification, and also generates VLIW instructions (Fig. 4) to control the chip.

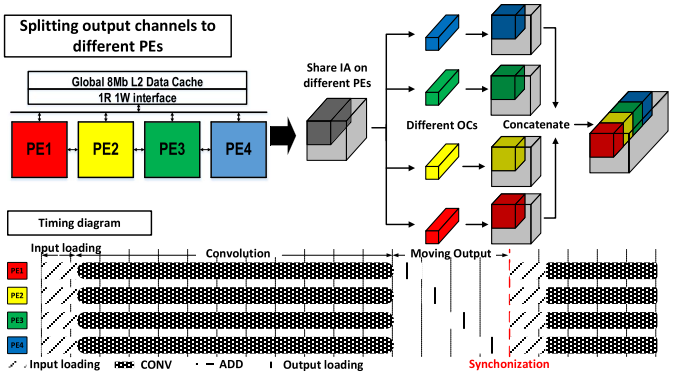

Fig. 8. Split convolution onto multiple PEs by OC.

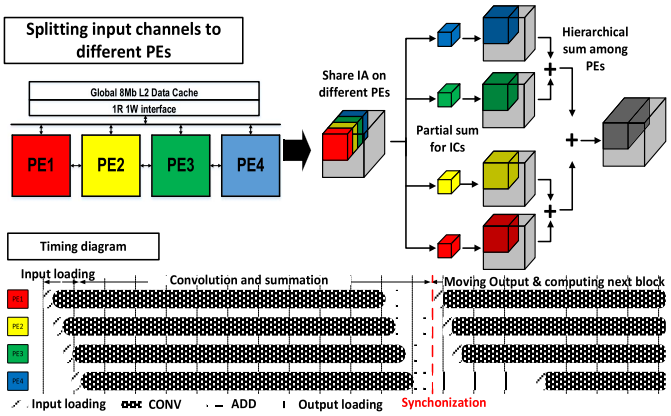

Fig. 9. Split convolution onto multiple PEs by IC.

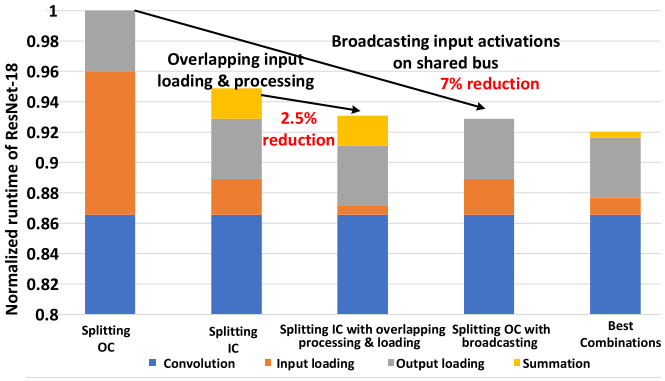

Fig. 10. Optimizing processing latency with multiple PEs (simulation).

A. Partition Workload Onto PEs by OC

One example of mapping a DNN layer to the architecture is shown in Fig. 8. The colors in Fig. 8 indicate weight/kernel mapping of a convolutional layer to the architecture, where the weights are split by different OC mapped on dedicated PEs. In this example, the weights are pre-partitioned on these four PEs, and each PE is programmed to compute different OC through instructions. Meanwhile, the IAs are partitioned into 8×8 blocks, with all associated IC, for processing to match the local memory capacity in each PE. When the processing of an 8×8 block for all IC finishes, the PE re-organizes the output and moves it back to the global memory. The outputs from multiple PEs are concatenated in this process to form the complete layer output. The timing diagram of the process is shown in Fig. 8 (bottom). Although each PE stores only 1/4 of the total weights and also processes only 1/4 of the convolutions, the same complete IAs from the prior layer must be copied to the local memories of each PE. To minimize this potentially redundant traffic and save data transfer time, we enable the bus to broadcast IA to all PEs. In simulation, the combination of IA broadcasting and global memory access coalescing improves the MAC utilization and reduces the inference latency by 7% (Fig. 10).

B. Partition Workload Onto PEs by IC

Another possible mapping of a convolutional layer to different PEs is input channel-based partitioning. In that case, each PE processes a partial sum of different IC as shown in Fig. 9. A selected PE merges the results from neighboring PEs hierarchically and then writes the merged results to the global memory (Fig. 9, bottom). Thanks to the local connection between neighboring PEs, no extra data movement is needed as each PE has read access to each neighboring PE's local memory. Similar to the output channel split mapping in Section III-A, weights are pre-partitioned on these four PEs and IAs are partitioned into 8×8 blocks (and 4 of all IC) for processing. Compared with splitting the OC, this input channel partitioning scheme involves uneven workload distribution among the PEs because a selected PE(s) needs to perform the extra merge and move operations. This can potentially lead to idle cycles and low MAC utilizations for the other PEs. However, the workload can be balanced throughout the entire convolution layer if the merge and move operations are mapped onto all PEs in a round-robin fashion. Because the IAs are partitioned into $8 \times 8 \times 4$ (IC) blocks per PEs, and typically there are >64 blocks in a layer, the workload can be balanced for the overall layer. This workload balancing scheme improves the overall MAC array utilization by 2.5%. Fig. 10 summarizes the different workload partitioning methods and their impacts on MAC utilization with ResNet-18.

Each individual layer in the network can be separately programmed for the best workload partitioning based on the layer characteristic. For the ResNet-18 example shown, 8% overall latency reduction can be achieved with layer-dependent best combinations of aforementioned partitioning schemes compared to a naïve approach (Fig. 10).

C. Data Reuse for Efficient Convolution Processing

Convolution operations on a single PE are optimized with massive parallelism and data-reuse. Similar to the CNN design in [31], each PE consists of four clusters of 8×4 MAC arrays, processing eight consecutive pixels and four consecutive IC in parallel. Partial convolution is performed with shifting IAs using a row of 8 MAC units with k (kernel size) cycles. This operation is repeated on the second and third row of IAs to complete the 2-D convolution. The pooling operations are performed in the same fashion except that MAC is replaced by Max in the 128 MAC units. Partial products in 2-D convolution are accumulated locally in each MAC unit to improve the energy efficiency without unnecessary memory accesses.

TABLE I
EXAMPLE OF APPLY COMPRESSION SCHEME ON RESNET18

	Total number non-zeros parameters (TNZ)	Weight bitwidth (w)	Index bitwidth (r)	Top-1 Error	Top-5 Error	Compression rate
Baseline	Conv layers: 10.99 million FC layers: 0.513 million	FP32	-	28.22%	9.42%	-
Pruning	Conv layers: 4.565 million FC layers: 0.094 million	FP32	-	28.20%	9.42%	-
Pruning + Quantization	Conv layers: 4.565 million FC layers: 0.094 million	INT8	-	28.17%	9.40%	-
Pruning + Quantization + Runlength coding	Conv layers: 4.565 million FC layers: 0.094 million	INT8	INT5	28.17%	9.40%	6.08x
Pruning + Quantization + Runlength coding + huffman coding	Conv layers: 4.565 million FC layers: 0.094 million	5.5	2.4	28.17%	9.40%	10.01x

$$Bit/weight = \frac{(r+w)*TNZ\text{-}conv + (r+w)*TNZ\text{-}fc}{TNZ\text{-}uncompressed}$$

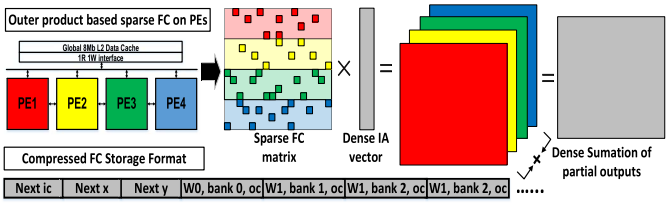

Fig. 11. Sparse FC operation of the RRAM-DNN design.

D. Data Reuse for Efficient Processing of Sparse Fully Connected Layers

The compressed weights for the FCL are very sparse, with typically less than 20% density [8] (Table I), whereas the IAs for the fully connected layers (FCL) are densely populated. Inspired by Subhankar *et al.*, [32], we deploy outer-product-based matrix vector multiplication to efficiently compute the FCL and skip all zero multiplications. Similar to the convolution operation, sparse FCL weights are stored in the compressed format and are pre-partitioned onto each PE during the compile time to enable highly parallelized processing with multiple PEs (Fig. 11). Different from convolution layers, weights for FCL are only pruned and quantized without Huffman coding to increase the decompression rate to match the throughput of parallelized processing without weight reuse. During processing, each element of IAs is multiplied with sparse non-zero weights from RRAM in each PE. Partial outputs are then accumulated and stored in the accumulators depending on the location of the non-zero weights. As multiple PEs finish processing subsets of an FCL, selected PEs merge the FCL output hierarchically and write the results to the global memory.

IV. COMPRESSED MODEL FOR SIMULATION AND MEASUREMENTS

To enable the single-chip implementation for DNN models, we leverage an idea from a state-of-the-art deep compression scheme [8] for compressing DNN models. However, the compression scheme also has to be co-designed to maximize the performance and efficiency of the architecture. The convolution layers typically require less bandwidth to decompress weights because each weight can be reused over multiple cycles for different input–OAs. Therefore, the weights for

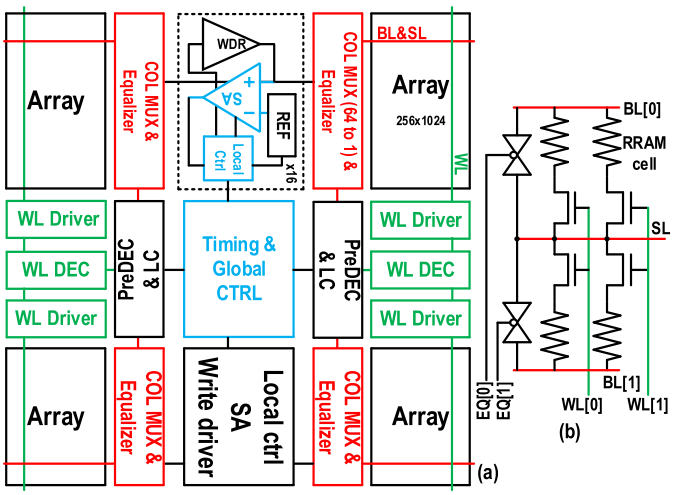

Fig. 12. (a) RRAM bank architecture (b) Common SL arrangement.

convolution layers are pruned, non-linearly quantized with 64 weight centroids and run-length coded using 5-bit codes to achieve maximum compression. On the other hand, weights are only used once for FCL. Thus, it is necessary to simplify the compression scheme to balance the weight decompression throughput with the FCL computation throughput. The weights for FCL in our design are pruned without any entropy coding. On average, the proposed compression scheme achieves ~5.5 bit per weight in convolution layers and 2.4 bit per weight in FC layers. Table I shows an example of applying the compression on ResNet18 when trained and evaluated under the ImageNet data set [2]. Pruning the weights reduces the model size of the convolution layers by 68% and FCL by 82%. Run-length coding and Huffman coding further compress the pruned convolution layers by 40% (from 8-bit weight and 5-bit run-length to 5.5-bit weight and 2.4-bit run-length for non-zero weights). With both methods combined, the average bits/weight is 3.2.

After the proposed weight compression, the DNN model exhibits negligible accuracy degradation compared with 8-bit uncompressed weights under ImageNet [2] evaluation.

V. CUSTOMIZED RRAM MEMORY

The 1 Mb custom-designed RRAM bank uses a butterfly architecture, as shown in Fig. 12(a), which is composed of four 256 × 1024 RRAM arrays with 32 b word length. The three colors denote the three main power domains used in the bank for testing flexibility: 1.4 V for the word line (WL, green), 1.25 V for the column mux (red), and 1 V for the sense amplifier (SA) and ctrl (blue). The RRAM array employs a common source line (SL) cell arrangement [33]. Thus, the column-wise peripherals include an equalizer [Fig. 12(b)] to virtually short the half-selected column when the other one is being written.

A. Dynamic Clamping Offset-Canceling SA

RRAM typically suffers from high variation in cell resistance which can vary by 2~10× for the low resistance state and 5~100× for the high resistance state [34], leaving a small sensing margin on sensing circuits. To address the high

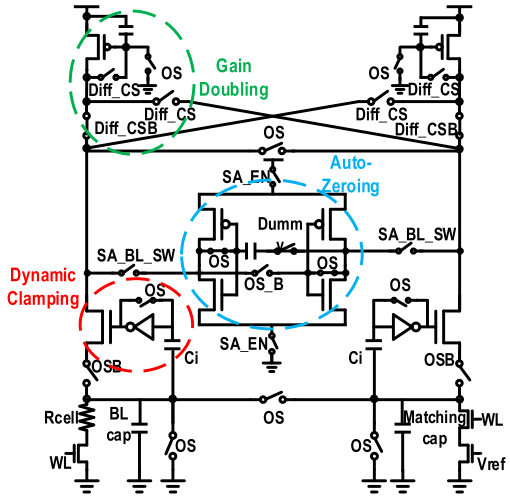

Fig. 13. Proposed DCOCSA.

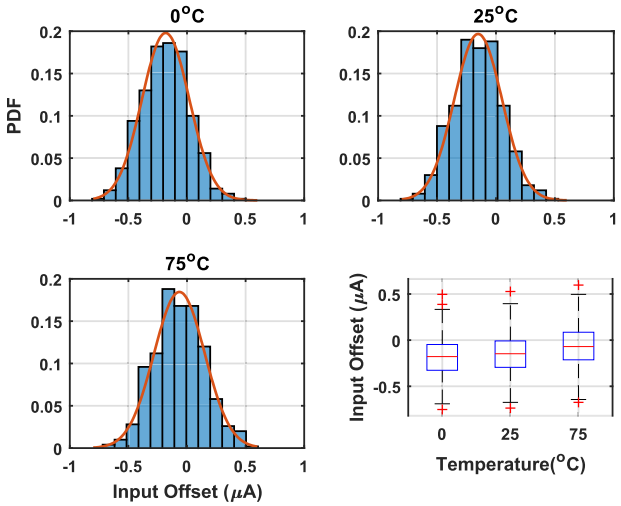

Fig. 14. DCOCSA input current offset MC simulation distribution.

variation nature of the RRAM, the two-stage offset-canceling current-mode SA shown in Fig. 13 is proposed. The first stage is composed of two cross-coupled current sampling branches similar to the scheme in [35], which doubles the input current difference and effectively halves the offset. In addition, the first stage incorporates dynamic clamping, instead of typical static clamping, to bring down the bitline settling time and increase the sensing speed. Unlike conventional clamping amplifiers, which are large and power hungry, a carefully designed self-biased inverter provides the feedback loop. The settling time is reduced by 50% (simulation) compared to a static clamping SA under the same load. The second stage provides further amplification and offset-reduction with a single-cap auto-zero regenerative amplifier [26].

Fig. 15(a) details the operation of the proposed SA. In step ①, the input and output of the inverter are shorted to self-bias the clamp transistors, with bias voltage sampled on the Ci's. Meanwhile, the regenerative amplifier of the second stage is also shorted to sample the offset and cancel it out in the following steps. This step overlaps with address decoding to avoid a timing penalty. Then, in step ②, the shorted inverter in phase one is disconnected to function as a negative feedback amplifier, and the WL is turned on to allow the two diode-connected PMOS headers to sample the currents I_{ref} and I_{cell} on their respective branches. After the current settles, in step ③, the two headers are switched to the other branch and function as a current source, which generates current difference $I_{\text{cell}} - I_{\text{ref}}$ on both input nodes of the second stage. However, note that the directions of the two current differences are opposite, which effectively doubles the current difference of the input to the second stage to $2(I_{\text{cell}} - I_{\text{ref}})$. Finally, in step ④, the second stage is fired and latches the output. The voltage waveforms of the internal nodes are shown in Fig. 15(b). A sub-microampere current offset is achieved at 21 μA common mode input under 1.2 V VDD from Monte Carlo (MC) simulation with 500 samples; Fig. 14 gives the offset distribution at different temperatures.

B. Write-Verify Process

RRAM also suffers from variation in write time. At a fixed write voltage, the write time of slow cells and fast cells can differ by more than 100× [36]. Thus, applying a write pulse of the same length to both fast and slow cells causes unnecessary power and endurance losses on the fast cell. So, a fine-grained iterative Write-Verify control is adopted. Each bit in a word is separately controlled based on the read result, ruling out correlation between fast and slow cells, which alleviates locality-dependent variation. Furthermore, with Write-Verify, each cell automatically adapts to the corresponding SA offset, further reducing the locality dependence.

Fig. 15(c) illustrates the block diagram of the Write-Verify control. Following a write request, each RRAM cell of the target address is read out first to compare with the input data (DG) initiated by the global control. If the read-out value (d) of a cell is the same as the corresponding bit in DG, the write process of that cell concludes for better endurance. On the other hand, the cell is programmed to the desired value by the iterative Write-Verify process.

VI. Measurement

We implement the proposed accelerator in 22 nm ULL CMOS technology with each PE of size 1614 × 1394 um^2 and each 1 Mb RRAM bank of size 235 × 514 um^2 as shown in the die photograph [Fig. 16 (a)]. The test chip achieves 120 MHz core clock frequency at 0.8 V VDD and consumes 42.4 mW when evaluating a CNN layer of size $4 \times 3 \times 3 \times 16$ as depicted in the measured power/frequency versus VDD plot [Fig. 16(b)] for core digital logic, which is everything except the RRAM banks.

In the implementation, the RRAM clock is hard coded to be half of the core clock; the RRAM operates at 60 MHz for the 120 MHz core frequency. A power breakdown of the four RRAM power domains is shown in Fig. 17(a), with 1V for the SA and control, 1.4 V for the WL, 1.25 V for the column mux, and 1.1 V for the inverter amplifier, noting that this breakdown includes the effect of the possible static errors in RRAM. A measured RRAM resistance distribution across ∼10 k cells randomly sampled from the 24 banks in one test chip at room temperature is shown in Fig. 17(b). The proposed

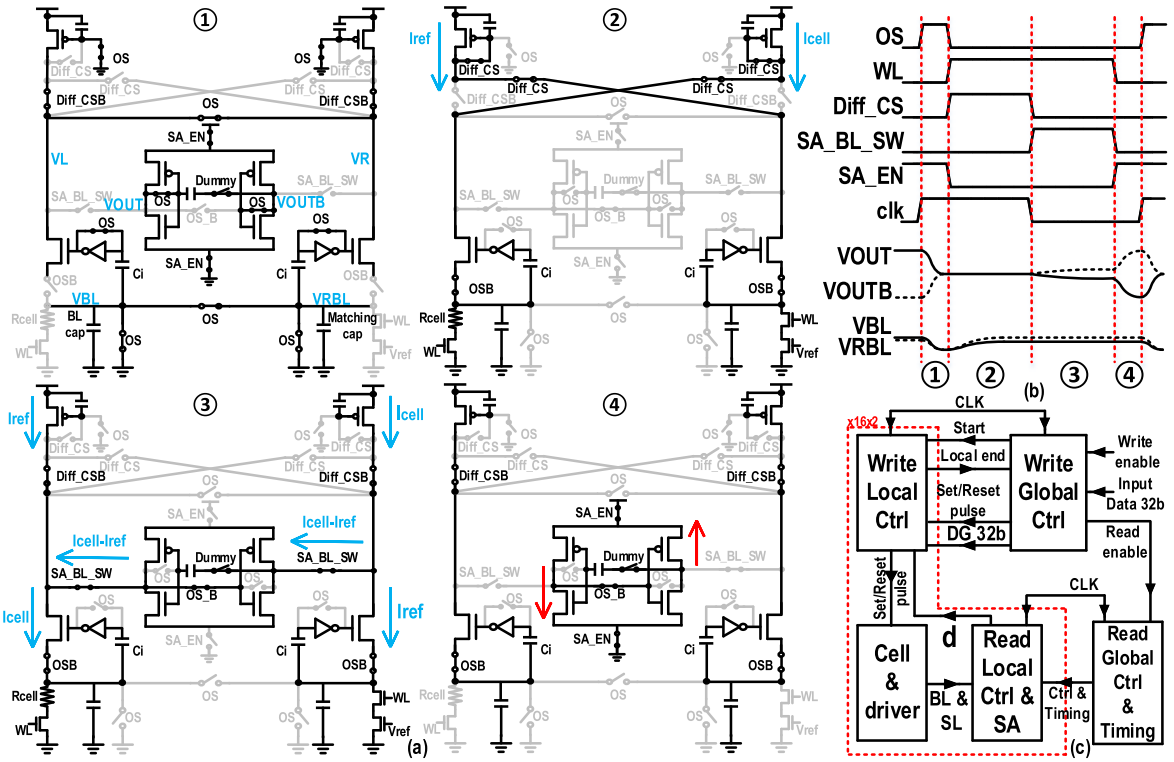

Fig. 15. (a) Operation and (b) timing of DCOCSA and (c) Write-Verify Signal Flow.

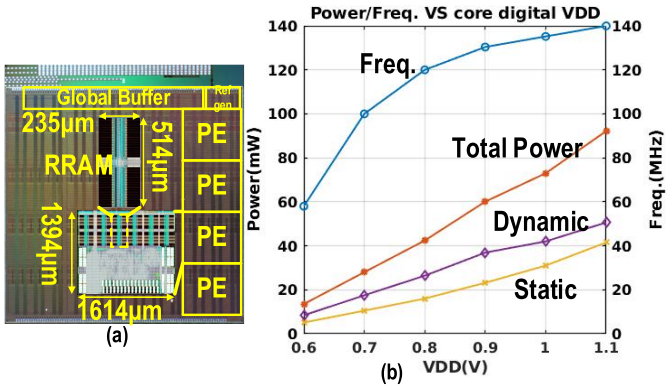

Fig. 16. (a) Die Photograph and (b) power/Frequency versus VDD for core digital logic.

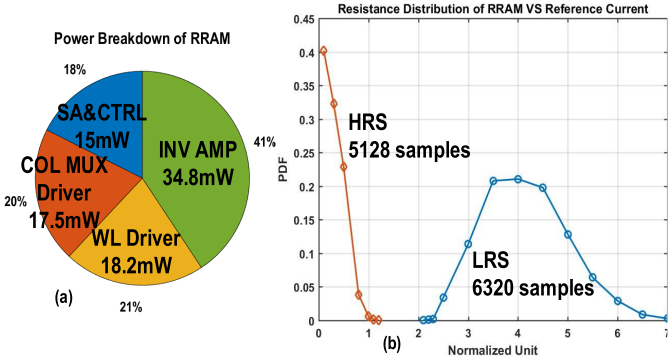

Fig. 17. (a) RRAM power breakdown and (b) measured RRAM resistance distribution.

accelerator consumes 127.9 mW in total, including weight decompression and transfer from RRAM to SRAM, resulting in a power efficiency of 0.96 TOPS/W. Table II compares the work to recent NN accelerators. The proposed design achieves the highest number of on-chip stored weights due to the model compression and better density of RRAM and is also the only design employing non-volatile memory as dedicated weight storage, thereby reducing standby power for edge devices.

TABLE II
COMPARISON TO OTHER WORKS

	This Work	QUEST[12]	SNAP[37]	STICKER[16]	UNPU[11]	Envision[38]
Technology	**ULL 22nm**	40nm	16nm	65nm	65nm	28FD-SOI
On-chip RAM(B)	**3M RRAM 1.3M SRAM**	7.68M+96M 3D SRAM	280.6K	170K	256K	148K
Max On-chip Weight	**16M@8b Non-Volatile**	15.36M@ 4b Volatile	140.3K@16b Volatile	170K@8b Volatile	256K@8b Volatile	148K@8b Volatile
Off-chip Memory	**No**	Yes	Yes	Yes	Yes	Yes
MACs	**4x128 (8x8b)**	24x512 (1x1b log)	252 (16x16b)	256 (8x8b)	4x576 (1x16b)	256 (8x8b)
Voltage (V)	**1.0-1.2 RRAM 0.6-1.1 Core**	1.1	0.55-0.8	0.67-1.0	0.63-1.1	1.05
Freq. (MHz)	**60 RRAM 120 Core**	300	33-480	20-200	200	200
TOPS/W	***0.96@8b**	†0.59@4b	‡3.61@16b	‡1.038@8b	‡5.57@8b	‡1@8b
GOPS	**123@8b**	1960@4b	65.52@16b	102@8b	690@8b	102@8b
Power (mW)	**127.9 @120MHz**	3300 @300MHz	364 @480MHz	284.4 @200MHz	297 @200MHz	44 @200MHz
Chip Area (mm^2)	**10.8**	122	2.4	12	16	1.87

* Including power of loading weights from RRAM to SRAM and MAC
† Including power of loading weights from 3D SRAM to on-chip SRAM & MAC
‡ Excluding power of loading weights from off-chip memory

VII. CONCLUSION

In summary, we present the first energy-efficient digital DNN accelerator featuring RRAM for dedicated weight

storage to enable efficient single-chip inference of NN models for mobile devices. Using on-the-fly weight decompression, we achieve a total capacity of 16 M 8 bit weights on chip. To reliably read from and write to the RRAM, we propose a DCOCSA achieving sub-microampere input-sensing offset. Together, these techniques help us eliminate fully off-chip weight access. The proposed processor is prototyped and measured in TSMC 22 nm ULL with RRAM technology. This design supports single-chip NN model inference with ∼16 million parameters. It achieves 123 GOPs throughput in real-time, consuming 127.9 mW from a 0.8 V supply, with measured 0.96 TOPS/W efficiency. The proposed design achieves the highest number of on-chip-stored weights and is also the only design employing non-volatile memory as dedicated weight storage, reducing standby power for edge devices.

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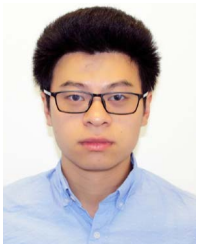

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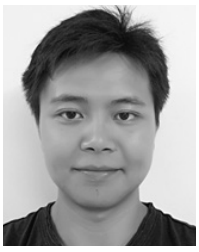

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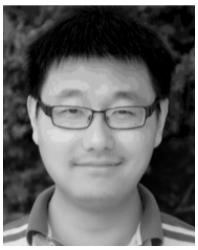

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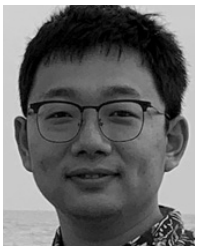

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Dr. Blaauw received the 2016 SIA-SRC Faculty Award for lifetime research contributions to the U.S. semiconductor industry and won the Motorola Innovation Award. He was the General Chair of the IEEE International Symposium on Low Power, the Technical Program Chair for the ACM/IEEE Design Automation Conference, and serves for the IEEE International Solid-State Circuits Conference's technical program committee.