

Reference Oversampling PLL Achieving -256 -dB FoM and -78 -dBc Reference Spur

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Abstract—This article presents a low jitter, low power, low reference spur LC oscillator-based reference oversampling digital phase locked loop (OSPLL). The proposed reference oversampling architecture simultaneously offers a low in-band phase noise, a wide-bandwidth, and a low spur. In addition, this article proposes an LC digitally controlled oscillator (DCO) for the proposed OSPLL to achieve a fast frequency update and fine frequency resolution, while its varactor switching timing is set optimally for low jitter using the proposed DCO tuning pulse timing control scheme. The proposed OSPLL was fabricated in a 28-nm CMOS process. The integrated rms jitter of the PLL was measured at 67.1 fs for an output frequency of 4 GHz. The in-band phase noise of the PLL was -129.2 and -132.5 dBc/Hz at 1- and 5-MHz offset frequencies. The measured reference spur of the PLL was -78.1 dBc. Total PLL power consumption was 5.2 mW, resulting in -256.3 -dB PLL jitter-power FoM, while occupying 0.17-mm² area.

Index Terms—Digital controlled oscillator (DCO), digital PLL, frequency synthesizer, reference oversampling PLL (OSPLL), reference spur.

I. INTRODUCTION

GENERATION of high-purity clock sources is becoming more crucial in today's communication systems. With the advent of advanced communication systems such as 5G wireless radios and ultrahigh-speed wireline transceivers, the required clock jitter is now below 100 fs [1]–[3], [51]. For example, the integrated jitter requirement of the local oscillator (LO) in 5G transceivers can be as low as 90 fs to maintain an acceptable error vector magnitude (EVM) [1], [2]. The front-end ADCs in ultrahigh-speed wireline transceivers demand clock jitter less than 100 fs to avoid signal-to-noise ratio (SNR) degradation [3].

However, it is hard to generate a clock with such a low jitter while satisfying other requirements such as power and

spur, due to conflicting trade-offs [4]–[9]. A wide bandwidth is beneficial since it provides larger suppression of the oscillator phase noise, achieving better power efficiency [50]. However, to achieve wide bandwidth, it is critical that the in-band phase noise from the loop components is low, which can incur large power consumption [9]. High reference spur [4]–[6] and stability issues [7], [8] are another concern that make it difficult to achieve wide bandwidth. Therefore, the bandwidth of a PLL is typically set much lower than the stability limit of $F_{\text{REF}}/10$, increasing the power consumption of the oscillator and degrading overall PLL power efficiency [43], [48]–[50].

There have been considerable efforts to reduce the jitter of frequency synthesizers over the years [10]–[21], [40]–[42]. Charge pump PLLs (CPPLLs) are widely used due to its robustness. However, a large charge pump current is required to achieve low in-band phase noise [9]. Also, the charge pump nonidealities-induced reference spur limits the PLL bandwidth [43], degrading its power efficiency [40]–[42]. Sub-sampling PLLs can attain low in-band phase noise by sampling the voltage-controlled oscillator (VCO) output with the reference clock [10]–[15]. A large phase detector (PD) gain can be obtained by utilizing the high VCO output slope, which in turn greatly suppresses the noise from the loop components. However, the sampling operation can disturb the VCO output, resulting in a high reference spur [14]. Also, the narrow capture range of the sub-sampling PD makes the loop susceptible to disturbance, therefore, an additional monitoring block is required [15]. Injection-locked clock multipliers (ILCMs) offer excellent VCO noise suppression by directly injecting the reference clock to the VCO [16]–[18]. Thanks to the instantaneous phase correction, the noise suppression bandwidth can be greater than that of conventional PLLs while low in-band phase noise is achieved in a power-efficient manner. However, due to the direct injection of the reference clock to the VCO, ILCMs are susceptible to a large reference spur, necessitating complex calibration [18]. Bang-bang PLLs (BBPLLs) are promising since they offer excellent power efficiency by making use of a low power 1-bit time-to-digital converter (TDC) as their phase detection block [19]–[21]. However, large quantization noise from the bang-bang phase detector (BBPD) can limit their in-band phase noise level.

One way to avoid the conflicting trade-offs and improve the performance of PLLs is to increase the reference frequency. A higher reference frequency can lower the in-band phase noise by reducing the charge pump noise [22], [26] or TDC quantization noise [23]. Also, the PLL bandwidth can be increased without stability or spur concerns [4], [26].

Manuscript received January 30, 2021; revised April 25, 2021 and May 24, 2021; accepted June 6, 2021. Date of publication June 25, 2021; date of current version September 24, 2021. This article was approved by Guest Editor Wei-Zen Chen. (*Corresponding author: Ji-Hwan Seol.*)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JSSC.2021.3089930>.

Digital Object Identifier 10.1109/JSSC.2021.3089930

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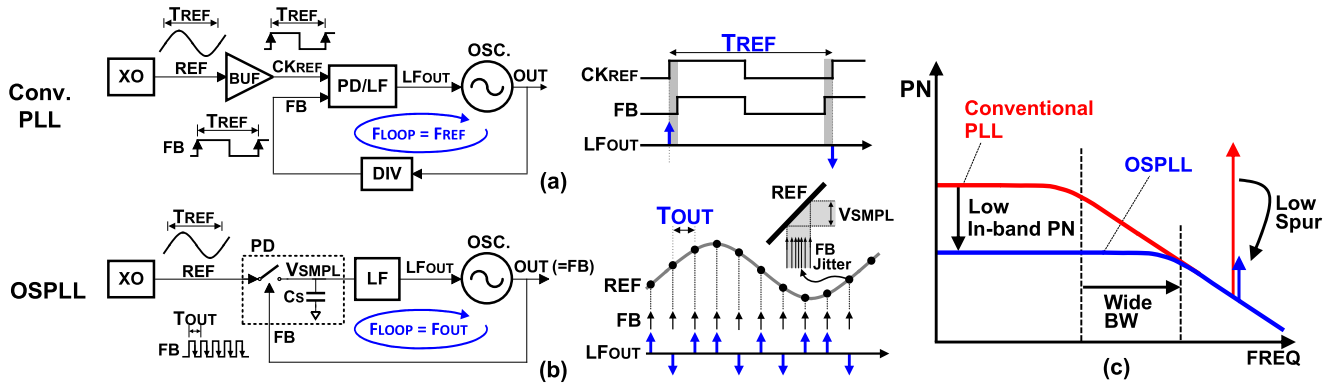


Fig. 1. (a) Operation of a conventional PLL. (b) Operation of the reference oversampling PLL. (c) Comparison between a conventional PLL and the OSPLL.

Consequently, reference boosting schemes, such as a reference doubler [24], or a quadrupler [25], [26], have become popular as a way of generating high reference frequencies without using expensive high frequency crystal oscillators. In [24] and [25] a delay line with an XOR gate is used, while Megawer *et al.* [26] employed comparators with multiple voltage references to boost the frequency of the input reference clock. However, both approaches rely on the absolute accuracy of the delay or voltage references to avoid a period error of the output clock, which can lead to a reference spur. Therefore, previous reference boosting schemes require complex calibration logic, making it hard to achieve a multiplication factor greater than four.

In this article, we present a reference oversampling PLL (OSPLL) [28] whose loop operates at the output frequency F_{OUT} , which effectively suppresses the noise from the loop components by oversampling, thereby achieving low in-band phase noise. The low in-band phase noise, in turn, enables wide bandwidth and better oscillator noise filtering, which is achieved with less stability issue and low reference spur as the loop operates at F_{OUT} rather than F_{REF} . This article also presents an LC digitally controlled oscillator (DCO) for the OSPLL with fine frequency resolution and fast switching capability. Furthermore, a timing control scheme is proposed to optimally position the varactor switching pulse for low phase noise. In combination with the low in-band phase noise and the wide bandwidth, the implemented PLL achieved 67.1-fs integrated rms jitter with 5.2-mW power consumption at 4 GHz, which leads to -256.3 FoM. The measured reference spur of the PLL was -78.1 dBc.

This article is organized as follows. Section II provides the principle and basic operation of the OSPLL. Section III discusses the design of the LC-DCO used in the proposed PLL. Section IV describes the design and implementation detail of each building block. The measurement results are presented in Section V, and conclusions are then drawn in Section VI.

II. PRINCIPLE OF THE REFERENCE OSPLL

To better explain the principle of the proposed OSPLL, we compare the OSPLL with a conventional PLL whose loop operates at every reference cycle T_{REF} , as shown in Fig. 1(a). The reference clock of the PLL is generated from a crystal oscillator (XO). Since the XO output (REF) is a sinusoidal

waveform, it is first converted to a square wave by a reference buffer (BUF). The output of the reference buffer CK_{REF} is then applied to a PD. The PD compares the positive edges of CK_{REF} to those from the feedback clock, FB, which is the divided oscillator output clock. The PD operates at every T_{REF} cycle, which is the period of CK_{REF} and FB. The PD output is then applied to the loop filter (LF), and the LF output LF_{OUT} drives the oscillator, suppressing the oscillator noise. In this case, the reference and PD noise are amplified by the frequency division ratio (N). Also, the reference buffer can induce large noise and/or power when it converts the sinusoidal reference, which has a slow slope, to a square wave [10].

Fig. 1(b) shows the conceptual diagram of the OSPLL [27], [28]. Without a reference buffer, the sinusoidal reference REF is directly applied to the sampling switch input. The switch samples its input at the falling edge of the oscillator output FB, which is the same as OUT, forming a PD. The PD of the OSPLL is based on the sampling circuits whose output voltage is proportional to their input phase error with the gain defined by the slope of the reference clock dV_{REF}/dt [29]. As the PD samples the phase error at every T_{OUT} , the loop now operates at a F_{OUT} rate, noise from the loop components is effectively suppressed by oversampling. This is illustrated in Fig. 1(b), where the black dots represent the sampling points, and the phase error of FB is converted to the sampled voltage V_{SMPL} . Note that different dc value at the sampling points is addressed using N interleaved PDs implemented with the ac coupling scheme, which will be explained later in this section. The extracted phase error at every FB edge then drives LF and its output LF_{OUT} suppresses oscillator noise. In other words, the OSPLL loop operates in F_{OUT} not F_{REF} , simultaneously enabling low in-band phase noise, wide bandwidth, and low spur as shown in Fig. 1(c). In addition, since the OSPLL directly samples the sinusoidal reference from the XO, no reference buffer is needed, improving power efficiency and output phase noise.

Fig. 2(a) shows the detailed structure of the proposed OSPLL. N reference sampling PDs (RSPDs) directly sample the input reference sinewave REF from the XO. $\Phi(1:N)$ denotes the time-interleaved sampling clocks generated from the DCO output (OUT) so that the effective sampling period of the RSPDs is the DCO period T_{DCO} while each RSPD operates in T_{REF} , relaxing the speed requirements. The RSPD

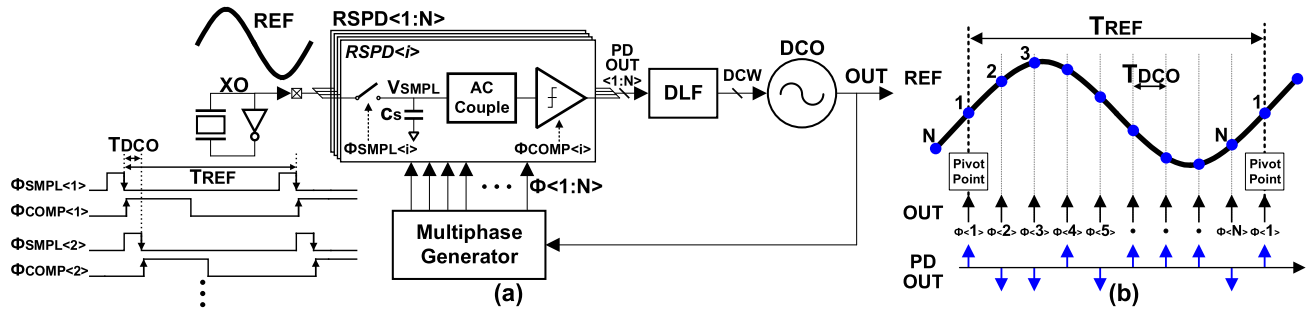


Fig. 2. (a) Simplified block diagram of the OSPLL. (b) Conceptual diagram of the sinusoidal reference and the RSPD sampling points.

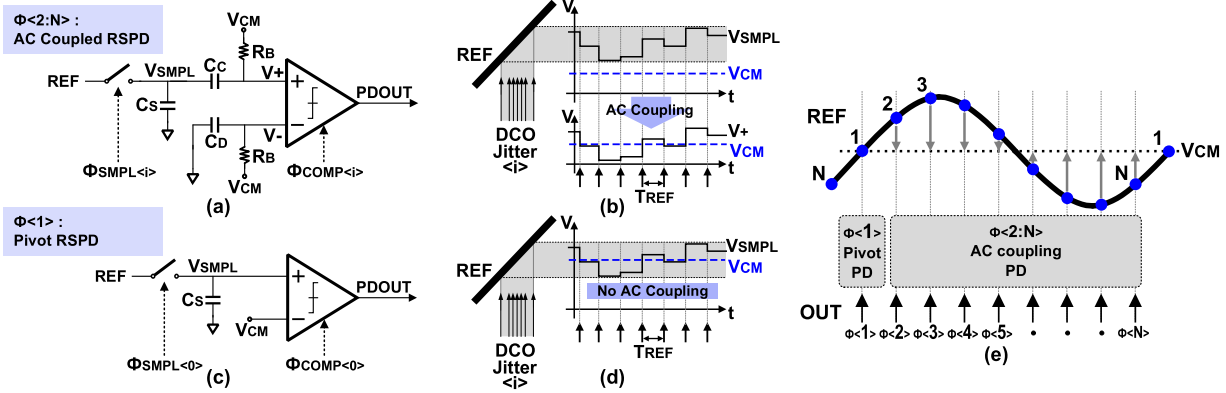


Fig. 3. (a) RSPD with the ac coupling. (b) Operation of the RSPD with ac coupling scheme. (c) Pivot RSPD. (d) Operation of the Pivot RSPD. (e) Assignment of the pivot RSPD and ac coupled RSPDs according to the RSPD index.

sampling clock $\Phi<1:N>$ is generated from the multiphase generator, driven by OUT. Each RSPD operating at $\Phi<i>$ receives $\Phi_{SMPL}<i>$ and $\Phi_{COMP}<i>$ to control the sampling switch and the comparator, respectively, in the corresponding RSPD<i>. At the falling edge of $\Phi_{SMPL}<i>$, REF is sampled on a sampling capacitor C_S . Assuming there is no noise in OUT, each RSPD samples an identical point of the sinewave reference REF, marked with a blue dot with corresponding RSPD index as shown in Fig. 2(b). Jitter in OUT will then cause a change of the sampled voltage, which represents the phase error. Therefore, the nominal dc value of V_{SMPL} is constant, and the voltage fluctuation due to the DCO jitter is superpositioned on the dc voltage. The sampled voltage V_{SMPL} is then quantized by a comparator at the rising edge of $\Phi_{COMP}<i>$ to produce 1-bit PD output PDOUT<i>, which indicates the phase of OUT either leads or lags the phase of REF. An ac coupling capacitor is placed between the sampling capacitor and the comparator to remove the dc voltage of V_{SMPL} . PDOUT<1:N> is then converted to DCO control word (DCW) by the digital loop filter (DLF) and fed to the DCO, forming a bang-bang PLL (BBPLL) operating at every DCO cycle.

Since each RSPD samples different points of the sinusoidal reference REF, the sampled voltages of the RSPDs have different nominal dc values, which raise several issues. In order for the comparator to accurately quantize the phase error, the sampled voltage must be compared with a reference voltage representing the nominal voltage of the sampling point. As each RSPD samples a different point of the sinusoidal reference clock, N voltage references that accurately represent

the sampling points are needed, which is impractical. The different common mode levels of each comparator also make it difficult to optimize the comparator. The ac-coupling scheme shown in Fig. 3(a) solves this issue by removing the dc of the sampled voltage, so that only a single reference voltage can be used for every RSPD. The dc level of V_{SMPL} is blocked by C_C and only the ac fluctuation caused by the output jitter is passed to the comparator input, which is biased at V_{CM} using a large resistor. Note that the other comparator input, V_- , is also biased at V_{CM} through the same type of resistor. Therefore, the comparator can operate at its optimal common mode voltage, V_{CM} . This ac coupling operation is illustrated in Fig. 3(b). The DCO jitter is converted to V_{SMPL} and then its dc level is shifted to around V_{CM} through ac coupling.

Since only ac fluctuations of the phase error can be detected through the coupling capacitor, an RSPD with ac coupling cannot provide absolute dc phase locking. Therefore, one of N RSPDs, RSPD(1), is designed as a pivot RSPD, without the ac coupling capacitor, to achieve absolute dc phase locking as shown in Fig. 3(c). The comparator reference voltage of the pivot RSPD is set to V_{CM} , which is also the positive zero crossing point of REF, so that it can provide the pivot position of the phase locking at the REF zero crossing while the sampling points of the other RSPDs are defined relative to the pivot position as shown in Fig. 3(e). Fig. 3(d) shows the operation of the pivot RSPD where the sampled voltage V_{SMPL} is directly compared with V_{CM} to provide dc phase locking point.

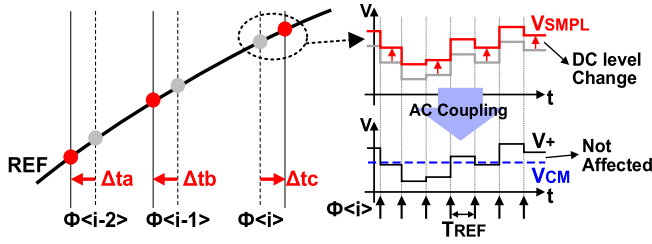


Fig. 4. Conceptual diagram that the static multiphase error, denoted as Δt_a , Δt_b , Δt_c , does not affect the comparator operation.

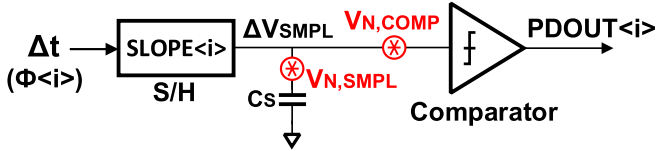


Fig. 5. Noise source of the RSPD.

As the ac coupling scheme effectively blocks the dc variation of the sampled voltage, the proposed RSPD is insensitive to the multiphase error between sampling clock $\Phi(1:N)$, or the distortion of the input sinewave reference. The sampling clocks, $\Phi(1:N)$, are generated from the multiphase generator and distributed to each RSPD. Mismatch in the multiphase generator and the wire delay can create multiphase error between $\Phi(1:N)$. This static phase error can move the sampling point slightly, resulting in the dc voltage shift at V_{SMPL} as shown in Fig. 4. However, the dc voltage shift in V_{SMPL} is blocked by the ac coupling capacitor and it does not affect the 1/0 probability at the comparator output. Likewise, the distortion of the sine reference is blocked by the ac coupling. Therefore, the multiphase error and the reference distortion do not create a reference spur at the PLL output, which is verified by simulation.

The intrinsic noise of an RSPD is composed of sampling noise ($V_{N,SMPL}$) and comparator noise ($V_{N,COMP}$) as shown in Fig. 5. The noise power generated by the two noise sources is identical for every RSPD. However, the input jitter-to-sampled voltage gain, represented by $\Delta V_{SMPL}/\Delta t$ at RSPD(i), depends on the slope (SLOPE(i)) of the sinusoidal reference where the RSPD(i) samples, which can be expressed as follows:

$$\begin{aligned} \Delta V_{SMPL} &= \text{SLOPE}(i) \cdot \Delta t \\ &= \frac{d}{dt}[A_{REF} \sin(\omega_{REF} t)] \cdot \Delta t, \quad t = \frac{i-1}{N} T_{REF} \\ &= A_{REF} \omega_{REF} \cos\left(2\pi \frac{i-1}{N}\right) \cdot \Delta t \end{aligned} \quad (1)$$

where A_{REF} is the amplitude of the input sinusoidal reference. The main implication of (1) is that due to the different slopes of the sinusoidal reference that each RSPD samples, the gain from the timing jitter Δt to the sampled voltage differs for each RSPD, as does the SNR of each RSPD. For example, near the zero-crossing point of the reference clock, the input slope is steeper, thus the gain from Δt to ΔV_{SMPL} is higher as

shown in Fig. 6(a). This high gain suppresses the subsequent noises $V_{N,SMPL}$ and $V_{N,COMP}$, providing excellent Δt detection. On the other hand, when the sampling points are near the peak, the gain is small, so the RSPD output is mostly dominated by $V_{N,SMPL}$ and $V_{N,COMP}$ rather than Δt .

For the optimal noise performance of the PLL, it is beneficial to emphasize the RSPDs that sample steeper points of REF compared with the RSPDs that sample REF near its peak points. For this, we set a different proportional path gain PGAIN(1:N) for each RSPD, so that the gain of each RSPD is proportional to the slope of the sampling points, which is quadrature to the reference clock, REF, as shown in Fig. 6(a). Note that it is even possible to remove the RSPDs near the peak/bottom which has near zero PGAIN value to save area and power. Fig. 6(b) shows the simplified structure of the proposed DLF, where the RSPD output PDOUT(1:N) is multiplied by the corresponding proportional path gain PGAIN(1:N), realizing the gain profile in the proportional path output UP/DN(1:N). Note that for the integral path, only one of the PDOUTs, PDOUT(1), is used to lower the operation speed and save power.

A discrete time domain model [30], shown in Fig. 7, is adopted to simulate the PLL noise and optimize its design parameters. The periodically time variant parameters such as SLOPE[i] and PGAIN[i] are modeled as shown in Fig. 7, while the index i is calculated as $\text{MOD}_N[k] + 1$. MOD_N is a modulo- N operation, and k is the index of the timestamps of the simulation, which increases by 1 at every T_{DCO} . In other words, the entire model operates in a single DCO clock domain. The reference sampling operation is modeled with a gain block with the gain of SLOPE[i] as derived in (1), and the sampling noise is added at its output. The comparator model is composed of a 1-bit quantizer and a latency block, Z^{-D} , that models the comparator evaluation time ($D = 6$ in the implementation, where D represents the number of DCO cycles). Also, the input referred noise of the comparator $V_{N,COMP}[k]$ is added to the input of the quantizer. The DLF consists of a proportional path and an integral path. The proportional path is modeled with the periodically varying gain PGAIN[i], which is proportional to SLOPE[i] with the amplitude of β . The integral path sub-samples its input when $\text{MOD}_N[k] = 0$ because the integral path only utilizes PDOUT(1). The sampled output is then applied to the integrator and the integral gain alpha. The output of the DLF is followed by the DCO, which is modeled as an integrator with a gain of K_{DCO} and the DCO noise $t_{N,DCO}[k]$ added at the output. The DCO output is fed back to the input, forming a PLL loop.

Fig. 8 shows the simulated output phase noise spectrum of the proposed OSPLL model. The number of the RSPDs (N) in the OSPLL is 20 and the reference frequency is 200 MHz, resulting in a 4-GHz output frequency. In order to show the advantage of the proposed OSPLL architecture, a conventional BBPLL is also simulated and its phase noise spectrum is plotted in Fig. 8. Compared with the BBPLL, the OSPLL achieved 10.1 dB of in-band phase noise suppression; the in-band phase noise of the OSPLL and the conventional BBPLL are -132.9 and -122.8 dBc/Hz, respectively. The

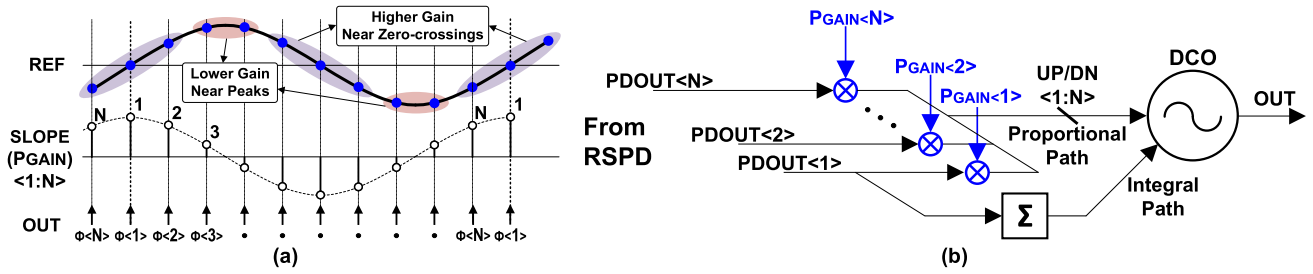


Fig. 6. (a) Different sampling gains due to the different reference slope. (b) Simplified structure of the proportional path with the gain profile and the integral path.

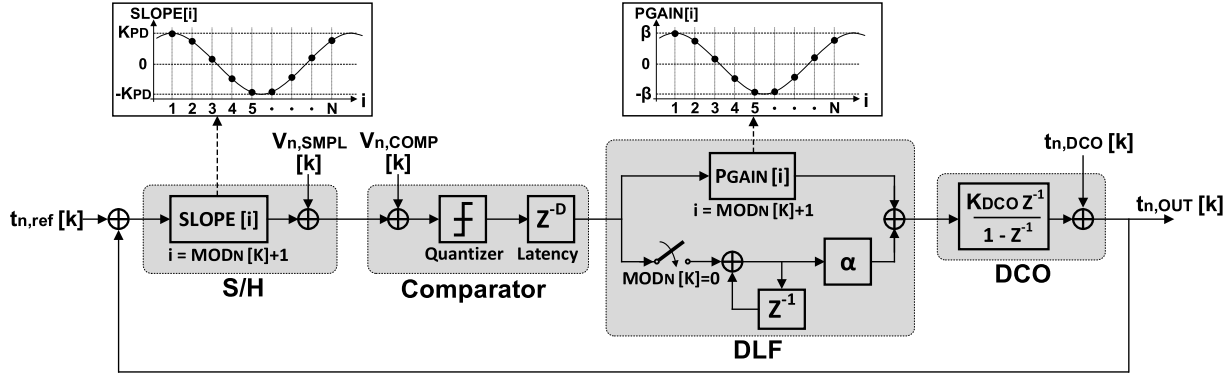


Fig. 7. Discrete time domain model of the proposed OSPLL.

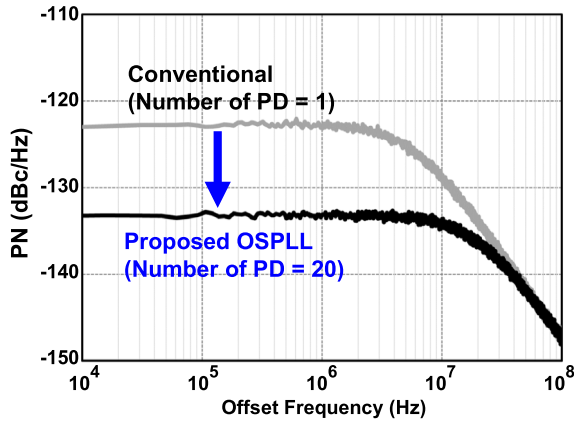


Fig. 8. Simulated phase noise plot of the proposed OSPLL ($N = 20$) and the conventional BBPLL ($N = 1$) at 4-GHz F_{OUT} and 200-MHz F_{REF} .

total integrated rms jitter of the OSPLL and BBPLL are 65 and 122.3 fs, respectively.

In the sinusoidal reference, there exists several low slope sampling points such that the RSPD output is dominated by the loop components noise. As a result, there will be an in-band phase noise amplification compared with when all sampling points have the same highest slope of the sinewave reference. This in turn lowers the in-band phase noise improvement of oversampling from $10\log N$ to $10\log N - A_N$, where A_N is the noise amplification. Fig. 9(a) shows the simulated in-band phase noise amplification with different multiplication ratio N . The noise amplification is 3 dB regardless of N when $N \geq 2$. This also agrees with the simulation results in Fig. 8,

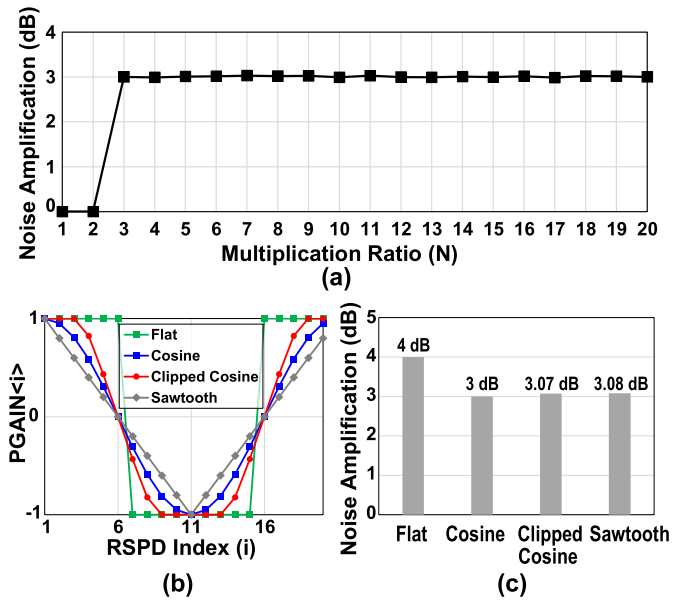


Fig. 9. (a) Simulated noise amplification due to sinusoidal reference when cosine PGAIN profile is used. (b) Tested PGAIN profile when $N = 20$. (c) Simulated noise amplification compared with flat profile when $N = 20$.

where the improvement from oversampling when $N = 20$ is $10\log N - A_N = 13 \text{ dB} - 3 \text{ dB} = 10 \text{ dB}$. Note that when $N = 1, 2$, the noise amplification is 0 dB since all sampling points have the same highest reference slope.

The effect of the time-varying proportional gain (PGAIN) on the noise amplification is verified by comparing OSPLLs

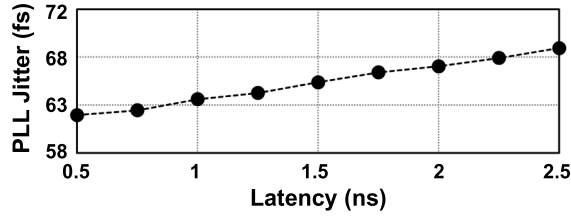


Fig. 10. Simulated PLL Jitter according to the loop latency.

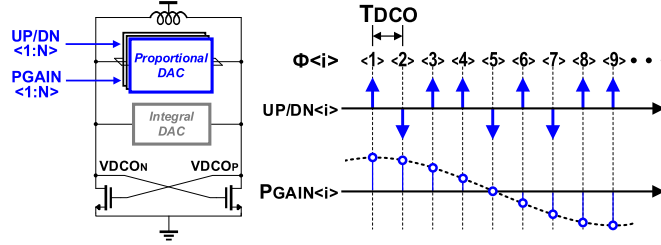


Fig. 11. Conceptual operation of the LC-DCO for the OSPLL.

operating with different PGAIN profiles, as shown in Fig. 9(b). Flat profile has the same PGAIN value for all RSPD indexes. The cosine is the profile we adopted in this design, which is quadrature to the input sinewave reference. Clipped cosine and sawtooth profiles represent steeper and more gradual slopes compared with the cosine profile. Fig. 9(c) shows the simulated in-band phase noise amplification when $N = 20$. The noise amplification of the flat and cosine profile was 4 and 3 dB, respectively, showing that 1-dB in-band phase noise improvement is achieved by using the time varying cosine PGAIN profile. Clipped cosine and sawtooth profile show 3.07- and 3.08-dB noise amplification, which is slightly worse than the cosine profile, but this implies that as long as the profile emphasize the high slope sampling points and deemphasize the low slope sampling points, the improvement is similar.

In addition to the noise of each building block, one important parameter of the OSPLL for jitter minimization is the latency of the loop, which is dominated by the comparator evaluation time modeled as Z^{-D} in Fig. 7. As the optimal loop bandwidth for the proposed OSPLL is high (~ 20 MHz) due to its low in-band phase noise level, the minimization of the latency is critical for low jitter [19]. Fig. 10 shows the simulated PLL jitter with different latency values, increasing at a 0.9-fs/250-ps rate. In this work, the latency is designed with six DCO cycles (1.5 ns) as a result of a trade-off between the latency and the comparator input transistor size. Note that even though the loop latency is multiples of the effective loop operating cycle (T_{DCO}), there is less stability or limit cycle issue since the loop time constant ($1/F_{BW}$) is much larger compared with the loop latency [45], [46].

III. DCO DESIGN FOR REFERENCE OSPLL

The design of an LC-DCO for the OSPLL introduces several requirements that differ from those of a conventional PLL. Fig. 11 shows the conceptual diagram of an LC-DCO for the

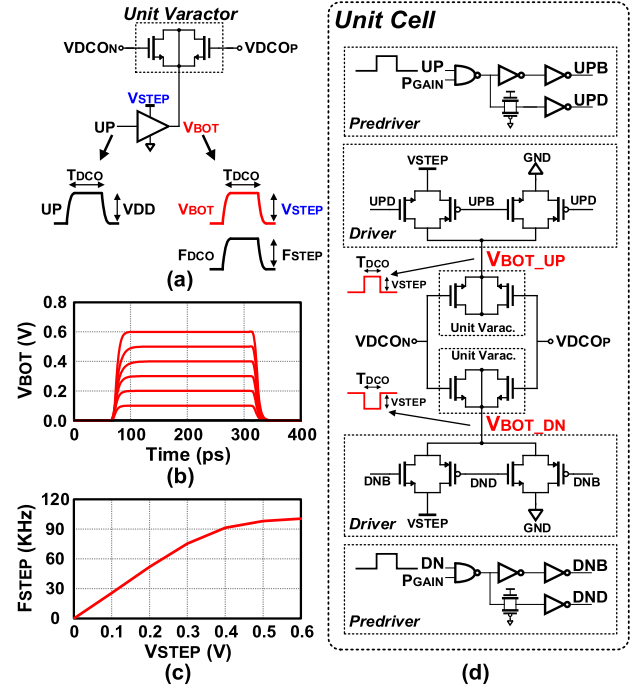


Fig. 12. (a) Conceptual operation of the unit varactor. (b) Simulated V_{BOT} when V_{STEP} is swept from 0 to 0.6 V. (c) Simulated F_{STEP} when V_{STEP} is swept from 0 to 0.6 V. (d) Detailed structure of the unit cell of the proportional DAC.

OSPLL. Phase detection is performed in every DCO cycle, as is frequency control. However, due to the F_{DCO} rate frequency control, it is challenging to support the fine frequency tuning step that is needed for the LC-DCO. According to simulation, the required frequency step of the proportional path is less than 10 kHz, which requires a sub-10-aF capacitance change. In conventional PLLs, where the loop operates in a reference cycle, this LC-DCO fine frequency step can be easily implemented using delta sigma modulator (DSM) clocked at F_{DCO} or a lower frequency [19]–[21]. However, this scheme cannot be adopted for the proportional path of the OSPLL, whose update rate is equal to F_{DCO} . In addition, the DCO needs to support the proportional path gain profile, which is proportional to the slope of the sampled reference point as explained in Section II. Therefore, the DCO should have the ability to set a different gain at each RSPD output as seen in Fig. 11.

Fig. 12 shows the structure of the unit cell of the proposed proportional DAC used in the LC-DCO to meet the aforementioned requirements of the OSPLL. Fig. 12(a) shows the principle of the unit cell operation. The unit cell consists of two NMOS varactors whose gates are connected to the $V_{DCOP/N}$ while the bottom nodes of the varactors V_{BOT} are connected to a driver whose supply voltage is V_{STEP} . This driver generates a pulse with an amplitude of V_{STEP} , which drives the varactor bottom node for one DCO cycle.

This short pulse enables fast frequency switching so that the DCO frequency can be briefly increased by F_{STEP} for one DCO cycle. The size of the frequency step, F_{STEP} , is controlled by V_{STEP} . By setting V_{STEP} sufficiently small, we can achieve

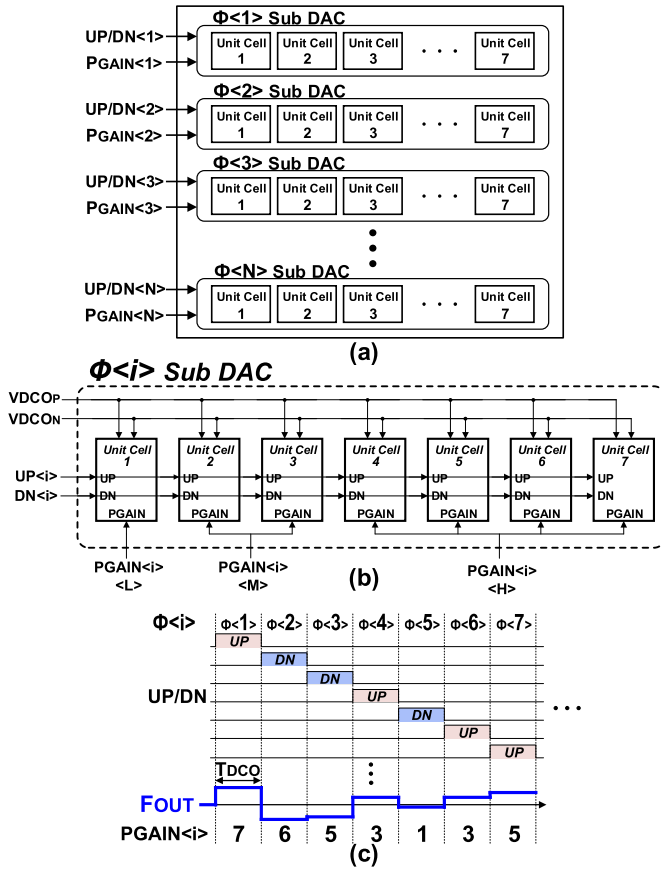


Fig. 13. (a) Structure of the proportional DAC. (b) Structure of the sub-DAC of the proportional DAC. (c) Conceptual operation of the proportional DAC.

fine frequency resolution of less than 10 kHz. Fig. 12(b) shows the simulated waveform of the V_{BOT} node of a unit varactor where V_{STEP} is swept from 0 to 0.6 V. Fig. 12(c) plots the corresponding F_{STEP} , which shows that F_{STEP} can be continuously tuned from 0 to 100 kHz. Note that the current load from V_{STEP} is less than 10 μ A, which can be supplied from a low power LDO. Fig. 12(d) shows the detailed schematic of the proposed unit cell which consists of two sets of the unit varactor and its drivers. Transmission gate type drivers are used to provide fast V_{BOT} rising/falling slope across the V_{STEP} tuning range (0–0.6 V), while delay matched pre-drivers drive the transmission gate type drivers.

Fig. 13(a) shows the structure of the proportional DAC (PDAC). To realize the proportional path gain profile, the PDAC is constructed with N sub-DACs, whose gain can be separately controlled. A sub-DAC is assigned to the output of corresponding RSPD $< i >$. Fig. 13(b) shows the sub-DAC, which consists of seven unit cells to provide gain programmability as previously described. A 3-bit PGAIN signal controls the number of unit cells that are enabled when UP/DN toggles. This enables each sub-DAC with eight-level programmability of 3-bit binary coding. PGAIN $< i >$ for each sub-DAC is pre-determined during the design phase to provide a quadrature profile to the sinusoidal reference shape. Fig. 13(c) shows the detailed operation of the proportional DAC. The DCO frequency switches according to the UP/DN pulses, and the

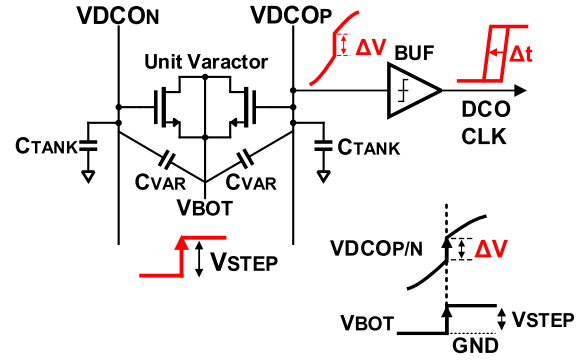


Fig. 14. Conceptual diagram that describes the phase disturbance due to the varactor switching.

size of the frequency step is controlled by the PGAIN value of each sub-DAC.

When the UP/DN pulses toggle at every DCO cycle, capacitive coupling from the varactor switching injects deterministic noise to the DCO, which may lead to an increase in PLL output jitter. Fig. 14 illustrates varactor switching, in which the bottom node of the varactor V_{BOT} rises by V_{STEP} to increase DCO frequency. This voltage transition injects charge into the DCO tank due to charge feedthrough, causing a voltage fluctuation ΔV at the DCO waveform $V_{DCOP/N}$. ΔV is determined by the capacitance divider ratio, expressed as follows:

$$\Delta V = \frac{C_{VAR}}{C_{VAR} + C_{TANK}} V_{STEP} \quad (2)$$

where C_{TANK} is the total tank capacitance of the LC-DCO, and C_{VAR} is the capacitance between V_{BOT} of a varactor and the C_{TANK} , which includes the varactor gate channel capacitance, the gate-to-drain/source overlap capacitance, and the parasitic capacitances due to layout. This voltage fluctuation can cause a phase disturbance of the DCO waveform by directly shifting its zero-crossing, resulting in jitter increase. To minimize such a side effect, we need to: 1) minimize the ΔV upon varactor switching and 2) prevent the created voltage fluctuation from disturbing the zero-crossing of the DCO waveform.

The magnitude of ΔV depends on the tank capacitance C_{VAR} as in (2), which varies according to the varactor switching location with respect to the DCO waveform as shown in Fig. 15(a) and (b). As an example, the gate capacitance is small when V_{DCO} is low because the varactor is in depletion mode. Therefore, it is preferable to switch V_{BOT} at the valley point of V_{DCO} . On the other hand, the varactor switching at the peak point of V_{DCO} should be avoided as the large varactor capacitance results in a large ΔV .

ΔV then causes DCO output phase disturbance by altering the zero-crossing point of the waveform, and the amount of the phase disturbance depends on the location of the varactor switching with respect to the DCO sinusoid, as described by the impulse sensitivity function (ISF) [31]. As shown in Fig. 15(c), if ΔV occurs near the peak/valley of V_{DCO} , the translation from ΔV to phase disturbance is minimized. However, the phase disturbance due to ΔV is maximum near the V_{DCO} zero crossings.

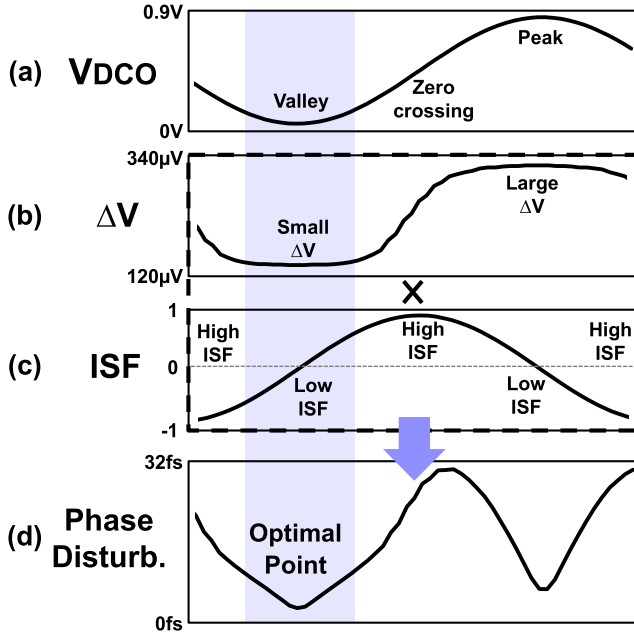


Fig. 15. Simulated phase disturbance due to the varactor switching (simulation condition: $TT/25^\circ\text{C}/V_{STEP} = 0.3\text{ V}/PGAIN = 111$). (a) DCO waveform. (b) Voltage disturbance due to the varactor switching according to the switching position. (c) Normalized ISF of the DCO. (d) Phase disturbance of the DCO according to the varactor switching position.

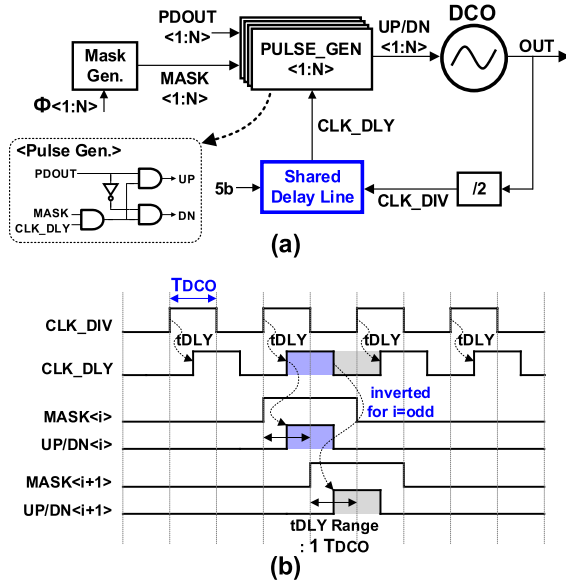


Fig. 16. (a) Proposed DCO tuning pulse timing control scheme. (b) Timing diagram.

Therefore, to minimize the phase disturbance, the varactor needs to be switched at the valley point of V_{DCO} where both ΔV and the ISF can be minimized. Near the zero crossing is not the optimal point due to the high ISF. The peak of V_{DCO} is also not the optimal point due to the high C_{VAR} . Fig. 15 illustrates the simulation results of ΔV , normalized ISF, and phase disturbance, clearly showing that the valley of V_{DCO} exhibits minimum phase disturbance due to the varactor switching.

To ensure the optimal timing for varactor switching at the DCO, the timing that UP/DN pulses reach the DCO should be controlled. Fig. 16 shows the control scheme for

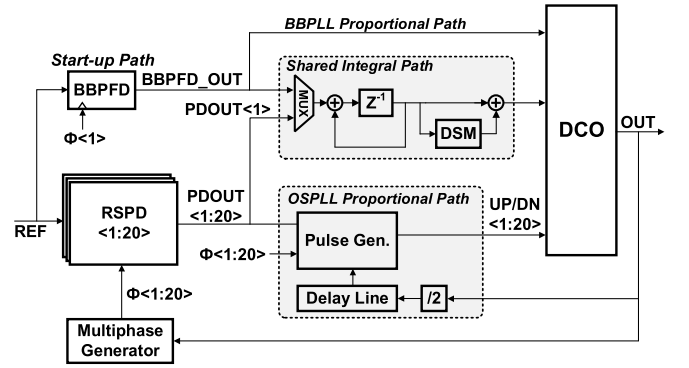


Fig. 17. Overall structure of the proposed OSPLL.

the DCO tuning pulse, which generates UP/DN pulses with a programmable delay line to position them at the optimal varactor switching timing. Similar to [32], a digitally controlled delay line is used to control the timing of the UP/DN pulses. Instead of using N different delay lines for N UP/DN pulses, which incurs area overhead, we used a single shared delay line as shown in Fig. 16(a). The DCO output is first divided by two before it is applied to the delay line to lower the power consumption of the delay line. The delay line output, CLK_DLY, then drives the N pulse generator unit, PULSE_GEN <1:N> where the CLK_DLY is multiplied by MASK <1:N> to select the corresponding pulse from CLK_DLY and generate UP/DN <1:N>, as shown in Fig. 16(b). Note that in the PULSE_GEN <i> unit with odd index, CLK_DLY is inverted before it is multiplied by MASK <i> to maintain the same UP/DN polarity. In Fig. 16(b), tDLY is the delay of the delay line, which is controlled with a 5b control word to set the timing of the UP/DN pulses. To cover the optimal range shown in Fig. 15(d), the delay range of the delay line is larger than $0.5 \times T_{DCO}$ range considering the PVT variation. The delay code is set during the test time for optimal jitter, and the measurement results are discussed in Section V.

IV. PLL DESIGN AND IMPLEMENTATION

A. Overall Architecture

Fig. 17 shows the overall architecture of the proposed PLL: 20 RSPDs are used in this design, so that the PLL can generate integer- N multiplication of the reference frequency by 20 or less. The multiphase generator is clocked by OUT and generates the interleaved clocks $\Phi_{SMPL}(1:20)$ and $\Phi_{COMP}(1:20)$, which drive the RSPDs. The outputs of the RSPDs, PDOUT <1:20>, are applied to the DLF, which is composed of a proportional and an integral path. The proportional path contains a DCO pulse generator, and a delay line whose input is a divided-by-two clock of the DCO output. The integral path is used for the type-II operation to provide better DCO flicker noise suppression and a zero phase offset. For the integral path, only one of the RSPD outputs, PDOUT <1>, is used to reduce its operation speed and power consumption. The 11 LSBs of the integrator are applied to DSM to obtain fine frequency resolution. The design also includes a startup

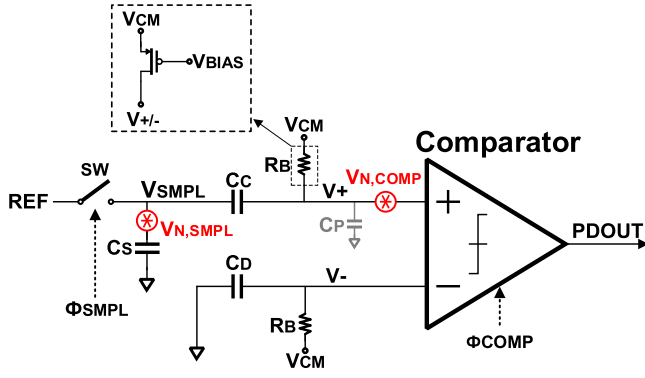


Fig. 18. Detailed schematic of the RSPD with its noise source.

path for wide and robust initial locking. When the PLL is turned on, the startup path using a conventional bang-bang phase and frequency detector (BBPFD) achieves initial phase and frequency lock. Then, the startup path is disabled, and the reference oversampling path takes over the loop. The startup path shares the integral path with the reference oversampling path to save area whereas the output of the BBPFD directly drives the DCO for the proportional path.

B. Reference Sampling Phase Detector

Fig. 18 shows the detailed schematic of the RSPD. An NMOS transistor driven by bootstrapped Φ_{SMPL} is used as a sampling switch (SW). The sampling capacitor C_S , the ac coupling capacitor C_C , and the dummy capacitor C_D are implemented with MOM capacitors.

It is important to optimize the noise and power of the RSPD, since the in-band noise of the PLL is dominated by the RSPD and its power takes up a large portion of the total PLL power. The RSPD noise mainly comprises comparator noise ($V_{N,COMP}$) and KT/C_S sampling noise ($V_{N,SMPL}$). The reduction of $V_{N,COMP}$ requires more comparator power, while a larger area is needed to reduce $V_{N,SMPL}$. In this design, we first set the noise of the comparator given the PLL total power budget, with the goal of achieving optimal PLL jitter-power efficiency [33]. We then decide the size of the sampling capacitor so that the sampling noise does not dominate the overall RSPD noise. According to the behavioral simulation, the required input referred noise of the comparator is $100 \mu V$.

Next, given the comparator noise, we determine the size of capacitors C_S and C_C . Maximizing the sampling capacitor C_S is advantageous for reducing the sampling noise. At the same time, the coupling capacitor C_C should also be large to minimize the signal attenuation due to the parasitic capacitance C_P at V_+ node, which can be represented as follows:

$$\Delta V_+ = \frac{C_C}{C_C + C_P} \Delta V_{SMPL}. \quad (3)$$

Therefore, given a fixed total capacitance, C_{TOT} , there exists an optimal C_S to C_C ratio. Fig. 19(a) shows the simulated PLL jitter, when C_S is increased and C_C is decreased for a fixed C_{TOT} . When C_S is small, the sampling noise dominates the comparator noise. Hence, increasing C_S can improve the

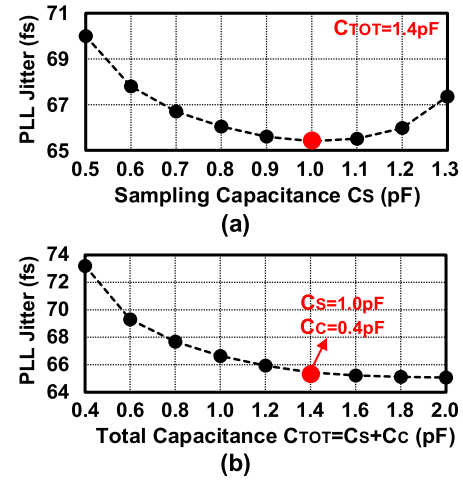


Fig. 19. (a) Simulated PLL jitter according to C_S with $C_{TOT} = 1.4$ pF. (b) Simulated PLL jitter according to C_{TOT} . Optimal C_S/C_C ratio is used for each point, which was obtained using the method in (a).

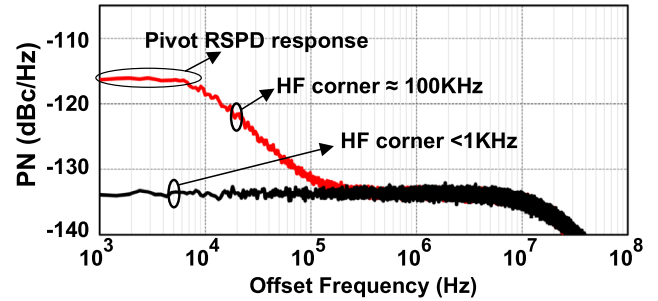


Fig. 20. Simulated PLL phase noise plot with different HF corner of the ac coupling path.

PLL jitter in this region. However, as C_S becomes larger, the signal attenuation effect due to a smaller C_C starts to degrade the PLL jitter. Therefore, the optimal ratio between C_S and C_C can be determined for minimum PLL jitter. Fig. 19(b) shows the PLL jitter with different C_{TOT} values, where the optimal C_S/C_C ratio is used for each C_{TOT} . As shown in the figure, the PLL jitter improvement diminishes as C_{TOT} is increased, and eventually saturates as the comparator noise starts to dominate the sampling noise. Thus, we set C_{TOT} to 1.4 pF, the point beyond which increasing C_{TOT} gives negligible jitter improvement considering the area increase (< 0.1 fs per 100 fF). The capacitances of C_S and C_C are set to 1 pF and 400 fF, respectively, yielding the optimal C_S/C_C ratio. Note that a matching capacitor, C_D , which is equivalent to the series capacitance of C_S and C_C (300 fF), is attached to the negative terminal of the comparator to minimize the comparator offset induced by the impedance mismatch.

The bias resistor R_B sets the high pass corner of the ac coupling path. Its value should be sufficiently low, otherwise it will block the low frequency component of the RSPD input phase error information, degrading the phase noise. As shown in Fig. 20, the low frequency phase noise increases if the high pass corner frequency is large (≈ 100 kHz). Note that the phase noise flattens again around 10 kHz due to the pivot RSPD.

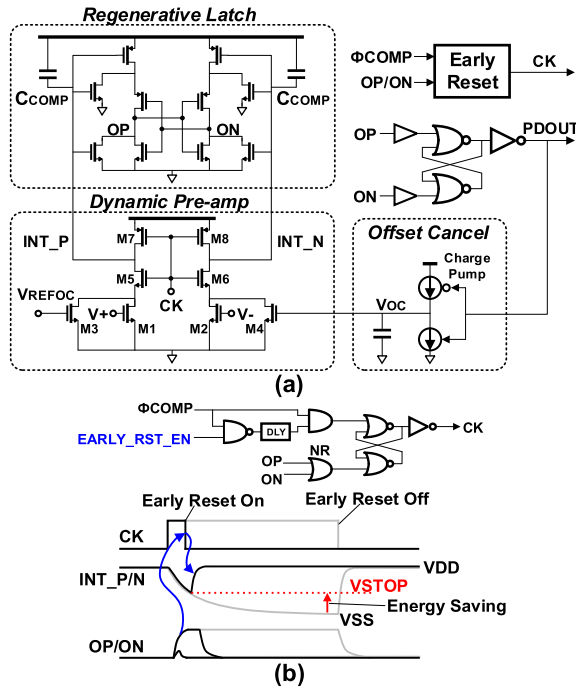


Fig. 21. (a) Detailed structure of the comparator in an RSPD. (b) Early reset scheme and its operation.

In this design, the high pass corner is set to a sufficiently low value (below 1 kHz) using a PMOS transistor biased in the sub-threshold region to avoid phase noise degradation at low-offset frequency. Note that V_{BIAS} for the resistor is generated from a diode connected replica transistor with current source load to reduce the resistance variation with PVT. Since V_{\pm} node is biased with high resistance, the input transistors of the comparator are designed with thick gate transistors to minimize the gate leakage.

C. Comparator of the RSPD

The comparator dominates the noise and power of an RSPD, making its optimization critical. Fig. 21(a) shows the schematic of the two-stage dynamic comparator adopted in this design [34]. It consists of a dynamic preamplifier followed by a regenerative latch. The comparator is in reset phase when CK is low, pre-charging INT_P/N node to VDD. As CK goes high, the input transistors M1, 2 start to discharge INT_P/N with a differential current in proportion to its input voltage difference, providing a voltage gain. When the voltages reach the latch threshold of the second stage, the latch outputs OP/ON are fully regenerated to the rail-to-rail digital level by the positive feedback. Note that the clock gating transistors M5 and M6 are placed at the drain side of the input transistors M1 and M2, instead of their source side to reduce kickback when CK toggles.

Comparator noise is mainly determined by pre-amplifier noise since the gain of the first stage pre-amplifier suppresses the noise from the second stage latch. Adding capacitor C_{COMP} at the integration node (INT_P/N) reduces the noise level by narrowing the noise bandwidth [35]. In this design, a 430-fF C_{COMP} was used to meet the target input-referred comparator

noise of 100 μV . Adding C_{COMP} inevitably increases comparator power consumption, since C_{COMP} is fully charged to VDD and then discharged to VSS in every cycle, consuming $2 \times f_{\text{REF}} \times C_{\text{COMP}} \times V_{\text{DD}}^2$. To reduce comparator power consumption while maintaining its noise performance, we adopted the early reset scheme [36] as shown in Fig. 21(b). The early reset scheme can reduce the energy dissipated in the capacitor by stopping capacitor discharge once comparator evaluation is finished. As shown in Fig. 21(b), the NOR gate NR resets the S-R latch when either OP or ON is asserted, thereby stopping the discharge of the INT_P/N node at the V_{STOP} level. As a result, power consumption is reduced to $2 \times f_{\text{REF}} \times C_{\text{COMP}} \times (V_{\text{DD}}^2 - V_{\text{STOP}}^2)$. Note that signal EARLY_RST_EN is added to turn on/off the early reset scheme for test purposes. The measurement result confirmed 25% power saving without phase noise degradation, when the early reset scheme is turned on.

In addition to its noise, the offset of the comparator should be minimized to ensure proper operation of the RSPD. If the offset is large, the output of the comparator can be dominated by the offset rather than the input phase error. In this case, the comparator output can be skewed to either one or zero, generating a spur at the PLL output and degrading phase noise. To remove comparator offset, we adopted continuous background offset cancellation using a charge pump as shown in Fig. 21(a) [37]. The charge pump adjusts V_{OC} based on the comparator output. V_{OC} is then applied to M3, forming a feedback loop so that offset is removed and equal probability of 1s and 0s is ensured at the output. Note that it is important to match the charge pump UP and DN currents to prevent the reference spur. The UP/DN mismatch will alter the 1/0 probability of the comparator output and create the reference spur. In this work, the UP/DN mismatch is suppressed to less than 2%, using the charge pump mismatch reduction technique [44]. We verified with simulation that the 2% charge pump mismatch creates less than -100-dBc reference spur.

It is important that the bandwidth of the offset cancellation loop is sufficiently low so that the low frequency component of the PD input is not attenuated by the offset cancellation loop, degrading PLL phase noise performance. We set the bandwidth of the offset cancellation loop lower than 1 kHz, similar to the high pass corner of the ac coupling path. The charge pump is biased with a small current to realize such a bandwidth.

D. Multiphase Generator

The multiphase generator produces interleaved clocks to drive the RSPDs. Fig. 22(a) shows the structure of the multiphase generator, which is based on a ring counter design [38]. Twenty unit cells form a closed loop in which each unit cell is composed of clock gating logic, a flip-flop, a mux, and control signal generation logic. The DCO output clock is applied to all of the unit cells as a common clock and a bypass mux is included in each cell to provide programmability of the frequency division ratio [27]. Initially, half of the unit cells are set to one while the other half are set to zero. Then the initialized signals circulate the loop when CLK toggles, generating interleaved clocks as shown in Fig. 22(b).

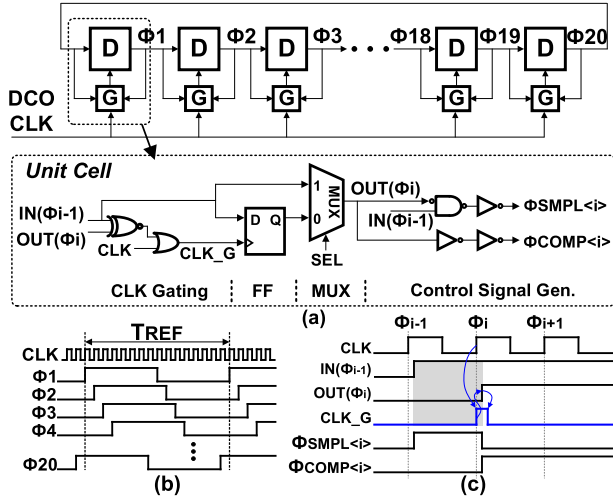


Fig. 22. (a) Proposed multiphase generator. (b) Operation of the multiphase generator. (c) Timing diagram of each unit cell.

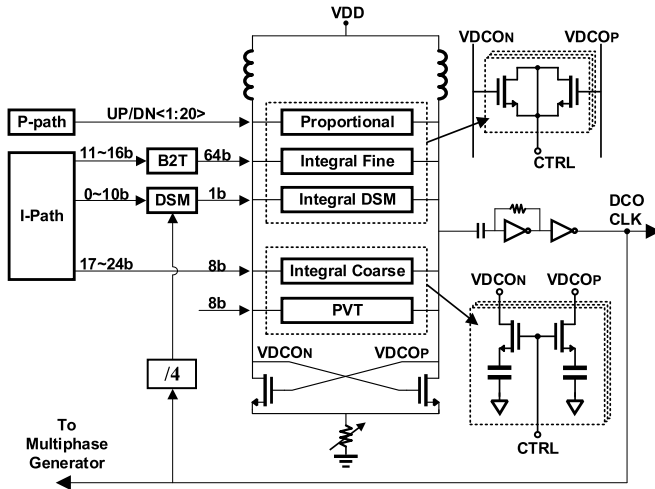


Fig. 23. Overall structure of the DCO.

To reduce the power consumption of the multiphase generator, the clock input CLK_G for the FF is gated so that CLK_G toggles only when the input and output of the unit cell are different, as shown in Fig. 22(c). The simulation result shows that the gating logic saves 20% power. The unit cell also contains a control signal generator to generate $\Phi SMPL\langle i \rangle$ and $\Phi COMP\langle i \rangle$ from Φ_i as shown in Fig. 22(c).

E. DCO

Fig. 23 shows the detailed structure of the DCO. We used digitally controlled resistors to set the DCO current instead of the current source to mitigate the flicker noise upconversion. The DAC of the DCO consists of a proportional DAC, an integral DAC, and a PVT DAC. The proportional DAC is driven by $UP/DN\langle 1:20 \rangle$ generated from the DCO pulse generator. The integral DAC is composed of a DSM DAC, a fine DAC, and a coarse DAC. Of the integral path output, 25 bit is divided into three groups and controls each integral DAC. The LSB part (0–10 bit) is applied to the DSM

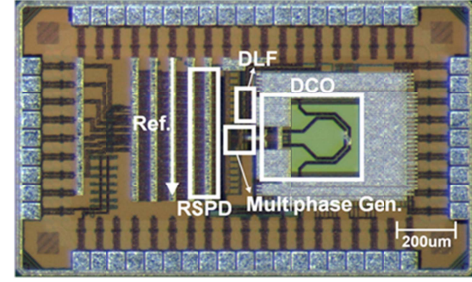


Fig. 24. Die photograph.

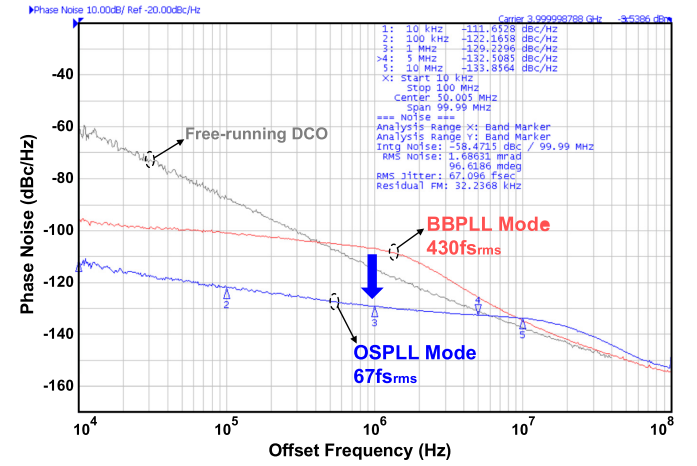


Fig. 25. Measured phase noise spectrum of the proposed OSPLL at 4 GHz.

for the fine frequency step. The middle part (11–16 bit) is converted to the thermometer code and drives the fine DAC, whereas the MSB part (17–24 bit) is applied to the coarse DAC. The DSM and the fine DAC use the varactor-based unit cell, which is the same as the one used in the proportional DAC, whereas the coarse DAC uses a MOM capacitor as its unit cell. The PVT DAC sets the coarse frequency of the DCO using 8-bit binary control code. An ac coupled inverter with resistive feedback is used to convert the DCO waveform to rail-to-rail digital output, which drives the multiphase generator, and a divide-by-4 circuit driving the DSM logic.

V. MEASUREMENT RESULTS

The proposed OSPLL is fabricated in 28-nm CMOS. Fig. 24 shows the die photograph and the PLL core occupies 0.17 mm^2 . To prevent the unwanted noise coupling to the sinusoidal reference, the reference distribution line is carefully shielded with the ground. Also, we used the thick and wide metal layer for the reference line to reduce the resistance and minimize the sinewave attenuation. The PLL generates 4-GHz output frequency using 200-MHz reference input, while consuming 5.2 mW. The reference sinusoidal clock is generated from an external crystal oscillator (Sprinter model from Wenzel Associates). A peak-to-peak 1.2-V reference signal is applied to the chip to avoid any reliability issues of the sampling switches.

Fig. 25 shows the measured phase noise spectrum of the PLL and the free-running DCO measured from a Keysight E5052B signal source analyzer. The in-band phase noise

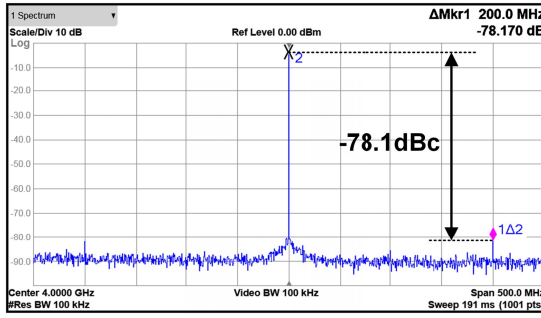


Fig. 26. Measured output spectrum of the proposed OSPLL.

is -129.2 dBc/Hz at 1-MHz offset and -132.5 dBc/Hz at 5-MHz offset. The integrated rms jitter of the PLL is 67.1 fs, and the integration range is from 10 kHz to 100 MHz. The PLL achieved -256.3 dB of PLL jitter-power FoM. The DCO phase noise in free-running mode at 4 GHz was -113.6 dBc/Hz at 1-MHz offset.

Fig. 25 also shows the measured phase noise spectrum of the proposed the conventional BBPLL mode for comparison. Note that for a fair comparison, both the OSPLL and BBPLL mode are measured with the optimal bandwidth which gives the lowest jitter. The in-band phase noise improvement of the OSPLL was larger than 20 dB compared with the BBPLL, where the in-band phase noises of the OSPLL and the BBPLL were -130 and -105 dBc/Hz, respectively. The integrated rms jitter was improved from 430 fs (BBPLL) to 67 fs (OSPLL), a greater than $5\times$ improvement.

The measured jitter performance of the BBPLL (430 fs) is worse than the simulated jitter of the conventional BBPLL in Fig. 8 (122.3 fs). We verified with simulation that this is due to the phase noise contribution from the inverter-based reference buffer of the BBPLL, which is necessary to convert the sinusoidal reference from the crystal oscillator to the rectangular pulse for the BBPFD. Since the input of the reference buffer is a sinusoidal clock with slow slope, the noise generated from the first-stage inverter is large [10]. The inverter chain reference buffer used in this design consumes $100\ \mu\text{W}$. Increased power could lower the noise contribution, but at the expense of higher overall power [21]. The proposed OSPLL avoids this issue since the OSPLL directly samples the sinusoidal reference from the crystal oscillator so that it does not need a reference buffer.

Fig. 26 shows the measured output spectrum of the proposed PLL measured from a Keysight EXA N9010B spectrum analyzer. The PLL achieved a reference spur of -78.1 dBc.

Fig. 27 shows the measured PLL output jitter according to the delay code of the proportional path timing control scheme that controls the varactor switching timing of the DCO proportional path. Across all 5-bit delay codes, the measured PLL output jitter changes from 67 to 82 fs, demonstrating the importance of the varactor switching timing control. The optimal code can be set around 11 for minimum output jitter. The range of the delay line is larger than $0.5 \times T_{\text{DCO}}$ to cover the optimal region given PVT variation.

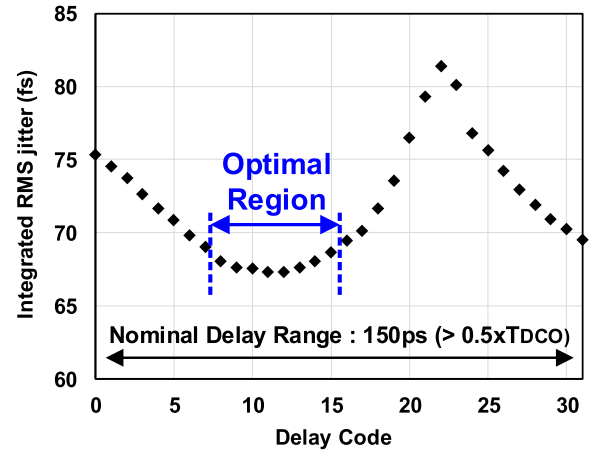


Fig. 27. Measured output jitter of the PLL with difference delay code of the DCO tuning pulse control scheme.

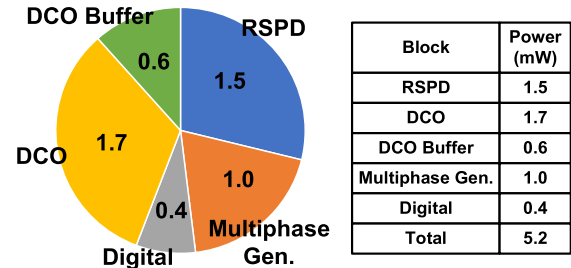


Fig. 28. Measured power breakdown of the PLL.

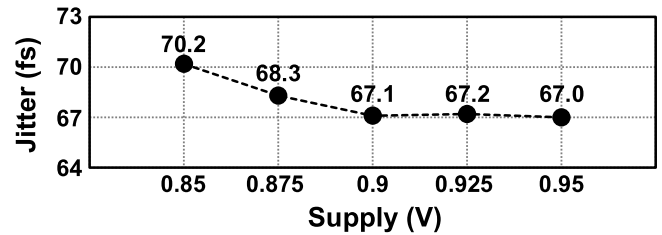


Fig. 29. Measured PLL jitter across the supply voltages.

Fig. 28 shows the measured power consumption of each building block. The RSPD, DCO, DCO buffer, multiphase generator and digital logic consume 1.5, 1.7, 0.6, 1.0, and 0.4 mW, respectively, resulting in 5.2 mW of total power. Note that three RSPDs near the peak and three RSPDs near the bottom are turned off to save power.

Fig. 29 shows the variation of the PLL output jitter across the supply voltages from 0.85 to 0.95 V. The jitter variation was less than 5%. Fig. 30 shows the jitter and reference spur measurement of five different chips. Note that the same supply, bias, and control codes are used for all chips. The jitter performance varied from 67.1 to 72.2 fs, while the spur performance measurement results range from -79.3 to -75.0 dBc.

Table I compares the performance of the proposed PLL with recent low-jitter integer- N PLLs. Thanks to the oversampling, the proposed PLL achieved the low in-band phase noise of -130 dBc/Hz. The measured bandwidth was 20 MHz, much

TABLE I
COMPARISON WITH RECENT LOW-JITTER PLLS

	This Work	RFIC 16 Ravinuthula [41]	ISSCC 18 Turker [40]	ISSCC 18 Sharkia [11]	ISSCC 19 Kim [13]	ISSCC 19 Zhang [12]	ISSCC 18 Sharma [29]	ISSCC 20 Mercandelli [39]	ISSCC 16 Elkholy [17]
Type	OSPLL	Charge-pump PLL	Charge-pump PLL	Sub-sampling PLL	Sub-sampling PLL	Sub-sampling PLL	Sampling PLL	Sampling PLL	ILCM
	Type-II	Type-II	Type-II	Type-I	Type-II	Type-II	Type-I	Type-I	Type-I
Process (nm)	28	65	16	65	65	40	65	28	65
Reference (MHz)	200	500	500	100	100	200	50	500	125
F_{BW} (MHz)	20	0.2	3	6	2	4	2	7	1
F_{BW}/F_{REF}	1/10	1/2500	1/166	1/17	1/50	1/50	1/25	1/71	1/125
F_{OUT} (GHz)	4	8	12.5	5	3.8	14	2.55	12.5	8
Int. Jitter (fs)	67.1 (69.3*)	110	53.6	185.3	72	56.4	110	51.7	104.7
Int. Range (Hz)	10K-100M	10K-20M	10K-10M	10K-50M	1K-30M	1K-100M	10K-100M	1K-100M	10K-30M
In-band PN (dBc/Hz) (Normalized to 4GHz)	-130	-104	-127.1	-122.3	-123.6	N/A	-121.3	-129	-115.6
Ref. Spur (dBc)	-78.1 (-77.5*)	N/A	-75.5	-64.1	-75	-64.6	-63	-73.5	-43
Power (mW)	5.2	140	45	1.1	19.1	7.2	3.7	18	2.7
FOM (dB)	-256.3	-237.7	-246.8	-254	-250.1	-256.4	-253.5	-253.2	-255.4
Area (mm ²)	0.17	1.48	0.35	0.01	0.21	0.23	0.36	0.16	0.27

*Averaged across 5 chips

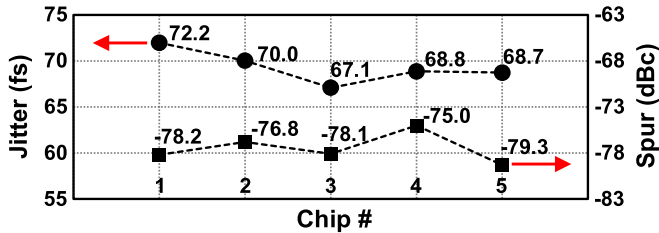


Fig. 30. Measured PLL jitter and reference spur of five chips.

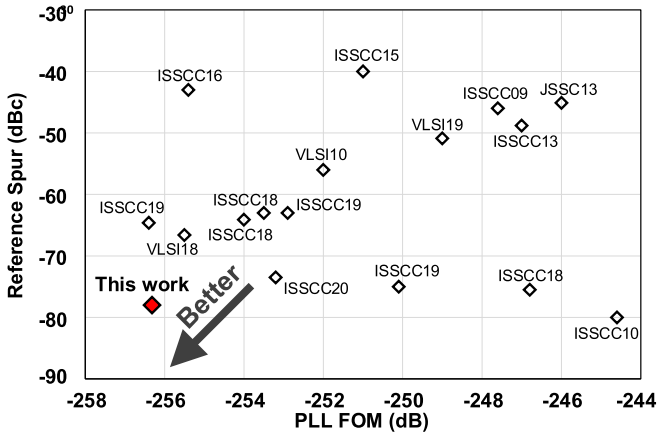


Fig. 31. Reference spur versus PLL FoM comparison plot of prior arts.

larger compared with state-of-the-art PLLs. In combination with the low in-band phase noise and the wide bandwidth, the proposed PLL achieved a sub-100-fs low-jitter performance of 67.1 fs_{rms} while maintaining excellent power efficiency, yielding a state-of-the-art jitter-power FoM of -256.3 dB. The proposed PLL demonstrated the best performance in terms of reference spur compared with the other PLLs. The performance comparison of the proposed PLL and recent

published PLLs in terms of the reference spur performance versus the PLL FoM is shown in Fig. 31. The proposed OSPLL achieved state-of-the-art performance in jitter, power, and spur among recent published work.

VI. CONCLUSION

In this article, we presented an ultralow jitter LC-DCO-based reference oversampling PLL. The reference oversampling technique effectively boosts the reference frequency to the output frequency, lowering in-band phase noise and achieving a wide bandwidth at the same time. The ac coupling technique in the RSPD removes the effect of the offset and timing mismatch of the RSPD, enabling low reference spur. Since the sinewave reference from the crystal oscillator is directly utilized, the noisy and power-hungry reference buffer in conventional PLLs can be removed. The varactor-switching noise of the LC-DCO is minimized by the proposed DCO tuning pulse timing control scheme, therefore the optimal PLL jitter performance is maintained. The proposed PLL, fabricated in 28-nm CMOS, achieved 67.1-fs_{rms} measured jitter performance and 5.2 mW of power consumption at 4 GHz, resulting in -256.3 -dB PLL FoM, while maintaining -78.1 -dBc reference spur.

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