CURRICULUM VITAE

David T. Blaauw

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I Personal Data

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II Employment History

A. Education

Doctor of Philosophy in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: "Functional Abstraction in Switch-Level Simulation."
Advisor: Professor Jacob A. Abraham

Master of Science in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: "Automatic Generation of Behavioral Models."
Advisor: Professor Jacob A. Abraham

Bachelor of Science in Physics with a second major in Computer Science, Duke University, May 1986.

B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

C. Employment History

• September 2007 - Present:	Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
• August 2001 - September 2007:	Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
• September 1994 - August 2001:	Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
• August 1993 - September 1994:	Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.
• August 1992 - August 1993:	Development Staff Member, IBM Corporation, Endicott, New York.

D. Honors and Awards

- Best Paper Award, Pierre Abillama, Zichen Fan, Yu Chen, Hyochan An, Qirui Zhang, Seungkyu Choi, David Blaauw, Dennis Sylvester, Hun-Seok Kim, "SONA: An Accelerator for Transform-Domain Neural Networks with Sparse-Orthogonal Weights," 34th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP), July 2023
- Selected for the ISCA 25 years retrospective (1996-2020) for year 2018: "Neural cache: bit-serial in-cache acceleration of deep neural networks," June 2023
- IEEE International Solid-State Circuits Conference Author-Recognition Award for its first 70 years as a contributor with more than 60 Papers.
- ACM/IEEE International Symposium on Microarchitecture (MICRO) Hall of Fame for co-authoring 8+ papers in Micro, October 2022
- IEEE International Symposium on Computer Architecture (ISCA) Hall of Fame for co-authoring 8+ papers in ISCA, 2022
- Best Paper Award, Andrea Bejarano-Carbo, Hyochan An, Kyojin Choo, Shiyu Liu, Dennis Sylvester, David Blaauw, Hun Seok Kim, "Millimeter-Scale Ultra-Low-Power Imaging System for Intelligent Edge Monitoring," TinyML conference, March 2022
- Highlighted paper in Nature Electronics: "Actuating sub-millimetre robots" in Proc. 2022 IEEE Int. Solid-State Circuits Conference, March 2022
- MobiCom 2021 Best Paper award "mSAIL: milligram-scale multi-modal sensor platform for monarch butterfly migration tracking". Also selected to be highlighted for the combined edition of Fall 2021/Spring 2022 SIGMOBILE Research Highlights
- 2022 Distinguished Academic Achievement Alumni Award from the Department of Computer Science at the University of Illinois at Urbana-Champaign. One award given per year.
- 2022 IEEE Micro Top Picks Special Issue on Top Picks from the 2021 Computer Architecture Conferences, Honorable Mention, "SquiggleFilter: An Accelerator for Portable Virus Detection"
- Test of Time award, "the highest honor an academic paper receives for its impact and recognizes an influential MICRO paper whose influence is still felt 18-22 years after its initial publication" for "Razor: A low-power pipeline based on circuit-level timing speculation," IEEE/ACM International Symposium on Microarchitecture, 2003, October, 2021
- Winner, 2019 Monarch Butterfly Fund for creating a system to track the flight of individual monarch butterflies on their migration to Mexico

- 2019 Distinguished University Innovator Award given to one team in the university for developing and marketing transformative ideas and technologies
- Named the Kensall D. Wise Collegiate Professor of Electrical Engineering and Computer Science, 2019
- Best Student Paper Award, "A 4×4×4-mm3 Fully Integrated Sensor-to-Sensor Radio using Carrier Frequency Interlocking IF Receiver with -94 dBm Sensitivity," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2019
- 2019 IEEE Micro Top Picks special issue on the Computer Architecture Conferences, "Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks"
- 15 year retrospective most influential paper in ISCA 2002 award for groundbreaking research in power-efficient computing, ACM/IEEE International Conference on Computer Architecture (ISCA), 2017
- Member of University of Illinois Engineering Advisory Panel. 2015 through current.
- Ranked as the top publishing author at IEEE VLSI Circuits Symposium over the last 30 years of the conference with 38 publications. June 2017
- 2016 University Researcher Award, Semiconductor Industry Association (SIA) – Semiconductor Research Corporation (SRC), established by the semiconductor industry association to recognize lifetime research contributions to the U.S. semiconductor industry by university faculty. One award given per year for circuits and technology each.
- 2016 IEEE Micro Top Picks special issue "MBus: The Missing Interconnect that Enables the Modular Millimeter-Scale Computing Class and Connects the World's Smallest Computer,"
- Best Paper Award, "Racetrack Converter: A Low Power and Compact Data Converter Using Racetrack Spintronic Devices," IEEE International Symposium on Circuits and Systems (ISCAS), May 2015
- 2014 John von Neumann Student Research Award for Excellence in Systems Research – SONIC Annual Review Meeting
- Recognized as top 50 innovator over the last 50 years graduating from the University of Illinois EECS department in 2014
- College of Engineering Innovation Excellence Award for 2013-2014
- Design Automation Conference (DAC) 50th Anniversary award for being the top 10 most cited DAC authors in DAC's 50 year history, June 2013
- Design Automation Conference (DAC) 50th Anniversary award for publishing the most papers in the fifth decade of DAC's history, June 2013
- 2013 University of Michigan Electrical Engineering and Computer Science (EECS) Department Outstanding Achievement Award for innovative research in variation-tolerant and energy efficient integrated circuit design, and exceptional mentoring and teaching in the area of VLSI circuits
- International Solid-State Circuits Conference (ISSCC) 60th Anniversary Special Recognition top 10 contributing author over the last 10 years, February 2013
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award, "Combined Dynamic Voltage Scaling and Adaptive Body biasing for Lower Power Microprocessors under Dynamic Workloads," ICCAD 2002 Conference, November 2012
- Second Prize in the 18th Samsung Human-Tech Thesis Competition for research on millimeter sensor design, February 2012

- IEEE Fellow status, January 2012
- Winner MuSyC Research Consortium annual best poster award, "A Modular 1mm^3 Die-Stacked Sensing Platform," Nov 2011
- Winner 11th International VLSI-Symposium Low Power Design Contest, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011
- Winner Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC) Design contest, "Design and Implementation of Centip3De, a 7-layer Many-Core System," Design Automation Conference (DAC)/International Solid-State Circuits Conference (ISSCC), Feb/June 2011
- Best Paper Award, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan, College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for "development of the Razor technology" (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is "at least five years old and has had a significant industrial impact."
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, "Energy Efficient Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
- Microprocessor Review Analysts' Choice Award in Innovation for "Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design," Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation"
- University of Michigan Henry Russel Award for "Exceptional Scholarship and Conspicuous Ability as a Teacher," November 2004
- Best Paper Nomination, "Parametric Yield Estimation Considering Leakage Variability," ACM/IEEE Design Automation Conference (DAC), June 2004
- Best Paper Award, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, "Noise Analysis Methodology for Partially Depleted SOI Circuits," IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003

- Best Paper Award, “Statistical Delay Computation Considering Spatial Correlations,” ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, “Pre-route Noise Estimation in Deep Submicron Integrated Circuits,” ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, “Driver Modeling and Alignment for Worst-Case Delay Noise,” ACM/IEEE Design Automation Conference (DAC), June 2001
- Best Paper Award, “On-Chip Inductance Modeling and Analysis,” ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

III Research Experience

A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

B. Doctoral Students Supervised

Student	Thesis Title/Topic	Graduation Date
Olivia Lee		In Progress
Rahul Narasimha		In Progress
Hyunwon Chung		In Progress
Mohammed Ashfakh		In Progress
Jeongtaek Chang		In Progress
Joey Costello		In Progress
Yi Shen		In Progress
Jungho Lee	Neural Stimulation In progress	In Progress
Andrea Bejarano	mm-Scale Image Sensing Through Low Power Circuit and Algorithm Co-Design	In Progress
Chien-Wei Tseng	Ultra-Low Power RF-Localization for Asset Management	In Progress
Yichen Gu	Computational Genomics for RNA Velocity Modeling	In Progress

Kuan Yu Chen	Design and Implementation of Domain-Specific Programmable Spatial Accelerators	November 2023
Rohit Rothe	Energy Efficient Circuit Design Techniques and Beyond CMOS Exploration for Internet of Things (IoT)	November 2023
Zhen Feng	Energy-Efficient Low-Power Mm-Scale Wireless Communication System	November 2022
Jihwan Seol	Energy-Efficient Mixed-Signal Circuits and Systems for Communication and Signal Processing	November 2022
Zhehong Wang	Application of New Technologies to Neural Networks Processors	December 2021
Xiao Wu	Energy Efficient Circuits and System for Internet of Things and Hardware Accelerator Design for Genome Sequencing	July 2019
Li-Xuan Chuo	Miniaturized Low-Power and Energy-Efficient RF Wireless Communication and Sensing Systems	June 2019
Ziyun Li	nergy-Efficient Mobile Computer Vision and Machine Learning Processors	May 2019
Kyojin Choo	Charge-domain analog/mixed-signal circuits and applications	Sept 2018
Yao Shi	Millimeter-Scale and Energy-Efficient RF Wireless System	Aug 2018
Wootaek Lim	Ultra-low Power Circuit Design for Miniaturized IoT Platform	May 2018
Taekwang Jang	Circuit and System Designs for Millimeter Scale IoT and Wireless Neural Recording	Dec 2017
Wanyeong Jung	Low-Power Energy Efficient Circuit Techniques for Small IoT Systems	April 2017
Supreet Jeloka	Cross-point Circuits for Computation, Interconnects, Security and Storage	Jan 2017
Yejoong Kim	Robust Circuit Design for Low-Voltage VLSI	May 2015

Nathaniel Pinckney	Near-Threshold design	July 2015
Dongmin Yoon	Low power timer references	Jan 2015
Inhee Lee	Power management for ultra-low power sensors systems	Oct 2014
Gyouho Kim	Ultra-low power visual monitoring	Aug 2014
Bharan Giridhar	Adaptive Computing	Dec 2013
Zhi Yoong Foo	Low power processor design techniques	Aug 2013
Sudhir Satpathy	Fast and low power inconnect fabrics	Dec 2012
David Fick	Adaptive Low-power design	Aug 2012
Yoonmyung Lee	Ultra Low-Power Memory Design	April 2012
Prashant Singh	Reliability analysis and wear-out detection	April 2010
Nurrachman Liu	Automatic tuning of VLSI circuits	April 2010
Brian Cline	Process variation modeling for advance semiconductor circuits	Feb 2010
Cheng Zhuo	VLSI wearout modeling	Dec 2010
Ravikishore Gandikota	Crosstalk-Noise analysis for nanometer VLSI circuits	Aug 2009
Carlos Tokunaga	Circuits and architectures for secure processing	Sep 2008
Shidhartha Das	Razor: circuit speculation for power and performance efficient design	Oct 2008
Kaviraj Chopra	Statistical timing analysis including spatial correlations	Apr 2008
Eric Karl	Reliable computing on unpredictable silicon	Mar 2008

Sanjay Pant	Power grid analysis and design	Dec 2007
Mini Nanua	Leakage and noise analysis in nano-scale technologies	Apr 2007
Bo Zhai	Dynamic voltage scaling for embedded processor designs	Mar 2007
Rajeev Rao	Modeling and design of low-power VLSI systems under for multiple sources of uncertainty	Jul 2006
Dongwoo Lee	Analysis and minimization of leakage current	May 2005
Aseem Agarwal	Statistical timing analysis for VLSI circuits	Mar 2005

C. Masters Students Supervised

Student	Thesis Title/Topic	Graduation Date
Alhad Daftardar	High Performance Computing	In Progress
Peijun Hou	Capacitance to Digital Conversion	In Progress
Li Yu Chen	High Voltage Upconversion	May 2021
Hengfei Zhong	Power Circuit Design	May 2020
Ashwin Bhat	Error Tolerant Long-Read Alignment for Genomic Sequencing	April 2020
Hyungjoo Seo	Low Power Energy Harvesting	May 2019
Tim Wesley	Low Power Neural Network Accelerators	May 2019
Yu Zeng	Low Power Crystal Oscillator Circuits	Dec 2017

Dongkwun Kim	Low Power Voltage References	May 2017
Skyler Skrzyniarz	Low Power Correlation Architectures for GPS	June 2015
Junhua Gu	Low Power Circuits for Analog to digital interfaces	May 2015
Ruochen Xie	Energy Reduction of FeRAM Memories for Millimeter Sensors	May 2015
Allen Wang	Low Power Level Conversion	May 2014
Naveen Akesh	Low Power Audio Device for Developing World	May 2014
Zhe Yu	RF Communication for Millimeter Scale Sensors	May 2014
Hsi-Shou Wu	Low Power Word-Spotting	April 2014
Siddharth Saxena	Low power correlation circuits	May 2013
Karan Jain	Low power synchronization using ambient RF signals	April 2012
Jordan LeNoach	pH sensor for millimeter sensors	Dec 2011
Jeffrey Yeh	Chip design for the developing world	April 2011
Nate Robert	Low power LDO	Dec 2010
Vikas Vinay	Low power Class-D amplifier for developing world applications	Dec 2010
Abhishek Madhaven	Low power chip design	Dec 2010
Junsun Park	Intra-cellular chip design	May 2010
Jou-ching (George) Sung	Low power ADC design	Aug 2009
Mao-Ter Chen	Low power sensor node design	Dec 2008

Sudherssen Kalaiselvan	Razor-3: A circuit speculation and SEU tolerant circuit technique	May 2007
Deepesh John	Low power design through typical-case optimization	May 2006
Yueh-Chuan Tzeng	Encryption processor for side channel attack avoidance	May 2006
Meghna Singhal	Low power design using subthreshold operation	May 2006
Amir Borna	Analysis of lithographic variations for chip performance	Aug 2005
Amit Jain	Delay modeling for non-ramp input transitions	Nov 2004
Toan Pham	Clock skew reduction using Razor flip-flops	Dec 2003
Bhavana Thudi	Non-iterative switching window computation for delay noise	May 2003
Wesley Kwong	Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs	May 2003

D. Research Grants

- National Science Foundation (NSF), "StiMote: An Ultrasmall, Modular Neurophotonic Stimulator," PI: James Weiland, $ 649,130, with $216,376 to Blaauw, 06/24/2021 – 6/23/2023
- Ministry of Defense, "Low Power Localization," PI: David Blaauw, $840,000, with $420,000 to Blaauw, 3/12/2020 - 3/31/2022
- Intel Corporation, "Valleytronics Circuit Design for Efficient Realization of Computational Logic," $555,000 to Blaauw, PI: Blaauw, 6/31/2020-6/30/23
- DARPA "Datalink Applications of DSSoC-DASH (KESTREL)," $720,000 with $360,000 to Blaauw, PI: Hun Seok Kim, 1/1/2020-1/17/2023
- Semiconductor Research Corporation (SRC), "Analog and Digital Assist Techniques to Improve Mixed-Signal," $130,000 with $65,000 to Blaauw, PI: Dennis Sylvester, 9/1/2020 - 12/31/2021
- Facebook, "Context-Aware Multi-Sensor Fusion System and SoC Integrated Circuits and Digital Signal Processing," $239,752, with $119,876 to Blaauw, PI: Dennis Sylvester, 1/1/20-12/31/21
- National Geographic Society, "M3 Monarch Migration Study," $150,000 with $75,000 to Blaauw, PI: David Blaauw, 10/11/2019-10/10/2022
- ARM, "ULP Sensor Fusion SoC for Micro Robots and Tiny IoT," $320,000 with $160,000 to Blaauw, PI: David Blaauw, 9/1/19-8/31/21

- Sony Corporation of America, “Ultra Low Power intelligent imaging sensors for the Internet of Things,” $1,493,433, with $511,041 to Blaauw, PI: Dennis Sylvester, 9/1/19-8/31/22
- Ministry of Defense “Ultra-Miniature Imager Technical Demonstrator,” $1,057,762, with $657,762 to Blaauw, PI: David Blaauw, 7/18/19-3/31/2021
- Ministry of Defense “M3 Audio-Logger,” $1,204,352, with $704,352 to Blaauw, PI: David Blaauw, 2/18/19-3/31/2021
- Semiconductor Research Corporation (SRC), “Mixed-Signal Circuits Enabling Ultra-Low Power Wireless Sensors,” $270,000, with $139,995 to Blaauw, PI: David Blaauw, 1/1/18-12/31/20
- Advanced Energy Consortium (AEC), “Millimeter Scale Down-hole Sensors,” $650,000, with $400,000 to Blaauw, PI: David Blaauw, 3/1/18-02/28/21
- National Science Foundation (NSF), “NCS FR - Elucidating the relationship between motor cortex neural firing rates and dextrous finger movement EMG for use in brain computer interfaces,” $2,276,395, with $194,603 to Blaauw, PI: Cindy Chestek, 9/1/19-8/31/23
- DARPA, “Domain-focused Advanced Software-reconfigurable Heterogeneous System-on-Chip (DASH-SoC),” $2,420,233, with $1,318,078 to Blaauw, PI: Hun-Seok Kim, 7/18/18-6/30/22
- National Science Foundation (NSF), “SHF: Medium: Compute Caches: Opportunistic Extreme Scale Parallelism in General Purpose Processors,” $300,000, with $80,579 to Blaauw, PI: Reetuparna Das, 10/1/18-9/30/20
- Leidos, “Trestle – small acoustic sensors” $1,882,300, with $983,104 to Blaauw, PI: David Blaauw, 5/3/19-2/28/2021
- National Institute of Health (NIH), “A 100μm Scale Single Unit Neural Recording Probe Using IR-Based Powering and Communication,” $429,971, with $224,890 to Blaauw, PI: David Blaauw, 9/1/18-8/31/2021
- DARPA, “Transmuter: A Reconfigurable Computer,” $5,845,690, with $1,524,096 to Blaauw, PI: Ron Dreslinski, 8/6/18-3/30/21
- DARPA, “OpenROAD: Foundations and Realization of Open, Accessible Design Integrated Circuits and Digital Signal Processing,” $1,600,000, with $248,754 to Blaauw, PI Andre Kahng, 6/1/18-5/31/22
- DARPA, “Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits,” $3,199,021, with $482,255 to Blaauw, PI: David Wentzloff, 6/12/18-6/11/20
- Leidos, “NZero Acoustic Switch (Dorado),” 930,000, with $699,424 to Blaauw, PI: David Blaauw, 11/11/17-6/30/19
- National Institute of Standards and Technology (NIST), United States Department of Commerce (DoC), “Decimeter Accurate, Long Range Non-Line-of-Sight RF Localization Solution for Public Safety Applications,” $997,873, with $310,041 to Blaauw, PI: Hun Seok Kim, 6/1/17-5/31/21
- Ministry of Defense, “Highly Size Constrained Logging Sensor Development,” $2,580,843, with $1,131,882 to Blaauw, PI: David Blaauw, 10/01/16 – 08/15/18
- Sony Electronics, Inc., “Low Power Motion Detection for the Internet of Things,” 1,193,000, with $400,000 to Blaauw, PI: Dennis Sylvester, 8/1/2016-12/31/2019
- DARPA, “Support for Porting S2CFF Design and Near-Threshold Voltage (NTV) Design Methodology to 32nm CMOS,” $310,829 to Blaauw, PI: David Blaauw, 12/8/2015-8/31/2017
- DARPA, “Near Zero-Power, Continuous Acoustic Sensing Microsystem using Active Integrated Circuits and Digital Signal Processing,” $2,505,000, with $835,000 to Blaauw, PI: Dennis Sylvester, 9/28/2015-7/31/2019

- Semiconductor Research Corporation (SRC), “Infrared-Based Power Delivery and Communication for Implanted Sensors,” $375,000 to Blaauw, PI: David Blaauw, 6/1/2015-5/31/2018
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Strategic Options and Scalability Limits,” $1,170,000, with $585,000 to Blaauw, PI: David Blaauw, 1/1/2015-7/1/2017
- ARM Ltd, “ARM III: Research into Low Energy Computer Systems,” $3,000,148, with $555,555 to Blaauw, PI: Trevor Mudge, 2015-2018
- National Institute of Health (NIH), “SCH: INT: Wireless Implantable Electronic Biosensors for Tumor Monitoring,” $1,759,460 with $849,804 to Blaauw, PI: David Blaauw, 9/22/2014 - 8/31/2018
- Ministry of Defense, “M3 mm scale computing GPS logger,” $1,352,145, with $250,000 to Blaauw, PI: David Blaauw, 04/01/14 - 03/31/16
- Ministry of Defense, “Dstl Sensor Development Kits,” $400,000, with $112,500 to Blaauw, PI: David Blaauw, 12/13/13 - 3/17/14
- Ministry of Defense, “Architectural Design Study for M3 mm Scale Computing GPS Logger,” $400,000, with $175,000 to Blaauw, PI: David Blaauw, 8/15/2013-3/14/2014
- National Science Foundation (NSF), “SHF: Small: Minimally Invasive Error Detection/Correction for Runtime Margin Elimination,” $450,000, with $252,750 to Blaauw, PI: David Blaauw, 7/2012-6/2015
- BAE Systems/United States Army, “Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT),” $400,000, with $135,000 to Blaauw, PI: Kamal Sarabandi, 9/2013-8/2016
- DARPA, “The TerraSwarm Research Center,” $4,234,183, with $1,624,897 to Blaauw, PI: Edward Lee, 1/15/2013-12/31/2017
- ARM, Ltd, “Low Power Computing for Embedded Applications,” $5,000,000, with $925,000 to Blaauw, PI: Trevor Mudge, 5/2010-5/2015
- Advanced Energy Consortium (AEC), “An Autonomous Microsystem Test-Bed for Extreme Environments: Integrating Sensor Elements, Electronics, and Packaging,” $950,000, with $226,625 to Blaauw, PI: Yogesh Gianchandani, 6/2012-12/2014
- Semiconductor Research Corporation (SRC), “Fast Power Supply Boosting for Energy-Efficient, High-Performance Processors,” $360,000, with $180,000 to Blaauw, PI: David Blaauw 8/2012 - 7/2015
- DARPA, “Systems on Nanoscale Information Fabrics (SONIC) Center,” $7,008,335, with $1,401,667 to Blaauw PI: Naresh Shanbhag, 1/2013-10/2017
- Ministry of Defense, “MM scale computing for GPS logger,” $400,000, with $175,000 to Blaauw, PI: David Blaauw
- Isocline Engineering LLC, “Power Efficient Software Define Radio (SDR) Mobile Architecture Technology for Handheld Devices,” $220,093 to Blaauw, PI: David Blaauw, 03/01/2013 - 02/28/2015
- Isocline Engineering LLC, “Programmable Microchip for Accelerating Neuromorphic Object Recognition,” $45,715 to Blaauw, PI: David Blaauw, 07/01/2013 - 12/31/2013
- QUALCOMM, “Near Threshold Computing,” $100,000, gift, 8/2011-8/2013
- Oracle, “High Performance Razor Architecture” $80,000, gift, 8/2013-8/2014
- AMD, “*In Situ* Wearout Detection and Mitigation,” $100,000, gift, with $50,000 to David Blaauw, 11/2011
- Food and Drug Administration, “Smart Rapid Palatal Expander for Pediatric Cleft and Palate Patients,” $312,000, with $136,000 to Blaauw, PI: Jeanne Nervina, 9/2011-8/2013

- National Science Foundation (NSF), "Integrating Circuits, Sensing, and Software to Realize the Cubic-mm Computing Class," $2,533,000, with $519,265 to Blaauw, PI: David Wentzloff, 08/2011 - 7/2016
- Qualcomm, "Near-Threshold Computing," $50,000, gift, PI: David Blaauw, 05/2011
- Department of Energy, "Hardware-Software Co-Design for Non-Volatile Memory in Exascale Systems," $525,000 with $202,747 to Blaauw, PI: Trevor Mudge, 1/2011-12/2013
- Intel Corporation, "A Confidence-Driven Model for Predictable Computing in Future Technologies," $249,000 with $65,916 to Blaauw, PI: Zhengya Zhang, 1/2010-10/2010
- QUALCOMM, "Adaptive Design Solutions for VLSI Circuits," $50,000, gift, 09/01/09
- National Science Foundation (NSF), "Reclaiming Moore's Law through Ultra Energy Efficient Computing," $2,778,507, with $643,700 to Blaauw, PI: Prof. David Blaauw, 9/2009-08/2014
- National Science Foundation (NSF), "Probabilistic Wearout in Nanoscale," $300,000, with $150,000 to Blaauw, PI: Dennis Sylvester, 8/2008-7/2011
- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), "Strained Si/SiGe/Ge HEterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics," $17,971,252, with $600,000 to Blaauw, PI: Steve Koester, 1/2008-12/2009
- BAE Systems/United States Army, "Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT)," $8,962,200 with $700,000 to Blaauw, PI: Kamal Sarabandi, 5/2008-5/2013
- Intel Corporation, "Adaptive Digital Design in the Nanometer Regime," $100,000, gift, 3/2008-3/2010
- Sun Microsystems, "Robust Low Voltage SRAM Design," $150,000, gift, 9/2007-9/2010
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design," $40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), "Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon," $600,000 to Blaauw, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), "A Design Optimization Framework for Process Variation Tolerance," $390,000, with $195,000 to Blaauw, PI: Dennis Sylvester, 9/2006 - 8/2009
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design" $40,000, gift, 7/2006
- Semiconductor Research Corporation (SRC), "CAD Solutions for Parametric Yield Optimization," $321,000, with $160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005-7/2008
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design" $40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), "Subthreshold Processor Design," $60,000 to Blaauw, PI: Kenneth Wise, 5/2005-5/2010
- ARM, Ltd, "Low Power Computing for Embedded Applications," $5,000,000, with approx. $1,600,000 to Blaauw, PI: Trevor Mudge, 5/2005-5/2010
- Semiconductor Research Corporation (SRC), "Optimization of Lithographic Induced Variability for Improved Circuit Performance," $161,029 to Blaauw, PI: David Blaauw, 9/2004-8/2007
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2004
- Photronics, Inc. $75,000, gift, 6/2004-5/2005
- ARM, Ltd, "Low Power Computing for Embedded Applications," $240,000, with $60,000 to Blaauw, PI: Trevor Mudge, 5/2004-5/2005

- National Science Foundation (NSF), Information Technology Research (ITR), "Collaborative Research ITR: Mobile Supercomputing," $1,900,000, with $320,603 to Blaauw, PI: Trevor Mudge, 11/2003-11/2007
- Intel Corporation, "VLSI Design Curriculum," $247,292, with $61,823 to Blaauw, PI: Richard Brown, 10/2003-10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), "Power Aware Systems," $600,000, PI: David Blaauw, 9/2003-9/2006
- IBM Corporation, Center for Advanced Studies, "Static Performance Analysis under Process and Environment Variations," $40,000, Faculty Award, 9/2003
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), "Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current," $360,000, with $160,000 to Blaauw, PI: David Blaauw, 7/2003-7/2006
- National Science Foundation (NSF), "Performance Analysis and Optimization for Nanometer Design," $375,000, PI: David Blaauw, 6/2003-6/2006
- ARM, Ltd, "Low Power Computing for Embedded Applications," $240,000, with $60,000 to Blaauw, PI: Trevor Mudge, 5/2003-5/2004
- IBM Corporation, Center for Advanced Studies, "Leakage Characterization and Analysis," $40,000, Faculty Award, 9/2002
- National Science Foundation (NSF), Information Technology Research (ITR), "Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty", $1,800,00 with $450,000 to Blaauw, PI: David Blaauw, 8/2002-8/2006
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), "Power Management for Nanometer design," $197,000, PI: David Blaauw, 10/2001-8/2003
- Semiconductor Research Corporation (SRC), "Variability in Chip-Level Performance and Signal Integrity Verification," $257,000, PI: David Blaauw, 10/2001-10/2004

IV Teaching Experience

Semester	Class	Course Number	Size	Rating (out of 5) Course/Instructor
Fall 2023	Advanced VLSI Design II	EECS 628	18	5/5
Winter 2023	Advanced VLSI Design	EECS 627	47	4.8/4/9
Fall 2022	VLSI Design I	EECS 427	53	4.9/4.9
Winter 2021	Advanced VLSI Design	EECS 627	27	4.3/4.2
Winter 2020	Advanced VLSI Design	EECS 627	26	4.5/4.3
Winter 2019	Advanced VLSI Design	EECS 627	24	4.5/4.6
Winter 2018	Advanced VLSI Design	EECS 627	18	4.08/4.75
Fall 2016	VLSI Design I	EECS 427	36	4.85/4.91
Fall 2015	Digital Integrated Circuits	EECS 312	35	4.58/4.81
Fall 2014	Advanced VLSI Design II	EECS 628	26	4.86/4.90
Winter 2014	Advanced VLSI Design	EECS 627	38	4.77/4.77
Fall 2013	VLSI Design I	EECS 427	39	4.74/4.78
Winter 2013	Introduction to Electronic Circuits	EECS 215	120	3.56/4.09
Winter 2012	Advanced VLSI Design	EECS 627	37	4.87/4.87
Fall 2011	VLSI Design I (Section 2)	EECS 427	18	4.79/4.79
Fall 2011	VLSI Design I (Section 1)	EECS 427	35	4.83/4.83
Winter 2011	Advanced VLSI Design	EECS 427	9	4.88/4.88
Fall 2010	Advanced VLSI Design II	EECS 628	19	4.81/5.00
Winter 2010	Advanced VLSI Design	EECS 627	19	4.85/4.96
Winter 2009	Advanced VLSI Design	EECS 627	23	4.75/4.75
Fall 2008	VLSI Design I	EECS 427	28	4.67/4.56
Winter 2007	Advanced VLSI Design	EECS 627	20	4.79

Fall 2006	VLSI Design I	EECS 427	31	4.89
Winter 2006	Advanced VLSI Design	EECS 627	22	4.55
Fall 2005	Topics in VLSI Design	EECS 598	12	4.25
Winter 2005	Advanced VLSI Design	EECS 627	20	4.79
Winter 2004	Advanced VLSI Design	EECS 627	35	4.59
Fall 2003	Introduction to Logic Design	EECS 270	87	4.77
Winter 2003	Advanced VLSI Design	EECS 627	36	4.61
Fall 2002	Introduction to Logic Design	EECS 270	109	4.77
Winter 2002	Advanced VLSI Design	EECS 627	40	4.31
Fall 2001	Issues in High-Performance Deep-Submicron Design	EECS 598	11	4.75

V Publications

A. Books

1. Ashish Srivastava, Dennis Sylvester and David Blaauw, Statistical Analysis and Optimization for VLSI: Timing and Power, Kluwer Academic Publishers, 2005

B. Book Chapters

1. Tutu Ajayi, Sumanth Kamineni, Morteza Fayazi, Yaswanth K. Cherivirala, Kyumin Kwon, Shourya Gupta, Wenbo Duan, Jeongsup Lee, Chien-Hen Chen, Mehdi Saligane, Dennis Sylvester, David Blaauw, Ronald Dreslinski Jr, Benton Calhoun, David D. Wentzloff, "Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation," in *IFIP/IEEE International Conference on Very Large Scale Integration - System on a Chip*, K. A. A. Makinwa, A. Baschirotto, and P. Harpe, Eds. Springer International Publishing, 2021
2. Sechang Oh, Yao Shi, Gyouho Kim, Yejoong Kim, Taewook Kang, Seok Hyeon Jeong, Dennis Sylvester, David Blaauw, "Low-Power Resistive Bridge Readout Circuit Integrated in Two Millimeter-Scale Pressure-Sensing Systems," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers: Advances in Analog Circuit Design 2018*, K. A. A. Makinwa, A. Baschirotto, and P. Harpe, Eds. Springer International Publishing, 2019
3. Sechang Oh, Wanyeong Jung, Hyunsoo Ha, Jae-Yoon Sim, David Blaauw, "Energy-Efficient CDCs for Millimeter Sensor Nodes," in *Efficient Sensor Interfaces, Advanced Amplifiers and Low Power RF Systems: Advances in Analog Circuit Design 2015*, K. A. A. Makinwa, A. Baschirotto, and P. Harpe, Eds. Springer International Publishing, 2016
4. Shidhartha Das, David Roberts, David Blaauw, David Bull, Trevor Mudge, "Architectural Techniques for Adaptive Computing", Chapter in *Adaptive Techniques for Dynamic Processor Optimization: Theory and Practice*, Alice Wang and Sam Naffziger, editors, Springer Publishing Company, 2008
5. David Blaauw, Sanjay Pant, Rajat Chaudhry and Rajendran Panda, "Design and Analysis of Power Supply Networks," Chapter in *Electronic Design Automation for Integrated Circuits Handbook*, Louise Sheffer, Luciano Lavagno and Grant Martin, editors, CRC Press, 2005
6. Sarvesh Kulkarni, Ashish Srivastava, Dennis Sylvester, David Blaauw, "Power Optimization Techniques using Multiple Supply Voltages," Chapter in *Closing the Power Gap between ASIC and Custom*, David Chinnery and Kurt Keutzer, editors, Kluwer Academic Publishers, 2005
7. Dongwoo Lee, Bo Zhai, David Blaauw, Dennis Sylvester, "Static Leakage Reduction through Simultaneous V_t/T_{ox} and State Assignment," Chapter in *Ultra Low-Power Electronics and Design*, Enrico Macii, editor, Kluwer Academic Publishers, 2004
8. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, "Design and Analysis of Power Distribution Networks for Processor Design," Chapter in IEEE *Design of High Performance Microprocessors Circuits*, Anantha Chandrakasan, William Bowhill, and Frank Fox, editors, IEEE Press, 2000
9. Abhijit Dharchoudhury, Shantanu Ganguly, David Blaauw, "Timing and Signal Integrity Analysis," Chapter in *Handbook for VLSI Design*, Wai Kai Chen, editor, IEEE Press, 2000

C. Invited Articles

1. Li Xu, David Blaauw, Dennis Sylvester, "Ultra-Low Power 32kHz Crystal Oscillators: Fundamentals and Design Techniques," *Open Journal of the Solid-State Circuits Society*, Vol. 1, September 2021, pgs. 79-93

2. Li Xu, Jeongsup Lee, Mehdi Saligane, David Blaauw, Dennis Sylvester, "Design Techniques of Integrated Power Management Circuits for Low Power Edge Devices," IEEE Custom Integrated Circuits Conference (CICC), April 2021
3. Sechang Oh, Minchang Cho, Xiao Wu, Yejoong Kim, Li-Xuan Chuo, Wootaek Lim, Pat Pannuto, Suyoung Bang, Kaiyuan Yang, Hun-Seok Kim, Dennis Sylvester, David Blaauw, "IoT2 — the Internet of Tiny Things: Realizing mm-Scale Sensors through 3D Die Stacking," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2019, pgs. 686-691
4. David Blaauw, "Unlocking New IoT Application Domains Through Ultra-Low Power mm-Scale Sensor Node Design," Keynote Address at ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2018
5. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyoong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor Nodes with illustration in a miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 64, No. 9, September 2017, pgs. 2237-2249
6. Taekwang Jang, Gyouho Kim, Benjamin Kempke, Michael Henry, Nikolaos Chiotellis, Carl Pfeiffer, Dongkwun Kim, Yejoong Kim, Zhiyoong Foo, Hyeongseok Kim, Anthony Grbic, Dennis Sylvester, Hun-Seok Kim, David Wentzloff, David Blaauw, "Circuit and System Designs of Ultra-low Power Sensor nodes with Illustration in a Miniaturized GNSS Logger for Position Tracking: Part II—Data Communication, Energy Harvesting, Power Management and Digital Circuits," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 64, No. 9, September 2017, pgs. 2250-2262
7. Wanyeong Jung, Dennis Sylvester, David Blaauw, "Low-Power Switched-Capacitor Converter Techniques for Small IoT Systems," European Conference on Circuit Theory and Design (ECCTD), September 2017
8. Taekwang Jang, Myungjoon Choi, Yao Shi, Inhee Lee, Dennis Sylvester and David Blaauw, "Millimeter-Scale Computing Platform for Next Generation of Internet of Things," IEEE International Conference on RFID (RFID), May 2016
9. Taekwang Jang, Seokhyeon Jeong, Myungjoon Choi, Wanyeong Jung, Gyouho Kim, Yen-Po Chen, Yejoong Kim, Wootaek Lim, Dennis Sylvester, David Blaauw, "Key Building Blocks and Integration Strategy of a Miniaturized Wireless Sensor Node," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2015
10. Nathaniel Pinckney, David Blaauw, Dennis Sylvester, "Low Power Near-Threshold Design," IEEE Solid-State Circuits Magazine, June 2015
11. Inhee Lee, Yejoong Kim, Suyoung Bang, Gyouho Kim, Hyunsoo Ha, Yen-Po Chen, Dongsuk Jeon, Seokhyun Jeong, Wanyeong Jung, Mohammad Hassan Ghaed, Zhiyoong Foo, Yoonmyung Lee, Jae-Yoon Sim, Dennis Sylvester, and David Blaauw, "Circuit Techniques for Miniaturized Biomedical Sensors," IEEE Custom Integrated Circuits Conference (CICC), September 2014
12. David Blaauw, Dennis Sylvester, Prabal Dutta, Yoonmyung Lee, Inhee Lee, Sechang Bang, Yejoong Kim, Gyouho Kim, Pat Pannuto, Ye-Shang Kuo, Dongmin Yoon, Wanyeong Jung, ZhiYoong Foo, Yen-Po Chen, Seok Hyeon Jeong, Myungjoon Choi, "IoT Design Space Challenges: Circuits and Systems" 2014 IEEE Symposium on VLSI Technology, June 2014
13. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Circuits for Ultra-Low Power Millimeter-Scale Sensor Nodes," 2012 Asilomar Conference on Signals, Systems and Computers (Asilomar), November 2012

14. David Blaauw, Dennis Sylvester, Yoonmyung Lee, Inhee Lee, Suyoung Bang, Yejoong Kim, Gyouho Kim, Hassan Ghaed, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," **Invited paper** to the IEEE Subthreshold Microelectronics Conference (SubVt), Plenary Keynote, October 2012
15. Nathaniel Pinckney, Korey Sewell, Ronald Dreslinski, Dave Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Assessing the Performance of Parallelized Near-Threshold Computing," ACM/IEEE Design Automation Conference (DAC), June 2012
16. Yoonmyung Lee, YeJoong Kim, Dongmin Yoon, David Blaauw, Dennis Sylvester, "Circuit and System Design Guidelines for Ultra-Low Power Sensor Nodes," ACM/IEEE Design Automation conference (DAC), June 2012
17. Yoonmyung Lee, Dennis Sylvester, David Blaauw, "Synchronization of Ultra-Low Power Wireless Sensor Nodes", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2011
18. Gregory Chen, Scott Hanson, David Blaauw, Dennis Sylvester, "Circuit Design Advances for Wireless Sensing Applications," Proceedings of the IEEE, Special Issue on Wireless Sensor Networks, Vol. 98, No. 11, November 2010, pg. 1808 - 1827
19. Prashant Singh, Dennis Sylvester, David Blaauw, "Adaptive Sensing and Design for Reliability," IEEE International Reliability Physics Symposium, May 2010
20. Ronald G. Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvester, Trevor Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology, Vol. 98, No. 2, February 2010, pg. 253 - 266
21. Prashant Singh, Cheng Zhuo, Eric Karl, David Blaauw, Dennis Sylvester, "Sensor Driven Reliability and Wearout Management," *IEEE Design & Test of Computers* (*D&T*), Vol. 26, No. 6, November/December 2009, pg. 40 - 49
22. David Blaauw, Shidhartha Das, "CPU, Heal Thyself," IEEE Spectrum, August 2009
23. Shidhartha Das, David Blaauw, David Bull, Krisztian Flautner, Rob Aitken, "Addressing Design Margins through Error-tolerant Circuits," ACM/IEEE Design Automation Conference (DAC), July 2009
24. Shidhartha Das, David Blaauw, "Adaptive Design for Nanometer Technology," IEEE International Symposium on Circuits and Systems (ISCAS), May 2009
25. Dennis Sylvester, Scott Hanson, Seok, Yu-Shiang Lin, David Blaauw, "Designing Robust Ultra-Low Power Circuits," International Electron Devices Meeting (IEDM), December 2008
26. David Blaauw, Kaviraj Chopra, Ashish Srivastava, Lou Sheffer, "Statistical Timing Analysis: Basic Principles to State-of-the-Art," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), invited review article, Vol. 27, No. 4, April 2008, pg. 589-607
27. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, "Energy-Optimal Circuit Design," IEEE International SoC Design Conference, November 2007
28. Sanjay Pant, Eli Chiprout, David Blaauw, "Power Grid Physics and Implications for CAD," *IEEE Design & Test of Computers (D & T)*, Vol. 24, No. 3, May-June 2007, pg. 246-254
29. Dennis Sylvester, Scott Hanson, Bo Zhai, and David Blaauw, "Design strategies for ultra-low voltage circuits," IEEE International SoC Design Conference, September 2006

30. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, Andres Bryant, Xinlin Wang, "Energy Optimality and Variability in Subthreshold Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
31. Shidartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, "A Self-Tuning Dynamic Voltage Scaled Processor Using Delay-Error Detection and Correction," IEEE International Conference on Integrated Circuit Design & Technology (ICICDT), May 2006
32. David Blaauw and Bo Zhai, "Energy Efficient Design for Subthreshold Supply Voltage Operation," IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
33. Rajeev R. Rao, David Blaauw, Dennis Sylvester, Anirudh Devgan, "Modeling and Analysis of Parametric Yield Under Power and Performance Constraints," *IEEE Design & Test of Computers (D&T),* Vol. 22, No. 4, July-August 2005, pg. 376-385
34. Todd Austin, Valeria Bertacco, David Blaauw, Trevor Mudge, "Opportunities and Challenges for Better Than Worst-Case Design," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg. I-2
35. Bo Zhai, David Blaauw, Dennis Sylvester, Krisztián Flautner, "Extended Dynamic Voltage Scaling for Low Power Design," IEEE International SOC Conference, September 2004, pg. 389-394
36. Todd Austin, David Blaauw, Trevor Mudge, Krisztián Flautner, "Making Typical Silicon Matter with Razor" *IEEE Computer,* March 2004, pg. 57-65
37. David Blaauw, Kaushik Gala, "Inductance: Implications and Solutions for High-Speed Digital Circuits - Inductance Extraction and Modeling," IEEE International Solid-State Circuits Conference (ISSCC), February 2002, pg. 548-553
38. David Blaauw, "Signal Integrity Issues in High Performance Design," IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
39. Kaushik Gala, David Blaauw, Junfeng Wang, Vladimir Zolotov, Min Zhao, "Inductance 101: Analysis and Design Issues," ACM/IEEE Design Automation Conference (DAC), June 2001, pg. 329-334
40. David Blaauw, Kaushik Gala, Vladimir Zolotov, Rajendran Panda, Junfeng Wang, "On-Chip Inductance Modeling," ACM/IEEE Great Lake Symposium on VLSI Design (GLSVLSI), March 2000, pg. 75-80
41. David Blaauw, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
42. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, Supamas Sirichotiyakul, Chanhee Oh, Tim Edwards, "Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 1998, pg. 143-148
43. Abhijit Dharchoudhury, Rajendran Panda, David Blaauw, Ravi Vaidyanathan, Bogdan Tutuianu, David Bearden, "Methodology for the Design and Analysis of Power Distribution Networks on the PowerPC Microprocessor," ACM/IEEE Design Automation Conference (DAC), June 1998, pg. 738-743

D. Journals

1. Qirui Zhang, Zichen Fan, Hyochan An, Zhehong Wang, Ziyun Li, Guanru Wang, Pierre Abillama, Hun-Seok Kim, David Blaauw and Dennis Sylvester, "RoboVisio: A Micro-Robot Vision Domain-

Specific SoC for Autonomous Navigation Enabling Fully-on-Chip Intelligence via 2MB eMRAM," *IEEE Journal of Solid-State Circuits (JSSC),* accepted

2. Heejin Yang, Ji-Hwan Seol, Rohit Rothe, Zichen Fan, Qirui Zhang, Hun-Seok Kim, David Blaauw, Dennis Sylvester, "A 1.5μW Fully-Integrated Keyword Spotting SoC in 28nm CMOS with Skip-RNN and Fast-Settling Analog Frontend for Adaptive Frame Skipping," *IEEE Journal of Solid-State Circuits (JSSC),* accepted
3. Chien-Wei Tseng, Zhen Feng, Zichen Fan, Hyochan An, Yunfan Wang, Hun-Seok Kim, David Blaauw, "A Low-Power Highly Reconfigurable Analog FIR Filter With 11-bit Charge-domain DAC for Narrowband Receivers," *IEEE Journal of Solid-State Circuits (JSSC),* **Invited Paper** to the *Special Issue on VLSI 2023*, February 2024
4. Yimai Peng, Seokhyeon Jeong, Kyojin Choo, Yejoong Kim, Li-Yu Chen, Rohit Rothe, Li Xu, Ilya Gurin, Omid Oliaei, Matthew J Thompson, Stephen Bart, Peter Hartwell, David Blaauw, Dennis Sylvester, "An Ultra-Low-Power Triaxial MEMS Accelerometer with High-Voltage Biasing and Electrostatic Mismatch Compensation," *IEEE Journal of Solid-State Circuits (JSSC),* January 2024, pgs. 1-17
5. Jungho Lee, Joseph G. Letner, Jongyup Lim, Gabriele Atzeni, Jiawei Liao, Abhilasha Kamboj, Bhavika Mani, Seokhyeon Jeong, Yejoong Kim, Yi Sun, Beomseo Koo, Julianna Richie, Elena della Valle, Paras R. Patel, Dennis Sylvester, Hun-Seok Kim, Taekwang Jang, Jamie Phillips, Cynthia A. Chestek, James Weiland, David Blaauw, "A Sub-mm3 Wireless Neural Stimulator IC for Visual Cortical Prosthesis with Optical Power Harvesting and 7.5 kbps Data Telemetry," *IEEE Journal of Solid-State Circuits (JSSC),* **Invited Paper** to the *Special Issue on VLSI 2023*, January 2024, pgs. 1-13
6. Anhang Li, Jeongsup Lee, Prashansa Mukim, Brian D. Hoskins, Pragya Shrestha, David Wentzloff, David Blaauw, Dennis Sylvester, Mehdi Saligane, "A fully integrated, automatically generated DC-DC converter maintaining >75% efficiency from 398 K down to 23 K across wide load ranges in 12 nm FinFET," *IEEE Solid-State Circuits Letters*, Vol. 7, January 2024, pgs. 4-45
7. Qirui Zhang, Hyochan An, Andrea Bejarano-Carbo, Hun-Seok Kim, David Blaauw, Dennis Sylvester, "An Ultra-Low-Power H.264/AVC Intra-Frame Image Compression Accelerator for Intelligent Event-Driven IoT Imaging Systems," *IEEE Solid-State Circuit Letters*, Vol. 7, December 2023, pgs. 30-33
8. Rohit Rothe, Hai Li, Dmitri E. Nikonov, Ian A. Young, Kyojin Choo, David Blaauw, "Energy Efficient Logic and Memory Design with Beyond-CMOS Magneto-Electric Spin-Orbit Technology Toward Ultra Low Supply Voltage," *IEEE Journal of Exploratory Solid-State Computational Devices and Circuits*, December 2023
9. Anish Krishnakumar, Hanguang Yu, Tutu Ajayi, A. Alper Goksoy, Vishrut Pandey, Joshua Mack, Sahil Hassan, Kuan-Yu Chen, Chaitali Chakrabarti, Daniel W. Bliss, Ali Akoglu, Hun-Seok Kim, Ronald G. Dreslinski, David Blaauw, Umit Y. Ogras, "FALCON: An FPGA Emulation Platform for Domain-Specific Systems-on-Chip (DSSoCs)," *IEEE Design & Test*, Vol. 41, No. 1, June 2023, pgs. 70-80
10. Donguk Seo, Minsik Cho, Minhyeok Jeong, Gicheol Shin, Inhee Lee, David Blaauw, Yoonmyung Lee, "An RC Delay-Based Pressure-Sensing System with Energy-Efficient Bit-Level Oversampling Techniques for Implantable IOP Monitoring Systems," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 58, No. 10, October 2023, pgs. 2745-2756
11. Harisankar Sadasivan, Jack Wadden, Kush Goliya, Piyush Ranjan, Robert P. Dickson, David Blaauw, Reetuparna Das, Satish Narayanasamy, "Rapid Real-time Squiggle Classification for Read

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12. Leul Belayneh, Haojie Ye, Kuan-Yu Chen, David Blaauw, Trevor Mudge, Ronald Dreslinski, Nishil Talati, "Locality-aware Optimizations for Improving Remote Memory Latency in Multi-GPU Systems," *31st International Conference on Parallel Architectures and Compilation Techniques (PACT)*, January 2023, pgs. 304–316
13. Yimai Peng, Gordy Carichner, Yejoong Kim, Li-Yu Chen, Rémy Tribhout, Benoît Piranda, Julien Bourgeois, Member, David Blaauw, Dennis Sylvester, "A High-Voltage Generator and Multiplexer for Electrostatic Actuation in Programmable Matter," *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2022*, Vol. 58, No. 4, April 2023, pgs. 915-928
14. Jongyup Lim, Jungho Lee, Eunseong Moon, Michael Barrow, Gabriele Atzeni, Joseph G. Letner, Joseph T. Costello, Samuel R. Nason, Paras R. Patel, Yi Sun, Parag G. Patil, Hun-Seok Kim, Cynthia A. Chestek, Jamie Phillips, David Blaauw, Dennis Sylvester, Taekwang Jang, "A Light Tolerant Wireless Neural Recording IC for Motor Prediction with Near-Infrared-based Power and Data telemetry," *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, Vol. 57., No. 4, January 2022, pgs. 1061-1074
15. Sujin Park, Ji-Hwan Seol, Li Xu, SeongHwan Cho, Dennis Sylvester, David Blaauw, "A 43nW, 32kHz, ±4.2ppm Piece-Wise Linear Temperature Compensated Crystal Oscillator with ΔΣ Modulated Load Capacitance," *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, Vol. 57, Vol. 4, January 2022, pgs. 1175 - 1186
16. Sung Kim, Morteza Fayazi, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor Mudge, Chaitali Chakrabarti, David Blaauw, Ronald Dreslinski, Hun-Seok Kim, "Versa: A 36-Core Systolic Multiprocessor with Dynamically-Reconfigurable Interconnect and Memory," *IEEE Journal of Solid-state Circuits (JSSC)*, **Invited Paper** to the *Special Issue on VLSI 2021*, Vol. 57, No. 4, January 2022, pgs. 986-998
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18. Jack Wadden, Brandon Newell, Joshua Bugbee, Vishal John, Amy K. Bruzek, Robert P. Dickson, Carl Koschmann, David Blaauw, Satish Narayanasamy, Reetuparna Das, "Ultra-Rapid Somatic Variant Detection via Real-Time Targeted Amplicon Sequencing," *Communications Biology*, July 2022
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20. Qirui Zhang, Wenbo Duan, Tim Edwards, Tim Ansell, David Blaauw, Dennis Sylvester, Mehdi Saligane, "An Open-Source and Autonomous Temperature Sensor Generator Verified with 64 Instances in SkyWater 130nm for Comprehensive Design Space Exploration," in IEEE Solid-State Circuits Letters, Vol. 5, July 2022, pgs. 174-177
21. Ji-Hwan Seol, Kyojin Choo, David Blaauw, Dennis Sylvester, Taekwang Jang, "A Reference Oversampling PLL achieving −256-dB FoM and −78-dBc Reference Spur," *IEEE Journal of Solid-State*

Circuits (JSSC), **Invited Paper** to the *Special Issue on ASSCC 2020,* Vol. 56, No. 10, October 2021, pgs. 2993-3007

22. Li Xu, Kyojin Choo, David Blaauw, Dennis Sylvester, "An Analog-Assisted Digital LDO with Single Subthreshold Output PMOS Achieving 1.44fs FOM," *IEEE Solid-State Circuits Letters*, August 2021, pgs. 154-157
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E. Conference Papers

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2. Pierre Abillama, Zichen Fan, Yu Chen, Hyochan An, Qirui Zhang, Seungkyu Choi, David Blaauw, Dennis Sylvester, Hun-Seok Kim, "SONA: An Accelerator for Transform-Domain Neural Networks with Sparse-Orthogonal Weights," 34th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP), July 2023, **Best Paper Award**
3. Zichen Fan, Qirui Zhang, Pierre Abillama, Sara Shoouri, Changwoo Lee, David Blaauw, Hun-Seok Kim, Dennis Sylvester, "TaskFusion: An Efficient Transfer Learning Architecture with Dual Delta Sparsity for Multi-Task Natural Language Processing," IEEE International Symposium on Computer Architecture (ISCA), June 2023
4. Jungho Lee, Joseph Letner, Jongyup Lim, Yi Sun, Seokhyeon Jeong, Yejoong Kim, Beomseo Koo, Gabriele Atzeni, Jiawei Liao, Julianna Richie, Elena della Valle, Paras Patel, Taekwang Jang, Cynthia Chestek, Jamie Phillips, James Weiland, Dennis Sylvester, Hun-Seok Kim, David Blaauw,

"A Wireless Neural Stimulator IC for Cortical Visual Prosthesis," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), **Invited Paper** to the IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI, June 2023

5. Chien-Wei Tseng, Zhen Feng, Zichen Fan, Hyochan An, Yunfan Wang, Hun-Seok Kim, David Blaauw, "A Low Power Highly Reconfigurable Analog FIR Filter With 11-bit Charge-domain DAC for Narrowband Receivers," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), **Invited Paper** to The IEEE Solid-State Circuit Letters (SSCL), Special Section on VLSI, June 2023
6. Yufeng Gu, Arun Subramaniyan, Tim Dunn, Alireza Khadem, Kuan-Yu Chen, Somnath Paul, Md Vasimuddin, Sanchit Misra, David Blaauw, Satish Narayanasamy, Reetuparna Das, "GenDP: A Framework of Dynamic Programming Acceleration for Genome Sequencing Analysis," IEEE International Symposium on Computer Architecture (ISCA), June 2023
7. Hyochan An, Yu Chen, Zichen Fan, Qirui Zhang, Pierre Abillama, Hun-Seok Kim, David Blaauw, Dennis Sylvester, "A 8.09TOPS/W Neural Engine Leveraging Bit-Sparsified Sign-Magnitude Multiplications and Dual Adder Trees," IEEE International Solid-State Circuits Conference (ISSCC), February 2023
8. Ji-Hwan Seol, Heejin Yang, Rohit Rothe, Zichen Fan, Qirui Zhang, Hun-Seok Kim, David Blaauw, Dennis Sylvester, "A 1.5μW End-to-End Keyword Spotting SoC with Content-Adaptive Frame Sub-Sampling and Fast-Settling Analog Frontend," IEEE International Solid-State Circuits Conference (ISSCC), February 2023
9. Leul Belayneh, Haojie Ye, Kuan-Yu Chen, David Blaauw, Trevor Mudge, Ronald Dreslinski, Nishil Talati, "Locality-aware Optimizations for Improving Remote Memory Latency in Multi-GPU Systems," 31st International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2022
10. Xin He, Kuan-Yu Chen, Siying Feng, Hun-Seok Kim, David Blaauw, Ronald Dreslinski, Trevor Mudge, "Squaring the circle: Executing Sparse Matrix Computations on FlexTPU—a TPU-like processor," 31st International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2022
11. Nishil Talati, Haojie Ye, Sanketh Vedula, Kuan-Yu Chen, Yuhan Chen, Daniel Liu, Yichao Yuan, David Blaauw, Alex Bronstein, Trevor Mudge, and Ronald Dreslinski "Mint: An Accelerator For Mining Temporal Motifs," ACM/IEEE International Symposium on Microarchitecture (MICRO), October 2022
12. Yufan Yue, Tutu Ajayi, Xueyang Liu, Peiwen Xing, Zihan Wang, David Blaauw, Ron Dreslinski, Hun-Seok Kim, "A Unified Forward Error Correction Accelerator for Multi-Mode Turbo, LDPC, and Polar Decoding," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2022
13. Yichen Gu, David Blaauw, Joshua Welch, "Variational Mixtures of ODEs for Inferring Cellular Gene Expression Dynamics," Thirty-ninth International Conference on Machine Learning (ICML), July 2022
14. Gabriele Atzeni, Jongyup Lim, Jiawei Liao, Alessandro Novello, Jungho Lee, Eunseong Moon, Michael Barrow, Joseph Letner, Joseph Costello, Samuel R. Nason, Paras R. Patel, Parag G. Patil, Hun-Seok Kim, Cynthia A. Chestek, Jamie Phillips, David Blaauw, Taekwang Jang, "C07-3 - A 260×274 μm2 572 nW Neural Recording Micromote Using Near-Infrared Power Transfer and an RF Data Uplink," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2022
15. Kuan-Yu Chen, Chi-Sheng Yang, Yu-Hsiu Sun, Chien-Wei Tseng, Morteza Fayazi, Xin He, Siying Feng, Yufan Yue, Trevor Mudge, Ronald Dreslinski, Hun-Seok Kim, David Blaauw, "A 507 GMACs/J 256-Core Domain Adaptive Systolic-Array-Processor for Wireless Communication and

Linear-Algebra Kernels in 12nm FINFET," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2022

16. Qirui Zhang, Hyochan An, Zichen Fan, Zhehong Wang, Ziyun Li, Guanru Wang, Hun-Seok Kim, David Blaauw and Dennis Sylvester, "A 22nm 3.5TOPS/W Flexible Micro-Robotic Vision SoC with 2MB eMRAM for Fully-on-Chip Intelligence," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2022
17. Yimai Peng, Gordy Carichner, Yejoong Kim, Li-Yu Chen, Rémy Tribhout, Benoît Piranda, Julien Bourgeois, David Blaauw, Dennis Sylvester, "A 286nW, 103V High Voltage Generator and Multiplexer for Electrostatic Actuation in Programmable Matter," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI*, June 2022
18. Yimai Peng, Seokhyeon Jeong, Kyojin Choo, Yejoong Kim, Li-Yu Chen, Rohit Rothe, Li Xu, Ilya Gurin, Omid Oliaei, Vadim Tsinker, Stephen Bart, Peter Hartwell, David Blaauw, Dennis Sylvester, "A 184nW, 121μg/$\sqrt{}$Hz Noise Floor Triaxial MEMS Accelerometer with Integrated CMOS Readout Circuit and Variation-Compensated High Voltage MEMS Biasing," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Solid-State Circuit Letters (SSCL), Special Issue on VLSI*, June 2022
19. Zichen Fan, Hyochan An, Qirui Zhang, Boxun Xu, Li Xu, Chien-wei Tseng, Yimai Peng, Ang Cao, Bowen Liu, Changwoo Lee, Zhehong Wang, Fanghao Liu, Guanru Wang, Shenghao Jiang, Hun-Seok Kim, David Blaauw, Dennis Sylvester, "Audio and Image Cross-Modal Intelligence via a 10TOPS/W 22nm SoC with Back-Propagation and Dynamic Power Gating," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2022
20. Daniel W. Bliss, Tutu Ajayi, Ali Akoglu, I. Aliyev, David Blaauw, Leul Belayneh, John Brunhaver, Chaitali Chakrabarti, L. Chang, Kuan-Yu Chen, M.-H. Chen, X. Chen, A. R. Chiriyath, A. Daftardar, Ronald Dreslinski, A. Dutta, Y. Fu, A. Goksoy, X. He, Md. S. Hassan, A. Herschfelt, J. Holtom, Hun Seok Kim, A. N. Krishnakumar, Y. Li, O. Ma1,, J. Mack, S. Mallik, S. K. Mandal, R. Marculescu, B. McCall, Trevor Mudge, U. Y. Ogras, V. Pandey, S. Siddiqui, Y.-H. Sun, A. Venkataramani, Xiangdong Wei, , B. R. Willis, H. Yu, Yufan Yue, "Enabling Software-Defined RF Convergence with a Novel Coarse-Scale Heterogeneous Processor," IEEE International Symposium on Circuits and Systems (ISCAS), May 2022
21. Siying Feng, Xin He, Kuan-Yu Chen, Liu Ke, Xuan Zhang, David Blaauw, Trevor Mudge, Ronald Dreslinski, "MeNDA: A Near-Memory Multi-way Merge Solution for Sparse Transposition and Dataflows," IEEE International Symposium on Computer Architecture (ISCA), June 2022
22. Nishil Talati, Haojie Ye, Yichen Yang, Leul Belayneh, Kuan-Yu Chen, David Blaauw, Trevor Mudge, Ronald Dreslinski, "NDMiner: Accelerating Graph Pattern Mining Using Near Data Processing," IEEE International Symposium on Computer Architecture (ISCA), June 2022
23. Andrea Bejarano-Carbo, Hyochan An, Kyojin Choo, Shiyu Liu, Dennis Sylvester, David Blaauw, Hun Seok Kim, "Millimeter-Scale Ultra-Low-Power Imaging System for Intelligent Edge Monitoring," TinyML conference, March 2022, **Best Paper Award**
24. Li Xu, Maya Lassiter, Xiao Wu, Yejoong Kim, Jungho Lee, Makoto Yasuda, Masaru Kawaminami, Marc Miskin, David Blaauw, Dennis Sylvester "A 210 × 340 × 50μm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2022
25. Chien-Wei Tseng, Demba Komma, Kuan-Yu Chen, Rohit Rothe, Zhen Feng, Makoto Yasuda, Masaru Kawaminami, Hun-Seok Kim, David Blaauw, "A Long-Range Narrowband RF Localization System with a Crystal-Less Frequency-Hopping Receiver," IEEE International Solid-State Circuits Conference (ISSCC), February 2022

26. Tim Dunn, Hari Sadasivan, Jack Wadden, Kush Goliya, Kuan-Yu Chen, David Blaauw, Reetuparna Das, Satish Narayanasamy, "SquiggleFilter: An Accelerator for Portable Virus Detection," IEEE International Symposium on Microarchitecture (MICRO-54), **Invited Paper** to *Special Top Picks* from the 2021 Computer Architecture Conferences, Honorable Mention, October 2021
27. Rohit Rothe, Minchang Cho, Kyojin Choo, Seokhyeon Jeong, Dennis Sylvester, David Blaauw, "A 192 nW 0.02 Hz High Pass Corner Acoustic Analog Front-End with Automatic Saturation Detection and Recovery," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI*, June 2021
28. Jongyup Lim, Jungho Lee, Eunseong Moon, Michael Barrow, Gabriele Atzeni, Joseph Letner, Joseph Costello, Samuel R. Nason, Paras R. Patel, Parag G. Patil, Hun-Seok Kim, Cynthia A. Chestek, Jamie Phillips, David Blaauw, Dennis Sylvester, Taekwang Jang, "Light Tolerant Neural Recording IC for Near-Infrared-Powered Free Floating Motes," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI*, June 2021
29. Sujin Park, Ji-Hwan Seol, Li Xu, Dennis Sylvester, David Blaauw, "A 43nW 32kHz Pulsed Injection TCXO with ±4.2ppm Accuracy Using DS Modulated Load Capacitance," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2021
30. Sung Kim, Morteza Fayazi, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor Mudge, Chaitali Chakrabarti, David Blaauw, Ronald Dreslinski, Hun-Seok Kim, "Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2021
31. Arun Subramaniyan, Jack Wadden, Kush Goliya, Nathan Ozog, Xiao Wu, Satish Narayanasamy, David Blaauw, Reetuparna Das, "Accelerated Seeding for Genome Sequence Alignment with Enumerated Radix Trees," IEEE International Symposium on Computer Architecture (ISCA), June 2021
32. Arun Subramaniyan, Yufeng Gu, Timothy Dunn, Somnath Paul, Md Vasimuddin, Sanchit Misra, David Blaauw, Satish Narayanasamy, Reetuparna Das, "GenomicsBench: A Benchmark Suite for Genomics," International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2021
33. Kyojin Choo, Hyochan An, Dennis Sylvester, David Blaauw, "14.1-ENOB 184.9dB-FoM Capacitor-Array-Assisted Cascaded Charge-Injection SAR ADC," IEEE International Solid-State Circuits Conference (ISSCC), February 2021
34. Mingyu Yang, Roger Hsiao, Gordy Carichner, Katherine Ernst, Jaechan Lim, Delbert A. Green II, Inhee Lee, David Blaauw, Hun-Seok Kim, "Migrating Monarch Butterfly Localization Using Multi-Modal Sensor Fusion Neural Networks," European Signal Processing Conference (EUSIPCO), January 2021
35. Ji-Hwan Seol, Kyojin Choo, David Blaauw, Dennis Sylvester, Taekwang Jang, "A 67fs_{rms} Jitter, −130dBc/Hz In-Band Phase Noise, −256-dB FoM Reference Oversampling Digital PLL With Proportional Path Timing Control," IEEE Asian Solid-State Circuits Conference (A-SSCC), **Invited Paper** to the *IEEE Solid-State Circuits Letters, Special Issue on ASSCC 2020*, November 2020
36. Jeongsup Lee, Yejoong Kim, Minchang Cho, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, David Blaauw, Dennis Sylvester, "A µProcessor Layer for mm-Scale Die-Stacked Sensing Platforms Featuring Ultra-Low Power Sleep Mode at 125˚C," IEEE Asian Solid-State Circuits Conference (A-SSCC), November 2020

37. Daichi Fujiki, Shunhao Wu, Nathan Ozog, Kush Goliya, David Blaauw, Satish Narayanasamy, Reetuparna Das, "SeedEx: A Genome Sequencing Accelerator for Optimal Alignments in Subminimal Space," ACM/IEEE International Symposium on Microarchitecture (MICRO), October 2020

38. Subhankar Pal, Siying Feng, Dong-hyeon Park, Sung Kim, Aporva Amarnath, Chi-Sheng Yang, Xin He, Jonathan Beaumont, Kyle May, Yan Xiong, Kuba Kaszyk, John Magnus Morton, Jiawen Sun, Michael O'Boyle, Murray Cole, Chaitali Chakrabarti, David Blaauw, Hun-Seok Kim, Trevor Mudge, Ronald Dreslinski, "Transmuter: Bridging the Efficiency Gap using Memory and Dataflow Reconfiguration," 29th International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2020

39. Yan Xiong, J. Zhou, Subhankar Pal, David Blaauw Blaauw, Hun-Seok Kim, Trevor Mudge, Ronald Dreslinski, C Chaitali Chakrabarti, "Accelerating Deep Neural Network Computation on a Low Power Reconfigurable Architecture," IEEE International Symposium on Circuits and Systems (ISCAS), October 2020

40. Jongyup Lim, Myungjoon Choi, Bowen Liu, Taewook Kang, Ziyun Li, Zhehong Wang, Yiqun Zhang, Kaiyuan Yang, David Blaauw, Hun-Seok Kim, Dennis Sylvester, "AA-ResNet: Energy Efficient All-Analog ResNet Accelerator," Midwest Symposium and Circuits and Systems (MWSCAS), August 2020

41. Zhen Feng, Li-Xuan Chuo, Yao Shi, Yejoong Kim, HunSeok Kim, David Blaauw, "A mm-Scale Sensor Node with a 2.7 GHz 1.3 μW Trasceiver using Full-Duplex Self-Coherent Backscattering Achieving 3.5 m Range," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2020

42. Hyochan An, Siddharth Venkatesan, Sam Schiferl, Tim Wesley, Qirui Zhang, Jingcheng Wang, Kyojin Choo, Shiyu Liu, Bowen Liu, Ziyun Li, Hengfei Zhong, Luyao Gong, David Blaauw, Ronald Dreslinski, Dennis Sylvester, Hun Seok Kim, "A 170μW Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI,* June 2020

43. Jingcheng Wang, Hyochan An, Qirui Zhang, Hun Seok Kim, David Blaauw, Dennis Sylvester, "1.03pW/b Ultra-low Leakage Voltage-Stacked SRAM for Intelligent Edge Processors," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits letters, Special Issue on VLSI,* June 2020

44. Rohit Rothe, Sechang Oh, Kyojin Choo, Seokhyeon Jeong, Minchang Cho, Dennis Sylvester, David Blaauw, "Sample and Average Common-Mode Feedback in a 101 nW Acoustic Amplifier," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2020

45. Seokhyeon Jeong, Yejoong Kim, Gyouho Kim, David Blaauw, "A Pressure Sensing System with ±0.75 mmHg (3σ) Inaccuracy for Battery-Powered Low Power IoT applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2020

46. Xiao Wu, Arun Subramaniyan, Zhehong Wang, Satish Narayanasamy, Reetu Das, David Blaauw, "17.3 GCUPS Pruning-based Pair-Hidden-Markov-Model Accelerator for Next-Generation DNA Sequencing," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Solid-State Circuits Letters, Special Issue on VLSI,* June 2020

47. Zhehong Wang, Ziyun Li, Li Xu, Qing Dong, Chin-I Su, Wen-Ting Chu, George Tsou, Yu-Der Chih, Tsung-Yung Jonathan Chang, Dennis Sylvester, Hun Seok Kim, David Blaauw, "An All-Weights-on-Chip DNN Accelerator in 22nm ULL Featuring 24×1 Mb eRRAM," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI,* June 2020

48. Anuraag Soorishetty, Jian Zhou, Subhankar Pal, David Blaauw, Hun Seok Kim, Trevor Mudge, Ronald Dreslinski, Chaitali Chakrabarti, "Accelerating Linear Algebra Kernels on a Massively Parallel Reconfigurable Architecture," IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), May 2020
49. Zhehong Wang, Tianjun Zhang, Daichi Fujiki, Arun Subramaniyan, Xiao Wu, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, Reetuparna Das, Satish Narayanasamy, David Blaauw, "A 2.46M reads/s Genome Sequencing Accelerator using a 625 Processing-Element Array," IEEE Custom Integrated Circuits Conference (CICC), March 2020
50. Jongyup Lim, Eunseong Moon, Michael Barrow, Samuel R. Nason, Paras R. Patel, Parag G. Patil, Sechang Oh, Inhee Lee, Hun-Seok Kim, Dennis Sylvester, David Blaauw, Cynthia A. Chestek, Jamie Phillips, Taekwang Jang, "A 0.19×0.17mm2 Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry," IEEE International Solid-State Circuits Conference (ISSCC), February 2020
51. Li Xu, Taekwang Jang, Jongyup Lim, Kyojin Choo, David Blaauw, Dennis Sylvester, "A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection," IEEE International Solid-State Circuits Conference (ISSCC), February 2020
52. Charles Eckert, Xiaowei Wang, Jingcheng Wang, Arun Subramaniyan, Ravi Iyer, Dennis Sylvester, David Blaauw, Reetuparna Das, "*Neural Cache*: Bit-Serial In-Cache Acceleration of Deep Neural Networks," ACM/IEEE International Symposium on Microarchitecture (MICRO), June 2019
53. Li-Xuan Chuo, Yejoong Kim, Nikolaos Chiotellis, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, Anthony Grbic, David Wentzloff, Hun-Seok Kim, David Blaauw, "A 4×4×4-mm3 Fully Integrated Sensor-to-Sensor Radio using Carrier Frequency Interlocking IF Receiver with -94 dBm Sensitivity," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on RFIC*, June 2019, **Best Paper Award**
54. Najme Ebrahimi, Behzad Yektakhah, Kamal Sarabandi, Hun Seok Kim, David Wentzloff, David Blaauw, "A Novel Physical Layer Security Technique Using Master-Slave Full Duplex Communication," IEEE MTT-S International Microwave Symposium (IMS), June 2019
55. Inhee Lee, David Blaauw, "A 31 pW-to-113 nW Hybrid BJT and CMOS Voltage Reference with 3.6% ±3σ-inaccuracy from 0 oC to 170 oC for Low-Power High-Temperature IoT Systems," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2019
56. Inhee Lee, Eunseong Moon, Yejoong Kim, Jamie Phillips, David Blaauw, "A 10mm3 Light-Dose Sensing IoT2 System with 35-to-339nW 10-to-300klx Light-Dose-to-Digital Converter," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2019
57. Taewook Kang, Inhee Lee, Sechang Oh, Taekwang Jang, Yejoong Kim, Hyochan Ahn, Gyouho Kim, Se-Un Shin, Seokhyeon Jeong, Dennis Sylvester, David Blaauw, "A 1.7×4.1×2 mm3 Fully Integrated pH Sensor for Implantable Applications using Differential Sensing and Drift-Compensation," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2019
58. Subhankar Pal, Dong-hyeon Park, Siying Feng, Paul Gao, Jielun Tan, Austin Rovinski, Shaolin Xie, Chun Zhao, Aporva Amarnath, Timothy Wesley, Jonathan Beaumont, Kuan-Yu Chen, Chaitali Chakrabarti, Michael Taylor, Trevor Mudge, David Blaauw, Hun-Seok Kim, Ronald Dreslinski, "A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator using Memory Reconfiguration in 40 nm," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI*, June 2019
59. Ji-Hwan Seol, Dennis Sylvester, David Blaauw, Taekwang Jang, "A Reference Oversampling Digital Phase-Locked Loop with −240 dB FOM and −80 dBc Reference Spur," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2019

60. Jingcheng Wang, Xiaowei Wang, Charles Eckert, Arun Subramaniyan, Reetuparna Das, David Blaauw, Dennis Sylvester, "A Compute SRAM with Bit-Serial Integer/Floating-Point Operations for Programmable In-Memory Vector Acceleration," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2019

61. Yimai Peng, David Kyojin Choo, Sechang Oh, Inhee Lee, Taekwang Jang, Yejoong Kim, Jongyup Lim, Dennis Sylvester, David Blaauw, "An Adiabatic Sense and Set Rectifier for Improved Maximum Power Point Tracking in Piezoelectric Harvesting with 541% Energy Extraction Gain," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2019

62. Kyojin D. Choo, Li Xu, Yejoong Kim, Ji-Hwan Seol, Xiao Wu, Dennis Sylvester, David Blaauw, "Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2019

63. Minchang Cho, Sechang Oh, Zhan Shi, Jongyup Lim, Yejoong Kim, Seokhyeon Jeong, Yu Chen, David Blaauw, Hun-Seok Kim, Dennis Sylvester, "A 142nW Voice and Acoustic Activity Detection Chip for mm-Scale Sensor Nodes Using Time-Interleaved Mixer-Based Frequency Scanning," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2019

64. Jeongsup Lee, Yiqun Zhang, Qing Dong, Wooteak Lim, Mehdi Saligane, Yejoong Kim, Seokhyeon Jeong, Jongyup Lim, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, David Blaauw, Dennis Sylvester, "A 6.4pJ/cycle Self-tuning Cortex-M0 IoT Processor based on Leakage-Ratio Measurement for Energy Optimal Operation across Wide-Range PVT Variation," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2019

65. Yao Shi, Xing Chen, Hun-Seok Kim, David Blaauw, David Wentzloff, "A 606-µW Millimeter-Scale Bluetooth Low Energy Transmitter using Co-Designed 3.5x3.5 mm2 Loop Antenna and Transformer-Boost Power Oscillator," IEEE International Solid-State Circuits Conference (ISSCC), February 2019

66. Ziyun Li, Ziyun Li, Yu Chen, Luyao Gong, Lu Liu, Dennis Sylvester, David Blaauw, Hun-Seok Kim, "An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration," IEEE International Solid-State Circuits Conference (ISSCC), February 2019

67. Mehdi Saligane, Jeongsup Lee, Qing Dong, Makoto Yasuda, Kazuyuki Kumeno, Fumitaka Ohno, Satoru Miyoshi, Masaru Kawaminami, David Blaauw, Dennis Sylvester, "An Adaptive Body-Biasing SoC using in situ Slack Monitoring for Runtime Replica Calibration," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018

68. Jongyup Lim, Taekwang Jang, Mehdi Saligane, Makoto Yasuda, Satoru Miyoshi, Masaru Kawaminami, David Blaauw, Dennis Sylvester, "A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018

69. Taekwang Jang, Jongyup Lim, Kyojin Choo, Samuel Nason, Jeongsup Lee, Sechang Oh, Seokhyeong Jeong, C. Chestek, Dennis Sylvester, David Blaauw, "A 2.2 NEF Neural-Recording Amplifier Using Discrete-Time Parametric Amplification," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018

70. Xiao Wu, Inhee Lee, Qing Dong, Kaiyuan Yang, Dongkwun Kim, Jingcheng Wang, Yimai Peng, Yiqun Zhang, Mehdi Saligane, Makoto Yasuda, Kazuyuki Kumeno, Fumitaka Ohno, Satoru Miyoshi, Masaru Kawaminami, Dennis Sylvester, David Blaauw, "A 0.04mm3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018
71. Inhee Lee, Gyouho Kim, Eunseong Moon, Seokhyeon Jeong, Dongkwun Kim, Jamie Phillips, David Blaauw, "A 179-lux Energy-Autonomous Fully-Encapsulated 17-mm3 Sensor Node with Initial Charge Delay Circuit for Battery Protection," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018
72. Kaiyuan Yang, Qing Dong, Zhehong Wang, Yi-Chun Shih, Yu-Der Chih, Jonathan Chang, David Blaauw, Dennis Sylvester, "A 28nm Integrated True Random Number Generator Harvesting Entropy from MRAM," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018
73. Supreet Jeloka, Zhehong Wang, Ruochen Xie, Sudhanshu Khanna, Steven Bartling, Dennis Sylvester, David Blaauw, "Energy Efficient Adiabatic FRAM with 0.99 pJ/bit Write for IoT Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2018
74. Ziyun Li, Jingcheng Wang, Dennis Sylvester, David Blaauw, Hun-Seok Kim, "A 1920 × 1080 25fps, 2.4TOPS/W Unified Optical Flow and Depth 6D Vision Processor for Energy-Efficient, Low Power Autonomous Navigation," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-StateSolid-States Circuits (JSSC), Special Issue on VLSI*, June 2018
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171. Nathaniel Pinckney, Matthew Fojtik, Bharan Giridhar, Dennis Sylvester, and David Blaauw, "Shortstop: An On-Chip Fast Supply Boosting Technique," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2013
172. Suyong Bang, Yoonmyung Lee, Inhee Lee, Yejoong Kim, Gyouho Kim, DavidBlaauw, Dennis Sylvester, "A Fully Integrated Switched-Capacitor Based PMU with Adaptive Energy Harvesting Technique for Ultra- Low Power Sensing Applications," IEEE International Symposium on Circuits and Systems (ISCAS), May 2013

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174. Nilmini Abeyratne, Reetuparna Das, Qingkun Li, Korey Sewell, Bharan Giridhar, Ronald Dreslinski, David Blaauw, Trevor Mudge, "Scaling Towards Kilo-Core Processors with Asymmetric High Radix Topologies," IEEE International Symposium on High Performance Computer Architecture (HPCA-19), February 2013

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177. Seon-Kyoo Lee, Seung-Hun Lee, Dennis Sylvester, David Blaauw, Jae-Yoon Sim, "A 95fJ/b Current-Mode Transceiver for 10mm On-Chip Interconnect," IEEE International Solid-State Circuits Conference (ISSCC), February 2013

178. Gyouho Kim, Mahmood Barangi, Zhiyoong Foo, Nathaniel Pinckney, Suyoung Bang, David Blaauw, Dennis Sylvester, "A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation," IEEE International Solid-State Circuits Conference (ISSCC), February 2013

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181. Suyoung Bang, David Blaauw, Dennis Sylvester, Massimo Alioto, "Reconfigurable Sleep Transistor for GIDL Reduction in Ultra-Low Standby Power Systems," IEEE Custom Integrated Circuits Conference (CICC), September 2012

182. Zhiyoong Foo, David Devescery, Mohammad Ghaed, Inhee Lee, Abishek Madhavan, Youn Sung Park, Aswin Rao, Zach Renner, Nathan Roberts, Aaron Schulman, Vikas Vinay, Michael Wieckowski, Dongmin Yoon, Cliff Schmidt, Thomas Schmid, Prabal Dutta, Peter Chen, David Blaauw, "A Low-cost Audio Computer for Information Dissemination among Illiterate People Groups," IEEE Custom Integrated Circuits Conference (CICC), September 2012

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187. Daeyeon Kim, Vikas Chandra, Robert Aitken, Dennis Sylvester, David Blaauw, "An Adaptive Write Word-Line Pulse Width and Voltage Modulation Architecture for Bit-Interleaved 8T SRAMS," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2012

188. Sudhir Satpathy, Dennis Sylvester, David Blaauw, "A Standard Cell Compatible Bidirectional Repeater with Thyristor Assist," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012

189. Yen-Po Chen, Matt Fijtik, David Blaauw, Dennis Sylvester, "A 2.98nW Bandgap Voltage Reference Using a Self-Tuning Low Leakage Sample and Hold," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012

190. Youn Sung Park, David Blaauw, Dennis Sylvester, Zhengya Zhano, "A 1.6mm2 38-mW 1.5-Gb/s LDPC Decoder Enabled by Refresh-Free Embedded DRAM," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012

191. Inhee Lee, Suyoung Bang, Yoonmyung Lee, Yejoong Kim, Gyouho Kim, Dennis Sylvester, David Blaauw, "A 635pW Battery Voltage Supervisory Circuit for Miniature Sensor Nodes," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2012

192. Dongsuk Jeon, Mingoo Seok, Zhengya Zhang, David Blaauw, Dennis Sylvester, "A design methodology for voltage overscaled ultra-low power systems," ACM/IEEE Design Automation Conference (DAC), June 2012

193. Sudhir Satpathy, Reetuparna Das, Ronald Dreslinski, Trevor Mudge, Dennis Sylvester, David Blaauw, "High radix self-arbitrating switch fabric with multiple arbitration schemes and quality of service," ACM/IEEE Design Automation Conference (DAC), June 2012

194. Sangwon Seo, Ronald Dreslinski, Mark Woh, Yongjun Park, Scott Mahlke, David Blaauw, Chaitali Chakrabarti, Trevor Mudge, "Process Variation in Near-Threshold Wide SIMD Architectures," ACM/IEEE Design Automation Conference (DAC), June 2012

195. Sudhir Satpathy, Korey Sewell, Thomas Manville, Yen-Po Chen, Ronald Dreslinski, Dennis Sylvester, Trevor Mudge, David Blaauw, "A 4.5Tb/s 3.4Tb/sW 64 x 64 Switch Fabric With Self-Updating Least-Recently-Granted Priority and Quality-of-Service Arbitration in 45nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2012

196. Yoonmyung Lee, Gyouho Kim, Suyoung Bang, Yejoong Kim, Inhee Lee, Prababl Dutta, Dennis Sylvester, David Blaauw, "A Modular 1mm^3 Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2012

197. Dongmin Yoon, Dennis Sylvester, David Blaauw, "A 5.58nW 32.768kHz DLL-Assisted XO for Real Time Clocks in Wireless Sensing Applications," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2012

198. Mathew Fojtik, David Fick, Yejoong Kim, Nathaniel Pinckney, David Harris, David Blaauw, Dennis Sylvester, "Bubble Razor: An Architecture-Independent Approach to Timing-Error Detection and Correction," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2012

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200. Mohammad Hassan Ghaed, Gregory Chen, David Blaauw, Dennis Sylvester, "Analysis and Measurement of the Stability of Dual-Resonator Oscillators," IEEE Custom Integrated Circuts Conference (CICC), September 2011

201. Daeyeon Kim, Vikas Chandra, Robert Aitken, David Blaauw, Dennis Sylvester, "Variation-Aware Static and Dynamic Writability Analysis for Voltage-Scaled Bit-Interleaved 8-T SRAMs," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2011

202. Mohammad Hassan Ghaed, Dennis Sylvester, David Blaauw, "A Dual-Passband Filter Architecture for Dual-Band Systems," IEEE Antennas and Propagation Society (AP-S), July 2011

203. Dongsuk Jeon, Mingoo Seok, Chaitali Chakrabarti, David Blaauw, and Dennis Sylvester, "A Super-Pipelined Energy Efficient Subthreshold 240MS/s FFT Core in 65nm," Design Automation Conference (DAC), June 2011

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206. Sudhir Satpathy, Ronald Dreslinski, Tai-Chuan Ou, Dennis Sylvester, Trevor Mudge, David Blaauw, "SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011, **Winner in the 11th Annual International VLSI-Symposium Low Power Design Contest**

207. Nurrachman Liu, Nathaniel Pinckney, Scott Hanson, Dennis Sylvester, David Blaauw, "A True Random Number Generator using Time-Dependent Dielectric Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2011

208. Dongsuk Jeon, Mingoo Seok, Chaitali Chakrabarti, David Blaauw, Dennis Sylvester, "Energy-Optimized High Performance FFT Processor," International Conference on Acoustics, Speech and Signal Processing (ICASSP), May 2011

209. Gregory Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, "A Dense 45nm Half-differential SRAM with Lower Minimum Operating Voltage," IEEE International Symposium on Circuits and Systems (ISCAS), May 2011

210. Daeyeon Kim, Gregory Chen, Matthew Fojtik, Mingoo Seok, David Blaauw, Dennis Sylvester, "A 1.85fW/bit Ultra Low Leakage 10T SRAM with Speed Compensation Scheme," IEEE International Symposium on Circuits and Systems (ISCAS), May 2011

211. Michael Wieckowski, Gregory Chen, Daeyeon Kim, David Blaauw, Dennis Sylvester, "A 128kb High Density Portless SRAM Using Hierarchical Bitlines and Thyristor Sense Amplifiers," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2011

212. Mark Woh, Sudhir Satpathy, Ronald G. Dreslinski, Daniel Kershaw, Dennis Sylvester, David Blaauw, Trevor Mudge, "Low Power Interconnects for SIMD Computers," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011

213. Chia-Hsiang Chen, Yejoong Kim, Zhengya Zhang, David Blaauw, Dennis Sylvester, Helia Naeimi, Sumeet Sandhu "A Confidence-Driven Model for Error-Resilient Computing," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011

214. Gregory Chen, Hassan Ghaed, Razi-Ul Haque, Michael Wieckowski, Yejoong Kim, Gyouho Kim, David Fick, Daeyeon Kim, Mingoo Seok, Kensall Wise, David Blaauw, Dennis Sylvester, "A 1 Cubic Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor," IEEE International Solid-State Circuits Conference (ISSCC), February 2011

215. Mingoo Seok, Dongsuk Jeon, Chaitali Chakrabarti, David Blaauw, Dennis Sylvester, "A 0.27V, 30MHz, 17.7nJ/transform 1024-pt complex FFT core with super-pipelining," IEEE International Solid-State Circuits Conference (ISSCC), February 2011

216. Yoonmyung Lee, Bharan Giridhar, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "A 660pW Multi-Stage Temperature Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization," IEEE International Solid-State Circuits Conference (ISSCC), February 2011

217. Zhiyoong Foo, David Devecsery, Thomas Schmid, Nathan Clark, Mohammad Ghaed, Ye-Sheng Kuo, Inhee Lee, Yongmin Park, Nathaniel Slottow, Vikas Vinay, Micheal Wieckowski, Dongmin Yoon, Cliff Schmidt, David Blaauw, Peter Chen, Prabal Dutta, "A Case for Custom Silicon in Enabling Low-Cost Information Technology for Developing Regions," ACM Symposium on Computing for Development, December 2010

218. Yoonmyung Lee, Mao-Ter Chen, Junsun Park, Dennis Sylvester, David Blaauw, "A 5.42nW/kB Retention Power Logic-Compatible Embedded DRAM with 2T Dual-Vt Gain Cell for Low Power Sensing Applications," Asian Solid-State Circuits Conference (A-SSCC), November 2010

219. Vineeth Veetil, Dennis Sylvester, David Blaauw, "A Lower Bound Computation Method for Evaluation of Statistical Design Techniques," ICCAD 2010, November 2010

220. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analysis and Optimization of SRAM Robustness for Double Patterning Lithography," ICCAD 2010, November 2010

221. Cheng Zhuo, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Active Learning Framework for Post-Silicon Variation Extraction and Test Cost Reduction," ICCAD 2010, November 2010

222. Prashant Singh, Eric Karl, Dennis Sylvester, David Blaauw, "Dynamic NBTI Management Using a 45nm Multi-Degradation Sensor," IEEE Custom Integrated Circuts Conference (CICC), **Invited Paper** to the *Special Issue on CICC, IEEE Transactions on Circuits and Systems I*: *Analog and Digital Signal Processing* (*T-CAS*), September 2010

223. Vivek Joshi, Michael Wieckowski, Gregory Chen, David Blaauw, Dennis Sylvester, "Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS," IEEE Custom Integrated Circuts Conference (CICC), September 2010

224. Mingoo Seok, Gyouho Kim, David Blaauw, Dennis Sylvester, "Variability Analysis of a Digitally Trimmable Ultra-Low Power Voltage Reference," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010

225. Greg Chen, Michael Wieckowski, David Blaauw, Dennis Sylvester, "Crosshairs SRAM - An Adaptive Memory for Mitigating Parametric Failures," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2010

226. Mingoo Seok, David Blaauw, Dennis Sylvester, "Clock Network Design for Ultra-Low Power Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2010

227. Nurrachman Liu, Scott Hanson, Dennis Sylvester, David Blaauw, "OxID: On-Chip One-Time Random ID Generation using Oxide Breakdown," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010

228. Sudhir Satpathy, Zhiyoong Foo, Bharan Giridhar, Dennis Sylvester, Trevor Mudge, David Blaauw, "A 1.07 Tbit/s 128x128 Swizzle Network for SIMD Processors," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2010

229. Vineeth Veetil, Yung-Hsu Chang, Dennis Sylveter, David Blaauw, "Efficient Smart Monte Carlo based SSTA on Graphics Processing Units with Improved Resource Utilization," ACM/IEEE Design Automation Conference (DAC), June 2010

230. Vivek Joshi, "Closed-Form Modeling of Layout-Dependent Mechanical Stress," ACM/IEEE Design Automation Conference (DAC), June 2010

231. Mingoo Seok, Scott Hanson, Michael Wieckowski, Gregory K. Chen, Yu-Shiang Lin, David Blaauw, Dennis Sylvester, "Circuit Design Advances to Enable Ubiquitous Sensing Environments," IEEE International Symposium on Circuits and Systems (ISCAS), May 2010

232. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Process Variation and Temperature Aware Reliability Management," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010

233. Michael Wieckowski, Dennis Sylvester, David Blaauw, "A Black Box Method for Stability Analysis of Arbitrary SRAM Cell Structures," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2010

234. David Bull, Shidhartha Das, Karthik Shivashankar, Ganesh Dasika, Krisztian Flautner, David Blaauw, "A Power-efficient 32bit ARM ISA Processor using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC,* February 2010

235. Prashant Singh, Zhiyoong Foo, Michael Wieckowski, Scott Hanson, Matt Fojtik, David Blaauw, Dennis Sylvester, "Early Detection of Oxide Breakdown Through In Situ Degradation Sensing," IEEE International Solid-State Circuits Conference (ISSCC), February 2010

236. Jae-sun Seo, Ron Ho, Jon Lexau, Michael Dayringer, Dennis Sylvester, David Blaauw, "High Bandwidth and Low Energy On-Chip Signaling with Adaptive Pre-Emphasis in 90nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), February 2010

237. Gregory Chen, Matthew Fojtik, Daeyeon Kim, David Fick, Junsun Park, Mingoo Seok, Mao-Ter Chen, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "A Millimeter-Scale Nearly-Perpetual Sensor System with Stacked Battery and Solar Cells," IEEE International Solid-State Circuits Conference (ISSCC), February 2010

238. David Fick, Nurrachman Liu, Zhiyoong Foo, Matthew Fojtik, David Blaauw, Dennis Sylvester, "In Situ Delay Slack Monitor for High-Performance Processors using an All-Digital, Self-Calibrating 5ps Resolution Time-to-Digital Converter," IEEE International Solid-State Circuits Conference (ISSCC), February 2010

239. Cheng Zhuo, Yung-Hsu Chang, Dennis Sylvester, David Blaauw, "Design Time Body Bias Selection for Parametric Yield Improvement," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010

240. Vivek Joshi, Kanak Agarwal, Dennis Sylvester, David Blaauw, "Analyzing Electrical Effects of RTA-driven Local Anneal Temperature Variation," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2010
241. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Post-Fabrication Measurement-Driven Oxide Breakdown Reliability Prediction and Management," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2009
242. Ravikishore Gandikota, David Blaauw, Dennis Sylvester**,** "Interconnect Performance Corners considering Crosstalk Noise," IEEE International Conference on Computer Design (ICCD), October 2009
243. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Near-Field Communications using Phase-Locking and Pulse Signalling for Millimeter-Scale Systems," IEEE Custom Integrated Circuts Conference (CICC), September 2009
244. Mingoo Seok, Gyouho Kim, Dennis Sylvester, David Blaauw, "A 0.5V 3.6ppm/0C 2.2pW 2-Transistor Voltage Reference," IEEE Custom Integrated Circuts Conference (CICC), September 2009
245. Daeyeon Kim, Yoonmyung Lee, Jin Cai, Leland Chang, Steven J. Koester, Dennis Sylvester, David Blaauw, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009, **Best Paper Award**
246. Ronald G. Dreslinski, David Fick, David Blaauw, Dennis Sylvester, Trevor Mudge, "Reconfigurable Multicore Server Processors for Low Power Operation," International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS), July 2009
247. Vineeth Veetil, Dennis Sylvester, David Blaauw, Saumil Shah, Steffen Rochel, "Efficient Smart Sampling based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence," ACM/IEEE Design Automation Conference (DAC), July 2009
248. Ravikishore Gandikota, Li Ding, Peivand Tehrani, David Blaauw, "Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models," ACM/IEEE Design Automation Conference (DAC), July 2009
249. David Fick, Andrew DeOrio, Jin Hu, David Blaauw, Dennis Sylvester, Valeria Bertacoo, "Vicis: A Reliable Network for Unreliable Silicon," ACM/IEEE Design Automation Conference (DAC), July 2009
250. Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Crosstalk-Aware PWM-Based On-Chip Global Signaling in 65nm CMOS," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
251. Mike Wieckowski, Gregory K. Chen, Mingoo Seok, David Blaauw, Dennis Sylvester, "A hybrid DC-DC Converter for Sub-Microwatt Sub-IV Implantable Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2009
252. David Fick, Andrew DeOrio, Gregory Chen, Valeria Bertacoo, Dennis Sylvester, David Blaauw, "A Highly Resilient Routing Algorithm for Fault-Tolerant NoCs," ACM/IEEE Design Automation and Test in Europe Conference (DATE), April 2009
253. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A 150pW Program-and-Hold Timer for Ultra-Low Power Sensor Platforms," IEEE International Solid-State Circuits Conference (ISSCC), February 2009
254. Carlos Tokunaga, David Blaauw, "Secure AES engine with a local switched capacitor current equalizer," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2009

255. Ronald Dreslinski, Greg Chen, Trevor Mudge, David Blaauw, Dennis Sylvester, Krisztian Flautner, "Reconfigurable Energy Efficient Near Threshold Cache Architectures," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2008

256. Brian Cline, Vivek Joshi, Dennis Sylvester, David Blaauw, "Stress-Enhanced Standard Cell Library Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008

257. Jae-Sun Seo, Igor Markov, Dennis Sylvester, David Blaauw, "On the Decreasing Significane of Large Standard Cells in Technology Mapping,"ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008

258. Kaviraj Chopra, Cheng Zhuo, David Blaauw, Dennis Sylvester, Vladimir Zolotov, "A Statistical Approach for Full-Chip Gate-Oxide Reliability Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2008

259. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "An Ultra Low Power 1V, 220nW Temperature Sensor for Passive Wireless Applications," IEEE Custom Integrated Circuts Conference (CICC), September 2008

260. Mingoo Seok, Scott Hanson, Jae-Sun Seo, Dennis Sylvester, David Blaauw, "Robust Ultra-Low Voltage ROM Design," IEEE Custom Integrated Circuts Conference (CICC), September 2008

261. Michael Wieckowski, Young Min Park, Carlos Tokunaga, Dong Woon Kim, Zhiyoong Foo, Dennis Sylvester, David Blaauw, "Timing Yield Enhancement Through Soft Edge Flip-Flop Based Design," IEEE Custom Integrated Circuts Conference (CICC), September 2008

262. Sanjay Pant, David Blaauw, "Circuit Techniques for Suppression and Measurement of On-chip Inductive Supply Noise," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008

263. Yoonmyung Lee, Mingoo Seok, Scott Hanson, David Blaauw, Dennis Sylvester, "Standby Power Reduction Techniques for Ultra-Low Power Processors," IEEE European Solid-State Circuits Conference (ESSCIRC), September 2008

264. Cheng Zhuo, David Blaauw, Dennis Sylvester, "Variation-Aware Gate Sizing and Clustering for Post-Silicon Optimized Circuits," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008

265. Mingoo Seok, Dennis Sylvester, David Blaauw, "Optimal Technology Selection for Minimizing Energy and Variability in Low Voltage Applications," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2008

266. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Sensor Data Retrieval Using Alignment Independent Capacitive Signaling," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*, June 2008

267. Mingoo Seok, Scott Hanson, Yu-Shiang Lin, Zhiyoong Foo, Dayeon Kim, Yoonmyung Lee, Nurrachman Liu, Dennis Sylvester, David Blaauw, "The Phoenix Processor: A 30pW Platform for Sensor Applications," IEEE Symposium on VLSI Circuits (VLSI-Symp), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on VLSI Circuits*, June 2008

268. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Modeling Crosstalk in Statistical Static Timing Analysis", ACM/IEEE Design Automation Conference (DAC), June 2008

269. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Leakage Power Reduction Using Stress-Enhanced Layouts," ACM/IEEE Design Automation Conference (DAC), June 2008

270. Vineeth Veetil, Dennis Sylvester, David Blaauw, "Efficient Monte Carlo based Incremental Statistical Timing Analysis," ACM/IEEE Design Automation Conference (DAC), June 2008
271. Yu-Shiang Lin, Scott Hanson, Fabio Albano, Carlos Tokunaga, Razi-Ul Haque, Kensall Wise, Ann Marie Sastry, David Blaauw, Dennis Sylvester, "Low-Voltage Circuit Design for Widespread Sensing Applications," IEEE International Symposium on Circuits and Systems (ISCAS), May 2008
272. Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw, Kanak Agarwal, "Stress Aware Layout Optimization", ACM/IEEE International Symposium on Physical Design (ISPD), April 2008
273. Eric Karl, David Blaauw, Dennis Sylvester, "Analysis of System-Level Reliability Factors and Implications on Real-time Monitoring Methods for Oxide Breakdown Device Failures," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2008
274. Brian Cline, Kaviraj Chopra, David Blaauw, Andres Torres, Savithri Sundareswaran, "Transistor-Specific Delay Modeling for SSTA," ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2008
275. Eric Karl, Prashant Singh, David Blaauw, Dennis Sylvester, "Compact in situ Sensors for Monitoring NBTI and Oxide Degradation," IEEE International Solid-State Circuits Conference (ISSCC), February 2008
276. David Blaauw, Sudherssen Kalaiselvan, Kevin Lai, Wei-Hsiang Ma, Sanjay Pant, Carlos Tokunaga, Shidhartha Das, David Bull, "RazorII: In-Situ Error Detection and Correction for PVT and SER tolerance," IEEE International Solid-State Circuits Conference (ISSCC), **Invited Paper** to the *IEEE Journal of Solid-State Circuits (JSSC), Special Issue on ISSCC*, February 2008
277. Sanjay Pant, David Blaauw, "A Charge-Injection Based Active Decoupling Technique for Inductive Supply Noise Suppression," IEEE International Solid-State Circuits Conference (ISSCC), February 2008
278. Gregory Chen, David Blaauw, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, "Yield-driven Near-threshold SRAM Design," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
279. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Murat Becer, "Victim Alignment in Crosstalk Aware Timing Analysis," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
280. Vivek Joshi, David Blaauw, Dennis Sylvester, "Soft-edge Flip-flops for Improved Timing Yield: Design and Optimization," ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2007
281. Ronald G. Dreslinski, Bo Zhai, Trevor Mudge, David Blaauw, Dennis Sylvester, "An Energy Efficient Parallel Architecture Using Near Threshold Operation," Parallel Architectures and Compilation Techniques (PACT), September 2007
282. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "A sub-pW timer using gate leakage for ultra low power sub-Hz monitoring systems," IEEE Custom Integrated Circuts Conference (CICC), September 2007
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407. Sergey Gavrilov, Alexey Glebov, Sergey Rusakov, David Blaauw, Larry Jones, Gopal Vijayan, "Fast Power Loss Calculation for Digital Static CMOS Circuits," ACM/IEEE European Design and Test Conference (ED&T), March 1997, 411-415
408. Alexey Glebov, David Blaauw, Larry Jones, "Transistor Reordering for Low Power CMOS Gates Using an SP-BDD Representation," ACM/IEEE International Symposium on Low Power Design (ISLPD), April 1995, pg. 161-166
409. David Blaauw, Larry Jones, "Reducing the Scheduling Cost in Event-Driven Simulation through Component Clustering," ACM/IEEE European Conference on Design Automation (EDAC), February 1993, pg. 18-22
410. David Blaauw, Daniel Saab, Prith Banerjee, Jacob Abraham, "Functional Abstraction of Logic Gates for Switch-Level Simulation," ACM/IEEE European Conference on Design Automation (EDAC), February 1991, pg. 329-333
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412. David Blaauw, Prith Banerjee, Jacob Abraham, "Automatic Classification of Node Types in Switch-Level Descriptions," IEEE International Conference on Computer Design (ICCD), September 1990, pg. 175-178
413. Daniel Saab, Robert Mueller-Thuns, David Blaauw, Joe Rahmeh, Jacob Abraham, "Fault Grading of Large Digital Systems," IEEE International Conference on Computer Design (ICCD), September 1990, pg. 290-293
414. David Blaauw, Daniel Saab, Junsheng Long, and Jacob Abraham, "Derivation of Signal Flow for Switch-Level Simulation," ACM/IEEE European Conference on Design Automation (EDAC), March 1990, pg. 301-305
415. David Blaauw, Daniel Saab, Robert Mueller-Thuns, Jacob Abraham, Joe Rahmeh, "Automatic Generation of Behavioral Models," ACM/IEEE Design Automation Conference (DAC), June 1989, pg. 179-184

416. Daniel Saab, Robert Mueller-Thuns, David Blaauw, Jacob Abraham, Joe Rahmeh, "CHAMP: Concurrent and Multilevel Program for Simulation of VLSI Circuit," ACM/IEEE International Conference on Computer Aided Design (ICCAD), November 1988, pg. 246-249

F. Workshop Papers

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2. Fabio Frustaci, David Blaauw, Dennis Sylvester, Massimo Alioto, "Better-than-Voltage Scaling Energy Reduction in Approximate SRAMs via Bit Dropping and Bit Reuse," Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), September 2015
3. Pat Pannuto, Yoonmyung Lee, Zhiyoong Foo, David Blaauw and Prabal Dutta, "M3: A mm-scale Wireless Energy Harvesting Sensor Platform," The First International Workshop on Energy Neutral Sensing Systems (ENSSys), November 2013
4. Yoonmyung Lee, Ye-Sheng Kuo, Pat Pannuto, Ron Dreslinski, Prabal Dutta, David Blaauw, "Architectural Challenges for MM-scale Sensor Nodes," The First International Workshop on the Swarm at the Edge of the Cloud (SEC'13) September 2013
5. Ronald Dreslinski, Bharan Giridhar, Nathan Pinckney, David Blaauw, Trevor Mudge, "Reevaluating Fast Dual-Voltage Power Rail Switching Circuitry," 10th Annual Workshop on Duplicating, Deconstructing and Debunking (WDDD12) June 2012
6. Pat Pannuto, Yoonmyung Lee, Ben Kempke, Dennis Sylvester, David Blaauw, Prabal Dutta, "Demo: Ultra-Constrained Sensor Platform Interfacing," Information Processing in Sensor Networks (IPSN), April 2012
7. David Fick, Ronald G. Dreslinski, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wiekowski, Gregory Chen, Trevor Mudge, Dennis Sylvester, David Blaauw, "Centip3De: A 7-Layer 3D System With 128 ARM Cortex-M3 Cores and 256MB of DRAM," 3D Integration Workshop, ACM/IEEE Design Automation and Test in Europe Conference (DATE), March 2011
8. Vivek Joshi, Valeriy Sukharev, Andres Torres, Dennis Sylvester, David Blaauw, "Closed-Form Modeling of Layout-Dependent Mechanical Stress," *Design for Manufacturability and Yield (DFM&Y)*, July 2009
9. Ronald Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvster, Trevor Mudge, "Near Threshold Computing: Overcoming Performance Degradation from Aggressive Voltage Scaling," Workshop on Energy-Efficient Design (WEED), June 2009
10. Ravikishore Gandikota, David Blaauw, Li Ding, Peivand Tehrani, "Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models," ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2009
11. David Blaauw, James Kitchener, Braden Phillips, "Optimizing addition for sub-threshold logic," Forty-Second Asilomar Conference on Signals, Systems and Computers, October 2008
12. Jae-Sun Seo, Igor Markov, Dennis Sylvester, David Blaauw, "On the Decreasing Significance of Large Standard Cells in Technology Mapping," International Workshop on Logic & Synthesis (IWLS), June 2008
13. Ravikishore Gandikota, David Blaauw, Dennis Sylvester, "Modeling Crosstalk in Statistical Static Timing Analsys," ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2008

14. Vineeth Veetil, Dennis Sylvester, David Blaauw, “Efficient Monte Carlo based Incremental Statistical Timing Analysis,” ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2008
15. David Roberts, Ronald G. Dreslinski, Eric Karl, Trevor Mudge, Dennis Sylvester, David Blaauw, “When Homogeneous becomes Heterogeneous,” Parallel Architectures and Compilation Techniques (PACT) workshop on Operating Systems support for Heterogeneous Multicore Architectures, September 2007
16. Mini Nanua, “Crosstalk Waveform Modeling Using Wave Fitting,” IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos) September 2007
17. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester, Murat Becer, “Top-k aggressors set in Delay Noise Analysis,” ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2007
18. Vineeth Veetil, Dennis Sylvester, David Blaauw, “Fast and Accurate Waveform Analysis with Current Source Models,” ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2007
19. Vineeth Veetil, Dennis Sylvester, David Blaauw, “Criticality Aware Latin Hypercube Sampling for Efficient Statistical Timing Analysis,” ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2007
20. Kaviraj Chopra, Narendra Shenoy, David Blaauw, “Variogram Based Robut Extraction of Process Variation,” ACM/IEEE International Workshop on Timing Issues, Febraury 2007
21. Fabio Albano, David Blaauw and Dennis Sylvester, Ann Mary Sastry, “Design and Optimization of Hybrid Power Systems for Fully Implantable Medical Devices,” Joint International Meeting Symposium on Bioelectronics, Biointerfaces, and Biomedical Applications 2, November 2006
22. Mini Nanua and David Blaauw, “Receiver Modeling for Static Functional Crosstalk Analysis,” IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos), September 2006
23. Sanjay Pant, David Blaauw, “Timing-aware Decoupling Capacitance Allocation in Power Distribution Networks,” in ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006
24. Kavi Chopra, Bo Zhai, David Blaauw, Dennis Sylvester “A New Statistical Max Operation for Propagating Skewness in Statistical Timing Analysis”, ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006
25. Kavi Chopra, Chandramouli Kashyap, Haihua Su, David Blaauw “Current Source Driver Model Synthesis and Worst-case Alignment for Accurate Timing and Noise Analysis”, ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006
26. Smitha Shyam, Sujay Phadke, Benjamin Lui, Hitesh Gupta, Valeria Bertacco, David Blaauw, “VOLTaiRE: Low-cost Fault Detection Solutions for VLIW Microprocessors,” Workshop on Introspective Architecture (WISA), February 2006.
27. Amir Borna, Christopher Progler, David Blaauw, “Correlation Analysis of CD-Variation and Circuit Performance Under Multiple Sources of Variability,” SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, May 2005
28. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, “Statistical Timing Based Optimization Using Gate Sizing,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005

29. Amit Jain, David Blaauw, Vladimir Zolotov, “Accurate Gate Delay Model for Arbitrary Waveform Shapes,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005
30. Christopher Progler, Amir Borna, David Blaauw, Pierre Sixt, “Impact of lithography variability on statistical timing behavior,” SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, Ed., Vol. 5379, May 2004, pg. 101-110
31. Amit Jain, David Blaauw, “Modeling Flip-Flop Delay Dependencies in Timing Analysis,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2004
32. Aseem Agarwal, David Blaauw, Vladimir Zolotov, Sarma Vrudhula, “Statistical Timing Analysis Using Bounds and Selective Enumeration,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 29-36
33. Aseem Agarwal, David Blaauw, Savithri Sundareswaran, Vladimir Zolotov, Min Zhou, Kaushik Gala, Rajendran Panda, “Path-Based Statistical Timing Analysis Considering Inter- and Intra-Die Correlations,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 16-21
34. Himanshu Kaul, Dennis Sylvester, David Blaauw, “Active Shielding of RLC Global Interconnects,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 98-104
35. Kanak Agarwal, Dennis Sylvester, David Blaauw, “A Library Compatible Driving Point Model for On-Chip RLC Interconnects,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 63-69
36. Bhavana Thudi, David Blaauw, “Efficient Switching Window Computation For Cross-Talk Noise,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 84-91
37. Fadi Aloul, Soha Hassoun, Karem Sakallah, David Blaauw, “Robust SAT-Based Search Algorithm for Leakage Power Reduction,” IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), September 2002, pg. 167-177
38. Murat Becer, David Blaauw, Ibrahim Hajj, Rajendran Panda, “Early Probabilistic Noise Estimation for Capacitively Coupled Interconnects,” ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP), April 2002, pg. 77-83
39. David Blaauw, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop - Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
40. Vladimir Zolotov, David Blaauw, Rajendran Panda, Chanhee Oh, Savithri Sundareswaran, “Slope Propagation in Static Timing Analysis,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 91-96
41. Supamas Sirichotiyakul, David Blaauw, Chanhee Oh, Rafi Levy, Vladimir Zolotov, “Driver Modeling and Alignment for Worst-Case Delay Noise,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 1-7
42. David Blaauw, Tim Edwards, “Generating False Path Free Timing Graphs Using Node Splitting,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), March 1999, pg. 112-117
43. David Blaauw, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
44. Daksh Lenther, Satya Pullela, David Blaauw, Shantanu Ganguly, “Hierarchical Clock-network Optimization,” ACM Physical Design Workshop, April 1996, pg. 49-54

45. John Willis, Rob Newshutz, Lance Thompson, Jeff Graves, Tom Dillinger, Jeff Snyder, Nimish Radia, Joe Skovira, David Blaauw, Sidhartha Mohanty, Zhiyuan Li, Sandra Samelson, Matt Lin, "MinSim: Optimized, Compiled VHDL Simulation Using Networked & Parallel Computers," IEEE VHDL International User Forum, October 1993, pg. 137-144

G. Patents Issued

1. "Wireless Neural Recording Devices And System With Two Stage RF And NIR Power Delivery And Programming," Patent number 17/173,976, issued February 11, 2021
2. "Millimeter-Scale Bluetooth Low Energy transmitter with dual purpose loop antenna," Patent number 10,911,078, issued February 2, 2021
3. "Low-Power, Long-Range RF Localization System and Method," Patent number 10,746,844, issued August 18, 2020
4. "Analog-To-Digital Conversion Circuit and Image Sensor Including the Same," Patent Number 10,594,333, issued March 17, 2020
5. "Variation-tolerant voltage reference," Patent number 10310537, issued June 4, 2019
6. "Intraocular pressure sensor with improved voltage reference circuit," Patent number 10,285,590, issued May 14, 2019
7. "Self-oscillating switched-capacitor DC-DC converter," Patent number 9,979,284, issued May 22, 2018
8. "Floating-gate transistor array for performing weighted sum computation," Patent number 9,760,533, issued September 12, 2017
9. "Electrostatic discharge clamp circuit for ultra-low power applications," Patent number 9,716,381, issued July 25, 2017
10. "Measurement circuitry and method for measuring a clock node to output node delay of a flip-flop," Patent number 9,638,752, issued May 2, 2017
11. "Ultra Low Power Temperature Insensitive Current Source With Line and Load Regulation," Patent Number 9,639,107, issued May 2, 2017
12. "Protocol for an electronic device to receive a data packet from an external device," Patent number 9,635,147, issued April 25, 2017
13. "Integrated circuit using topology configurations," Patent Number 9,589,601 issued March 7, 2017
14. "Single Cycle Arbitration Within an Interconnect," Patent Number 9,514,074 B2 issued December 6, 2016
15. "Error recovery within integrated circuit," Patent Number 9,448,875, issued September 20, 2016
16. "Storage Device Supporting Logical Operations, Methods and Storage Medium," Patent Number 9,396,795, issued July 19, 2016.
17. "Low Power Oscillator with Charge Subtraction Scheme," Patent Number 9,385,692, July 5, 2016
18. "True random number generator," Patent Number 9,335,972, May 10, 2016
19. "Memory Circuit Including Read Voltage Boost," Patent Number 9,275,702 issued March 1, 2016
20. "Error Recovery Within Integrated Circuit," Patent Number 9,164,842 issued October 20, 2015
21. "Low Power Reference Current Generator with Tunable Temperature," Patent Number 9147443 issued September 29, 2015
22. "Randomized Value Generation," Patent Number 8,930,427 issued January 6, 2015

23. “Crossbar circuitry for applying an adaptive priority scheme,” Patent Number 8,868,817 issued October 21, 2014
24. “Apparatus and Method for Transferring a Data Signal Propagated Along a Bidirectional Communication Path Within a Data Processing Apparatus,” Patent Number 8,713,232 issued April 29, 2014
25. “Error Recovery Within Integrated Circuit” Patent Number 8,650,470 issued February 11, 2014
26. “Reference voltage generator having a two transistor design,” Patent Number 8,564,275 issued October 22, 2013
27. “Crossbar circuitry for applying an adaptive priority scheme and method of operation of such crossbar circuitry,” Patent Number 8,549,207 issued October 1, 2013
28. “Integrated circuit memory power supply,” Patent Number 8,526,261 issued Setember 3, 2013
29. “Vertical interconnect patterns in multi-layer integrated circuits,” Patent Number 8,381,155 issued February 19, 2013
30. “Random Number Generator,” Patent Number 8,346,832 issued January 1, 2013
31. “Cache memory system for a data processing apparatus,” Patent Number 8,335,122 issued December 18, 2012
32. “Stalling synchronization circuits in response to a late data signal,” Patent Number 8,276,014 issued September 25, 2012
33. “Crossbar circuitry for applying a pre-selection prior to arbitration between transmission requests and method of operation of such crossbar circuitry,” Patent Number 8,255,610, issued August 28, 2012
34. “Crossbar circuitry and method of operation of such crossbar,” Patent Number 8,230,152, issued July 24, 2012
35. “Single Event Upset Error Detection Within an Integrated Circuit,” Patent Number 8,185,812, issued May 22, 2012
36. “Error Recovery Within Processing Stages of an Integrated Circuit,” Patent Number 8,185,786, issued May 22, 2012
37. “Memory Cell Structure, a Memory Device Employing Such a Memo,” Patent Number 8,107,290, issued January 31, 2012
38. “Crossbar Circuitry and Method of Operation of Such Crossbar” Patent Number 8,108,585, issued on January 31, 2012
39. “Error Detection in Precharged Logic,” Patent Number 8,103,922, issued on January 24, 2012
40. “Error Detection in Precharged Logic,” Patent Number 8,006,147, issued on August 23, 2011
41. “Isolation Circuity and Method for Hiding a Power Consumption Characteristic of an Associated Processing Circuit,” Patent Number 7,880,339, issued on February 1, 2011
42. “Integrated Circuit Memory Access Mechanisms,” Patent Number 7,864,562, issued on January 4, 2011
43. “On-chip Power Supply Voltage Regulation,” Patent Number 7,839,129, issued on November 23, 2010
44. “Integrated Circuit with Error Correction Mechanisms to Offset Narrow Tolerancing,” Patent Number 7,701,204, issued on April 20, 2010
45. “Error Detection and Recovery Within Processing Statges of an Integrated Circuit,” Patent Number 7,650,551, issued on January 19, 2010

46. “Data Processor Memory Circuit,” Patent Number 7,533, 226, issued on May 12, 2009
47. “Systematic and Random Error Detection and Recovery Within Processing Stages of An Integrated Circuit,” Patent Number 7,337,356, issued on February 26, 2008
48. “Error Recovery Within Processing Stages of an Integrated Circuit,” Patent Number 7,320,091, issued on January 15, 2008
49. “Data Retention Latch Provision Within Integrated Circuits,” Patent Number 7,310,755, issued on December 18, 2007
50. “Error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,278,080, issued on October 2, 2007
51. “Address Decoding,” Patent Number 7,263,015, issued on August 28, 2007
52. “Systematic and random error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,162,661, issued on January 9, 2007
53. “Methods for analyzing integrated circuits and apparatus therefor,” Patent Number 7,149,674, issued on December 12, 2006
54. “Noise analysis for an integrated circuit model,” Patent Number 7,093,223, issued on August 15, 2006
55. “Memory System having Fast and Slow Data Reading Mechanisms,” Patent Number 7,072,229, issued on July 4, 2006
56. “Data Processor Memory Circuit,” Patent Number 7,055,007, issued on May 30, 2006
57. “Memory System Having Fast and Slow Data Reading Mechanisms,” Patent Number 6,944,067, issued on September 13, 2005
58. “Actively-Shielded Signal Wires,” Patent Number 6,919,619, issued on July 19, 2005
59. “Method and Apparatus for Controlling Current Demand in an Integrated Circuit”, Patent Number 6,819,538, issued on November 16, 2004
60. “Cross Coupling Delay Characterization for Integrated Circuits,” Patent Number 6,799,153, issued on September 28, 2004
61. “Iterative, Noise-Sensitive Method of Routing Semiconductor Nets,” Patent Number 6,480,998, issued on November 12, 2002
62. “Waveform Manipulation in Time Warp Simulation,” Patent Number 6,195,628, issued on February 27, 2001
63. “Optimizing Combinational Circuit Layout through Iterative Restructuring,” Patent Number 6,074,429, issued on June 13, 2000
64. “In-Transit Message Detection for Global Virtual Time Calculation in Parallel Time Warp Simulation,” Patent Number 5,956,261, issued on September 21, 1999
65. “Method for Optimizing Element Sizes in a Semiconductor Device,” Patent Number 5,903,471, issued on May 11, 1999
66. “Updating Hierarchical DAG Representations through a Bottom up Method,” Patent Number 5,790,416, issued on August 4, 1998
67. “Complementary Network Reduction for Load Modeling,” Patent Number 5,790,415, issued on August 4, 1998
68. “Simulation Corrected Sensitivity,” Patent Number 5,787,008, issued on July 28, 1998

69. “Accurate Delay Prediction Based on Multi-Model Analysis,” Patent Number 5,751,593, issued on May 12, 1998

70. “Apparatus and Method for the Automatic Determination of a Standard Library Height within an Integrated Circuit Design,” Patent Number 5,737,236, issued April 7, 1998

71. “Integrated Circuit Design and Manufacturing Method and an Apparatus for Designing an Integrated Circuit in Accordance with the Method,” Patent Number 5,689,432, issued on November 18, 1997

72. “Method and Apparatus for Designing an Integrated Circuit,” Patent Number 5,666,288, issued on September 9, 1997

73. “Logic Gate Size Optimization Process for an Integrated Circuit Whereby Circuit Speed is Improved While Circuit Areas is Optimized,” Patent Number 5,619,418, issued on April 8, 1997

74. “Message Sequence Number Control in a Virtual Time System,” Patent Number 5,617,561, issued on April 1, 1997

VI Scholarly Addresses

A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, "The Internet of Tiny Things - IoT^2: Challenges and Opportunities in mm-Scale Computing," ECE Distinguished Lecture Series, George Washington University, December 2018
2. Plenary Keynote Address, "Unlocking New IoT Application Domains Through Ultra-Low Power mm-Scale Sensor Node Design," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), July 2018
3. Invited presentation, "Low-Power Circuit Techniques for IoT Energy Harvesting," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2016
4. Plenary Keynote Address, "From Digital Processors to Analog Building Blocks: Enabling New Applications through Ultra-Low Voltage Design," IEEE Subthreshold Microelectronics Conference (SubVt), October 2012
5. Invited presentation, "Adaptive Sensing and Design for Reliability," IEEE International Reliability Physics Symposium, May 2010
6. Invited presentation, "Architectural Techniques for Self-Adaptive Computing," IEEE International Solid-State Circuits Conference (ISSCC), February 2007
7. Invited presentation, "Energy Optimality and Variability in Subthreshold Design," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
8. Invited presentation, "Energy Efficient Design for Subthreshold Supply Voltage Operation," IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
9. Invited presentation, "Extended Dynamic Voltage Scaling for Low Power Design," IEEE International SOC Conference, September 2004
10. Invited presentation, "Signal Integrity Issues in High Performance Design," IEEE International Workshop-Power and Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001
11. Invited presentation, "Inductance 101: Analysis and Design," ACM/IEEE Design Automation Conference, June 2001
12. Invited presentation, "Inductance Extraction and Modeling," ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
13. Keynote address, "Power Management Issues in High Performance Processor Design," IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
14. Keynote address, "Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

VII Professional Activities

A. Professional Societies

- Fellow of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design & Test of Computers*, special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), special issue on Low Power Electronics, 1999

C. Conference and Workshop Organization

- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2018 - current
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006 – 2009
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004 - 2007
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999 - 2006
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997, 2005 – 2006
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002 - 2004
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2003
- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001 - 2002
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

D. Consulting & Advisory Boards

- **Technical Consulting and Advisory boards**
    - Member of University of Illinois at Urbana – Champaign Advisory Panel 2013 – current

- Gear Inc. 2013 – 2015
- Apache Design Automation – member of advisory board
- Nascentric, Technical Consulting, 2008
- CLK Design Automation (CLK-DA), Technical Consulting, 2005 – 2008

- **Legal Consulting**
  - Parkins Coie LLP, 2014 – 2015
  - WilmerHale, 2012 – 2013
  - Alston & Bird, 2010 – 2011
  - Weil, Gotshal & Manges, 2008 – 2010
  - WilmerHale, 2007

F. Refereeing and Reviewing

- NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)
- IEEE, IEEE T-VLSI, ACM TODAES, IEEE D&T
- DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS