A 43 nW, 32 kHz, ±4.2 ppm Piecewise Linear Temperature-Compensated Crystal Oscillator With ΔΣ-Modulated Load Capacitance

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***Abstract*— This article describes an ultralow-power (ULP) temperature-compensated crystal oscillator (TCXO) with a pulsed-injection XO driver for IoT applications. Temperature compensation is achieved by changing the load capacitance (C_L) between two values using a delta-sigma modulator (ΔΣM). The complex modulation profile across temperature is approximated as piecewise linear elements that is selected by a coarse temperature sensor. As a result, the power and area of fine-grain look-up tables (LUTs) or a polynomial engine used in prior works can be avoided. The proposed pulsed-injection XO driver that directly replenishes the energy of the C_L sustains the XO oscillation for the two different C_L states. Implemented in 40-nm CMOS, the proposed 32.768-kHz TCXO achieves an accuracy of ±4.2 ppm from −20 °C to 85 °C with just three-point trimming and an Allan deviation floor of 34 ppb while consuming 43 nW, which is an approximate 8× improvement over the recent state-of-the-art TCXOs.**

***Index Terms*— Piecewise linear (PWL) approximation, pulse injection XO, real time clock (RTC), temperature compensation, temperature-compensated crystal oscillator (TCXO).**

I. Introduction

A REAL-time clock (RTC) is often realized using a 32.768-kHz (2^{15} Hz) crystal oscillator and is essential in battery-operated IoT devices used in smart homes, industrial monitoring, etc., [1]–[12]. Since an RTC is always on, its power consumption must be much lower than other circuits of the IoT device that can be duty-cycled. Moreover, its accuracy must be high because timing uncertainty yields longer radio ON-time during synchronization, incurring high-energy penalties [2]. For example, in applications such as smart metering, clocks are required to maintain frequency error of less than ±5 ppm across a wide range of temperatures.

Recently, several ultralow-power (ULP) RTC oscillators using tuning fork crystals have been proposed, which include amplifier-based XO [6], [14], [15] or pulsed-injection XO [1]–[4], [13]. The XOs using amplifiers use an inverting amplifier or dc-sustaining amplifier and thus consume static current. Moreover, they are sensitive to process, voltage, and temperature (PVT) variation, and it is hard to tune the oscillation frequency. To avoid the use of an amplifier, pulsed-injection drivers [1]–[4], [13] that directly replenish the energy of the XO load capacitors (C_Ls) were introduced. The pulsed-injection driver provides energy via narrow pulses to compensate for the crystal energy loss only at peaks and valleys of crystal oscillation, and thus achieves high-energy efficiency. Unfortunately, existing ULP oscillators [1]–[4], [6], [13]–[15] are not temperature compensated and hence have a frequency inaccuracy of more than 100 ppm across temperature due to the inherent temperature characteristics of tuning fork crystals [16], [17].

To achieve a frequency accuracy of less than ±5 ppm, a temperature compensation scheme based on a fractional-N phase-locking loop (PLL) [7]–[9] or frequency interpolation [10] has been presented. In [7]–[9], temperature compensation is implemented using a third-order polynomial engine which controls the division value of a fractional-N PLL. In [10], temperature compensation is achieved via frequency interpolation, using duty-cycled C_L in a fractional divider and polynomial engine. While these previous works achieve good frequency accuracy, they suffer from μW-level power as they all require a polynomial engine, a high-frequency oscillator as well as a high-resolution temperature sensor.

In this article, we introduce an ULP temperature-compensated XO (TCXO) [5]. Temperature compensation is achieved by changing the C_L through a 1-bit delta-sigma modulator (ΔΣM). The complex modulation profile necessary to compensate for the temperature variation of the crystal is approximated with several piecewise linear (PWL) elements from which the needed element is selected by a coarse temperature sensor. The advantage of the proposed approach is that, unlike conventional TCXOs, the temperature is never explicitly determined or used to index a large look-up table (LUT)

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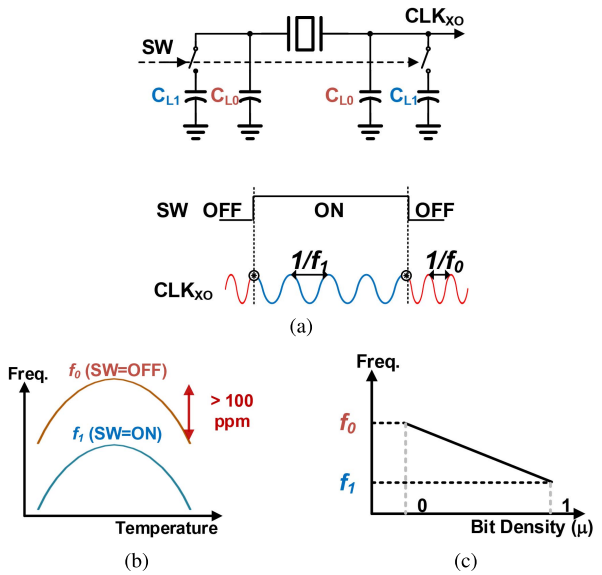

Fig. 1. (a) Concept of changing XO frequency by modulating C_L, (b) temperature characteristic of f_0 and f_1, and (c) graph of f_{avg} across μ.

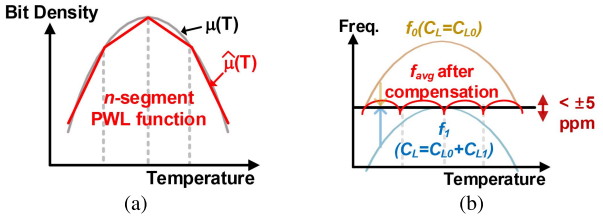

Fig. 2. (a) n-segment PWL $\widehat{\mu}(T)$ function, and (b) f_{avg} accuracy over temperature after compensation.

controlling a fine-grain capacitor DAC (CDAC) connected to the XO. Instead, only a small number of PWL parameters are stored, which are directly converted by the $\Delta\Sigma$M into the single-bit C_L modulation. The proposed TCXO achieves 43-nW power consumption at room temperature, which is 8× lower than prior state-of-the-art TCXOs while maintaining a frequency accuracy of ±4.2 ppm across a temperature range from −20 °C to 85 °C with only three-point trimming.

The article is organized as follows. In Section II, the concept of the temperature compensation scheme using a single switched C_L and the overall architecture of the proposed TCXO are described. Section III introduces the circuit implementation of the proposed pulsed-injection XO driver. Section IV presents the implementation details of the current-steering DACs, the single-bit $\Delta\Sigma$M, the dual-slope based temperature sensor, and the small LUT. Measurement results of the TCXO are presented in Section V. Finally, the article is concluded in Section VI.

II. Proposed TCXO

A. Temperature Compensation

The proposed TCXO exploits the fact that frequency of a tuning-fork crystal changes according to C_L, i.e., XO frequency increases as C_L decreases. Fig. 1(a) depicts an XO that has two different load capacitances, C_{L0} and $C_{L0}+C_{L1}$ which results in frequencies of f_0 and f_1, respectively. For each C_L, the frequency accuracy across temperature is more than 100 ppm as shown in Fig. 1(b). By switching between the two C_L values, average XO frequency (f_{avg}) can be varied. The average frequency then corresponds to the bit density (μ) of the switch connected to C_{L1}. Connecting $C_{L0}+C_{L1}$ and C_{L0} to the XO for the ratio of μ to $1-\mu$ results in an f_{avg} that is

$$f_{\text{avg}} = \frac{1}{\mu \cdot \frac{1}{f_1} + (1-\mu)\cdot \frac{1}{f_0}} \tag{1}$$

with a graph as shown in Fig. 1(c). Therefore, using a single-bit C_L modulation, we can achieve a temperature-independent f_{avg} if f_0 and f_1 are appropriately weighted and summed in time, which is similar to the $\Delta\Sigma$ divider in a fractional-N PLL. To keep a temperature independent f_{avg}, the required μ over temperature can be calculated by rearranging (1) as follows:

$$\mu(T) = \frac{\frac{1}{f_{\text{avg}}} - \frac{1}{f_0(T)}}{\frac{1}{f_1(T)} - \frac{1}{f_0(T)}} \tag{2}$$

where

$$f_0(T) = f_{0,25\,^\circ\text{C}}\left(1 + \frac{\Delta f_0(T)}{f_{0,25\,^\circ\text{C}}}\right) \tag{3}$$

$$f_1(T) = f_{1,25\,^\circ\text{C}}\left(1 + \frac{\Delta f_1(T)}{f_{1,25\,^\circ\text{C}}}\right) \tag{4}$$

$f_{0,25\,^\circ\text{C}}$ and $f_{1,25\,^\circ\text{C}}$ are f_0 and f_1 at 25 °C, respectively, and $\Delta f_0(T)$ and $\Delta f_1(T)$ are the frequency deviation of f_0 and f_1 across temperature, respectively. It is noted that the shape of the required $\mu(T)$ is similar to the temperature characteristics of XO [i.e., $((\Delta f(T))/f_{25\,^\circ\text{C}})$] which is a high-order function. To accurately implement a high-order $\mu(T)$ function on-chip, a polynomial engine or a large LUT is required. However, to reduce the cost, complexity, and power consumption, we approximate the required $\mu(T)$ using $\widehat{\mu}(T)$ with an n-segment PWL function. For example, the $\mu(T)$ and $\widehat{\mu}(T)$ of a four segment case is shown in Fig. 2(a) and its corresponding frequency error is shown in Fig. 2(b), where it can be seen that the error can be reduced, although it is larger than the case of ideal $\mu(T)$. The frequency accuracy depends on the number of PWL segments (n), where larger n results in better accuracy. This is shown in Fig. 3, where we used the above equations and PWL approximations on a commercial XO's temperature characteristics. It can be seen that $n \geq 9$ results in frequency accuracy of less than 1 ppm. In our design we chose $n = 10$ to have some margin. Moreover, to reduce the frequency error degradation caused by error in the temperature switching point due to the hysteresis or offset of the PWL segments, ±3 °C margin was added at the end of each PWL segment as shown in Fig. 4(a). With this margin, the frequency error appears as shown in Fig. 4(b), and the frequency error can be maintained even if the temperature section is selected incorrectly within ±3 °C.

To generate the PWL $\widehat{\mu}$ function, we employ two types of current sources I_a and I_b, where I_a is a temperature-proportional current, and I_b is a temperature-independent current. By combining $a \cdot I_a$ and $b \cdot I_b$, we can build a

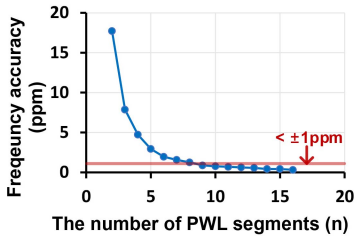

Fig. 3. Frequency accuracy over temperature according to the number of PWL segments (n).

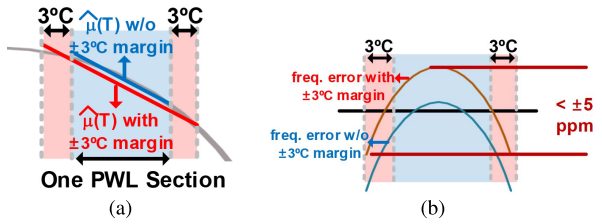

Fig. 4. (a) PWL $\widehat{\mu}(T)$ function w/ and w/o a margin of ±3 °C, and the (b) corresponding frequency error.

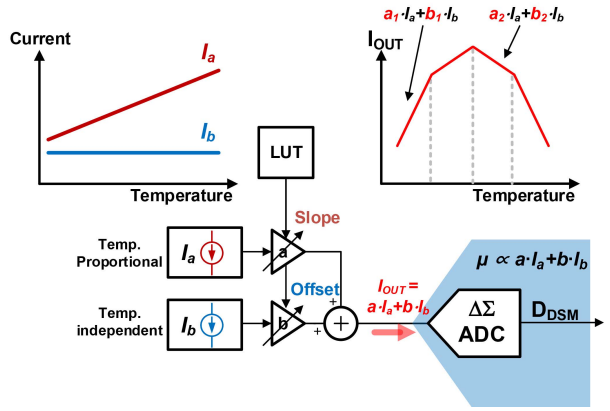

Fig. 5. Implementation of PWL μ function.

linear function of temperature with different slopes and offsets depending on coefficients (a, b). Therefore, if coefficients (a, b) are correctly set for each PWL segment, the necessary PWL current source can be created. Note that PWL coefficients (a, b) are stored in an LUT. The combined current $(a \cdot I_a + b \cdot I_b)$ is applied as the input of $\Delta\Sigma$ modulator and digitized to a single-bit stream as shown in Fig. 5. As a result, the bit density of the $\Delta\Sigma$ modulator μ_{DSM} has the same PWL $\widehat{\mu}$ shape over temperature. The output of DSM (D_{DSM}) then controls the single-bit C_L, thereby compensating f_{avg} over temperature.

B. Overall TCXO Architecture

The block diagram of the proposed TCXO is shown in Fig. 6. It consists of a coarse temperature sensor, an LUT, two current-steering DACs ($a \cdot I_a$, $b \cdot I_b$), a single-bit $\Delta\Sigma$ modulator, and a pulsed-injection XO driver. The coarse temperature sensor selects the appropriate PWL segment by having the

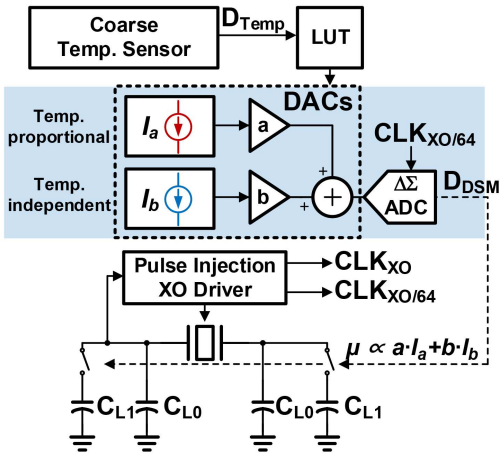

Fig. 6. Block diagram of the proposed TCXO architecture.

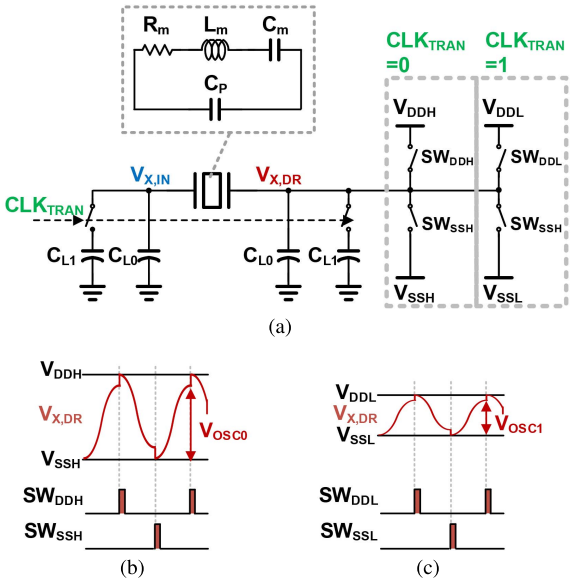

Fig. 7. Concept of the XO driver with two different C_L states. (a) Simplified circuit, and (b) abstract waveform with C_{L0} and (c) $C_{L0} + C_{L1}$.

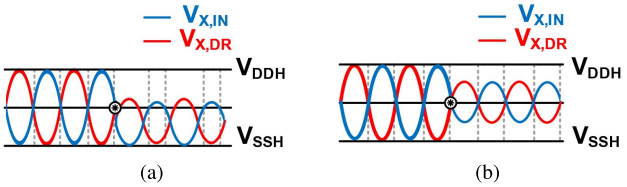

Fig. 8. C_L transition with C_{L1} pre-charge voltage of (a) V_{SSH}, and (b) middle of the oscillation.

output of the temperature sensor (D_{Temp}) index an n-entry LUT that stores n pairs of PWL parameters as coefficients (a, b).

The combined current of $a \cdot I_a + b \cdot I_b$ which represents the PWL function is then digitized by a single-bit $\Delta\Sigma$M whose output has a bit density of $\widehat{\mu}(T)$. For the XO driver, a pulsed-injection scheme is used to minimize the power consumption [1]–[4], [13]. The XO driver handles two load capacitance states (C_{L0}, $C_{L0} + C_{L1}$) and injects energy at the peak and

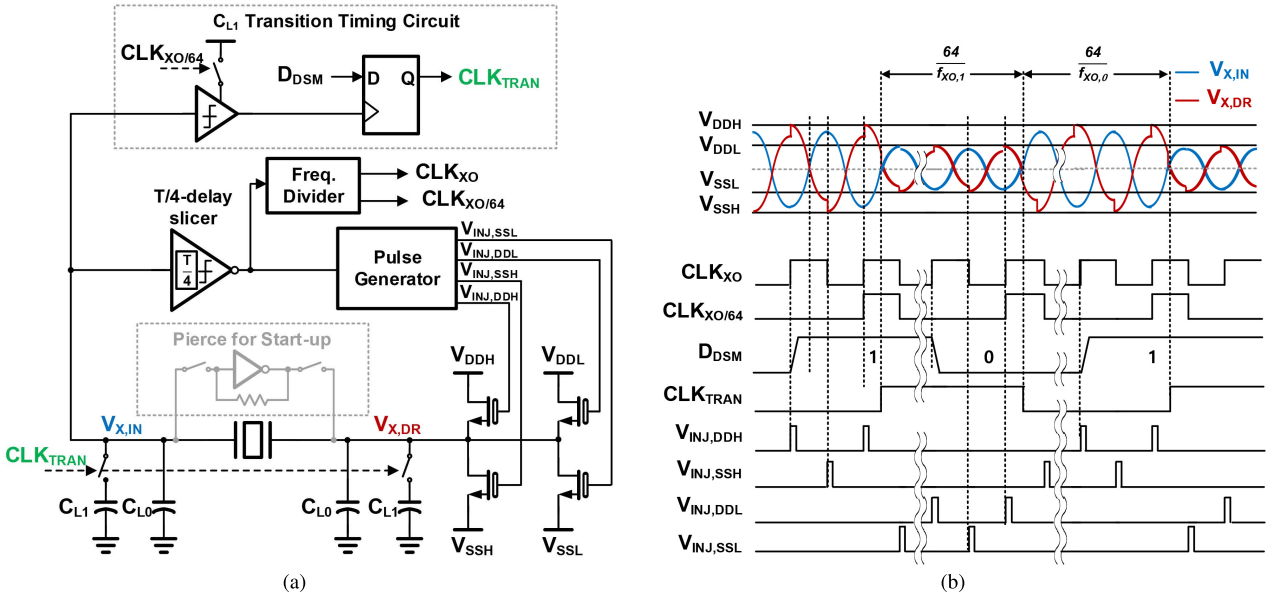

Fig. 9. Proposed pulsed-injection XO driver: (a) architecture and (b) timing diagram.

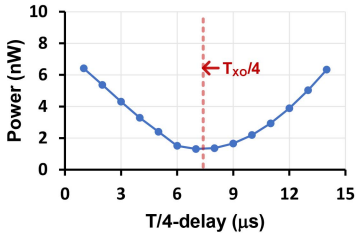

Fig. 10. Simulated power consumption of pulsed-injection switches according to the delay of the slicer.

valley of crystal oscillation to reduce phase error [1], [18]. In addition, the XO driver generates a reduced clock frequency ($CLK_{XO/64}$) for the other blocks to reduce energy and noise.

III. Pulsed-Injection XO Driver

A. Changes in XO Due to Different C_L

The proposed XO driver that includes two sets of pulsed-injection switch drivers with different supplies is shown in Fig. 7, which is designed to achieve high-energy efficiency. Although a single pulsed-injection switch driver can be used [1]–[4], [13], it causes a couple of issues. Since the output amplitude (V_{OSC}) of the XO changes according to C_L [2], there are two different oscillation amplitudes that the pulsed-injection switch driver must handle. If the driver uses only a single low supply voltage V_{DDL} and V_{SSL}, energy will be extracted from C_L when V_{OSC} is large (i.e., V_{OSC0}). This extraction of energy will cause the oscillation to rapidly diminish and waste energy. On the other hand, if the driver uses large supply (i.e., V_{DDH}, V_{SSH}), the large voltage drop between the supply voltage and V_{OSC1} leads to high regeneration energy, which in turn results in poor energy efficiency. Hence, instead of using a single pulsed-injection switch driver, we propose having two pulsed-injection switch drivers with different supplies. In detail, when $CLK_{TRAN} = 0$, one of the two drivers operates at V_{DDH} and V_{SSH}. When $CLK_{TRAN} = 1$, the other operates at V_{DDL} and V_{SSL}. Using this scheme, power consumption is significantly reduced.

When C_L changes, not only does the oscillation amplitude change but also the dc voltage of the oscillation can shift, which will cause an injection timing error. That is, when C_{L1} is connected to C_{L0}, there is charge sharing between the two capacitors, which sets the dc voltage. Since the initial voltage of C_{L1} is unknown, the dc voltage is also uncertain and can cause an injection timing error as shown in Fig. 8(a). To ensure a constant dc voltage, C_{L1} is precharged to half the supply as shown in Fig. 8(b).

B. Proposed XO Driver Architecture

Fig. 9 shows the complete schematic of the proposed XO driver and its timing diagram. It consists of a startup circuit, two pulsed-injection drivers, a T/4-delay clock slicer, a pulse generator, a frequency divider, and a C_{L1} transition timing circuit. The startup circuit is based on a Pierce XO and it is connected in parallel to the proposed driver and turned off when the XO has established its oscillation. The proposed pulsed-injection driver which is an all-nMOS single-ended driver, can reduce the power consumption compared to pMOS/nMOS complementary drivers [2]–[4], [13] or differential drivers [1] since it requires less injection pulses. Moreover, the single-ended driver reduces the injection timing error due to dc voltage fluctuation of $V_{X,IN}$ when a C_L value change occurs. We sized the pulsed-injection switches considering the on-resistance R_{ON}. When $T_{ON} < R_{ON} \cdot C_{eq,SW}$, the oscillation energy is not sufficiently replenished within T_{ON}, and thus the energy efficiency is degraded. To reduce R_{ON}, a large switch with a level-converted control signal is used. As a result, the proposed pulsed-injection driver has R_{ON} of 1.75 kΩ which is much smaller than T_{ON} of 1 μs when multiplied by $C_{eq,SW}$.

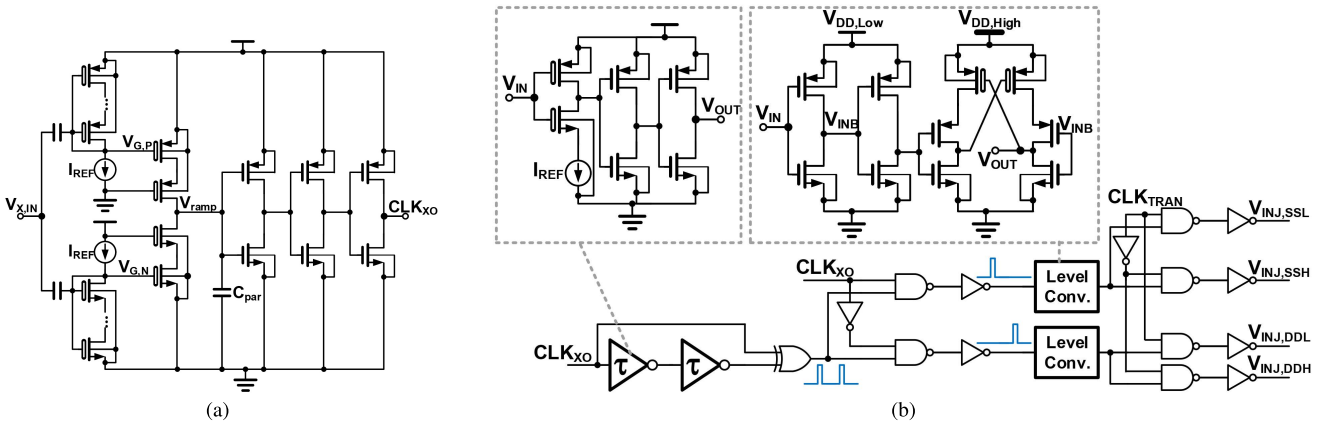

Fig. 11. Circuit schematic of (a) slicer, and (b) pulse generator with level converter.

For the pulsed-injection driver, a timing control circuit for the pulse injection at the peak and valley of the oscillation is needed, which requires an T/4-delay generation. Note that the accuracy of this delay affects the power consumption of the pulsed-injection driver since injection timing error will cause waste of regeneration power [18]. The simulated power consumption of pulsed-injection switches according to the delay are shown in Fig. 10 where it can be seen that deviation from $T_{XO}/4$ increases the power consumption. In [2], [3], and [13], T/4-delay is generated by a delay-locking loop (DLL) or a PLL which consumes large power and area. In [4], delay is generated in the slicer whose transistors are biased on the edge of conduction. Unfortunately, there is significant delay variation with change in PVT. To reduce the power consumption and variation of the T/4-delay, we employ the T/4-delay clock slicer [1], which performs zero-crossing detection and the T/4-delay generation to provide a proper pulse injection timing. To reduce the PVT variation of the delay, a cascode structure is employed. The circuit schematic of the slicer is shown in Fig. 11(a). Simulation results show that T/4-delay variation is within ±15% across PVT variation.

The schematic of the pulse generator with a level converter is shown in Fig. 11(b). Pulses are generated at the CLK_{XO} edge using a delay cell and XOR gate. The pulsewidth (T_{ON}) is designed considering the regeneration efficiency [2], which is optimum when T_{ON} is about 10% of T_{XO}. This is because larger T_{ON} improves the efficiency, but having too large T_{ON} degrades the efficiency as more energy is dissipated through the switches. In our design, we chose T_{ON} to be 1 μs (3.3% of T_{XO}) to have margin for PVT variation. The simulated T_{ON} varies from 1.7% to 8.3% of T_{XO} across PVT variation. The first stage of the delay cell is implemented using a current starving structure with I_{REF} to reduce delay variation. To lower R_{ON}, a level converter is used to up-convert the pulses to the high supply voltage $V_{DD,High}$. $V_{INJ,SSH}$ and $V_{INJ,SSL}$ have a pulse at the rising edge of CLK_{XO} depending on CLK_{TRAN}. $V_{INJ,DDH}$ and $V_{INJ,DDL}$ have a pulse at the falling edge of CLK_{XO} depending on CLK_{TRAN}.

A frequency divider generates a 1/64 duty-cycled clock $CLK_{XO/64}$ of 512 Hz. A C_L transition timing circuit which consists of the fast slicer and D-flip-flop is turned on only when $CLK_{XO/64}$ is high. Hence, the energy and noise from transitions are reduced by about 1/64. A folded cascode amplifier is used as the fast slicer to detect when $V_{X,IN}$ crosses 0°. The amplifier has a gain of 44 dB with a gain-bandwidth of 3.3 MHz and a power consumption of 15.2 nW, but the power consumption is reduced to 0.24 nW by duty cycling. The timing variation of the slicer is less than 0.5 μs across −40° to 85 °C. CLK_{TRAN} changes according to the output of $\Delta\Sigma$M when the fast slicer output changes.

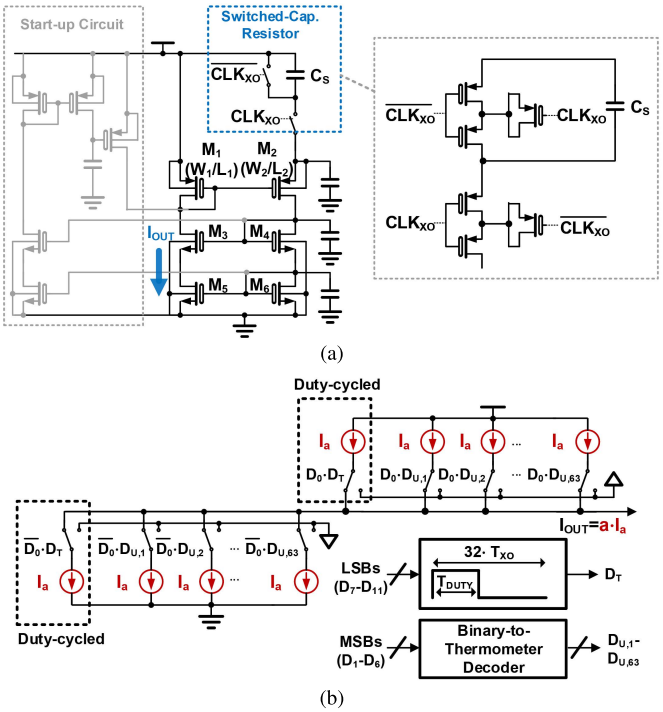

Fig. 12. Circuit schematic of (a) subthreshold current source, and (b) current-steering DAC.

IV. Implementation Details

A. Current-Steering DACs

The PWL function is realized with current-steering DACs with a unit current source I_a that is proportional to temperature

and I_b that is constant. Fig. 12(a) shows the schematic of the subthreshold current source I_a and I_b. Current I_{OUT} can be calculated using the following equation:

$$I_{\mathrm{OUT}} = \left\{ \left(V_{\mathrm{th},1} - V_{\mathrm{th},2}\right) + \frac{nkT}{q} \cdot \ln\left(\frac{W_2/L_2}{W_1/L_1}\right) \right\} \cdot f_{\mathrm{XO}} \cdot C_S \tag{5}$$

where $V_{\mathrm{th},1}$ and $V_{\mathrm{th},2}$ are the threshold voltages of M_1 and M_2, respectively, and (W_1/L_1) and (W_2/L_2) are the W/L ratios of M_1 and M_2, respectively. Since the threshold difference has a small temperature dependence, it can be seen that the temperature coefficient of the output current can be controlled by the size ratio $((W_2/L_2)/(W_1/L_1))$, and the temperature-independent part is related to the threshold voltages. For the PTAT current source I_a, M_1 and M_2 have the same threshold voltage and different W/L ratios, so the current can be expressed as follows:

$$I_a = \left\{ \frac{nkT}{q} \cdot \ln\left(\frac{W_2/L_2}{W_1/L_1}\right) \right\} \cdot f_{\mathrm{XO}} \cdot C_S. \tag{6}$$

We set W_2/L_2 as three times W_1/L_1, and C_S as 24 fF so that I_a is ~30 pA at 27 °C with a sensitivity of 0.11 pA/°C. On the other hand, for I_b, where M_1 and M_2 have the same W/L ratio and different threshold voltage by changing the channel length, the current can be expressed as follows:

$$I_b = \left(V_{\mathrm{th},1} - V_{\mathrm{th},2}\right) \cdot f_{\mathrm{XO}} \cdot C_S. \tag{7}$$

We set L_1 as 2.5 times L_2, and C_S as 24 fF so that I_b is ~40 pA. The temperature characteristics of I_a and I_b can be impacted by parasitic capacitance or process mismatch. However, the TCXO performance is not significantly affected since this variation was accounted for when calculating the coefficients a and b.

A switched capacitor resistor using C_S is used to achieve a large resistance (~1.3 GΩ) to reduce power consumption. Ultralow-leakage composite switches [4] are used to suppress the switching leakage by decreasing V_{DS} when switches are turned off. Also, dummy transistors are implemented to compensate for clock feedthrough. A cascode structure is used to improve the performance of the current mirror and pMOS devices are used for M_1 and M_2 to remove body effect.

A 12-bit current-steering DAC for the PWL function is shown in Fig. 12(b), where direction of the current is determined by the signs of a and b. For the 6-bit MSB, 63 thermometer coded current sources are used to improve linearity. For the 5-bit LSB, a duty-cycled current source is used where it is turned on from a single period of XO (i.e., T_{XO}) to $31 \cdot T_{\mathrm{XO}}$, resulting in a duty cycle of 1/32–31/32. As a result, the total charge from the DAC during one integration period (i.e., $32 \cdot T_{\mathrm{XO}}$) of ΔΣM can be expressed as

$$\begin{aligned} \Delta Q = D_0 \cdot \big\{ &\left(D_1 \cdot 2^5 + \cdots + D_6 \cdot 2^0\right) \cdot I_{\mathrm{LSB}} \cdot 32T_{\mathrm{XO}} \\ &+ I_{\mathrm{LSB}} \cdot \left(D_7 \cdot 2^4 + \ldots D_{11} \cdot 2^0\right) \cdot T_{\mathrm{XO}} \big\} \end{aligned} \tag{8}$$

where D_0 is the sign bit, $D_1 - D_6$ is the MSB and $D_7 - D_{11}$ is the LSB.

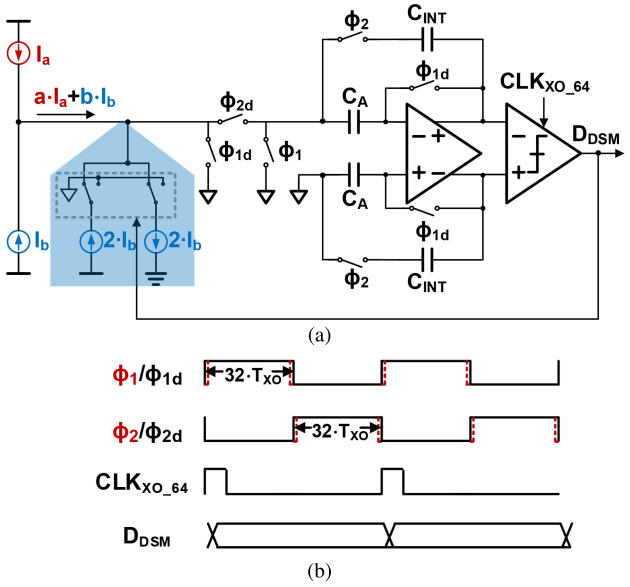

Fig. 13. Single-bit 1st-order ΔΣM: (a) circuit schematic, and (b) timing diagram.

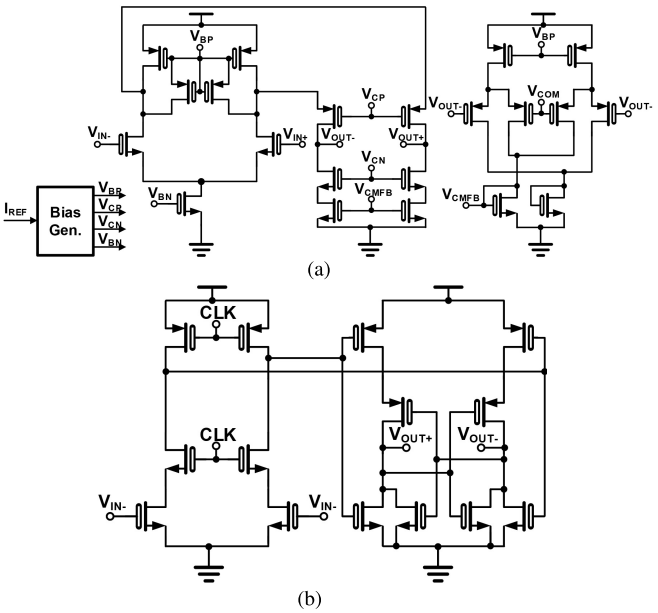

Fig. 14. Circuit schematic of (a) amplifier, and (b) clocked comparator of ΔΣM.

B. Single-Bit 1st-Order ΔΣM

Fig. 13(a) shows the circuit schematic of the 1st-order ΔΣM which produces a single-bit stream with the desired bit density $\widehat{\mu}(T)$. The associated timing diagram is shown in Fig. 13(b), where ϕ_1, ϕ_{1d}, ϕ_2, and ϕ_{2d} are non-overlapping clocks with a frequency of $f_{\mathrm{XO}}/64$ for bottom plate sampling [19]. The combined current, $a \cdot I_a + b \cdot I_b$, is accumulated on the integrator capacitor (C_{INT}) during ϕ_2 which has a period of $32 \cdot T_{\mathrm{XO}}$. The 1-bit feedback DAC is consists of a current $2 \cdot I_b$. Therefore, the bit density μ_{DSM} of the bitstream D_{DSM} ($0 \leq \mu_{\mathrm{DSM}} \leq 1$)

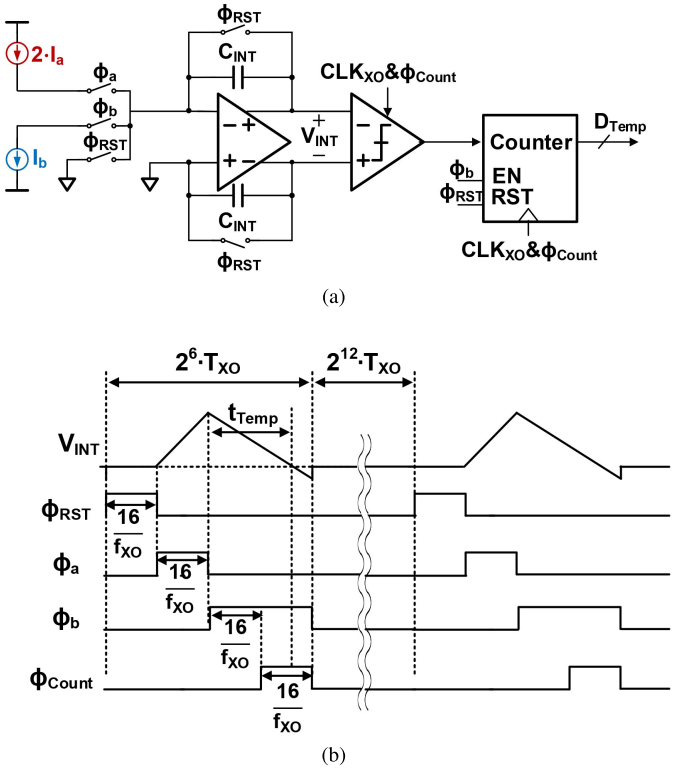

Fig. 15. Coarse temperature sensor using dual-slope conversion: (a) circuit schematic, and (b) timing diagram.

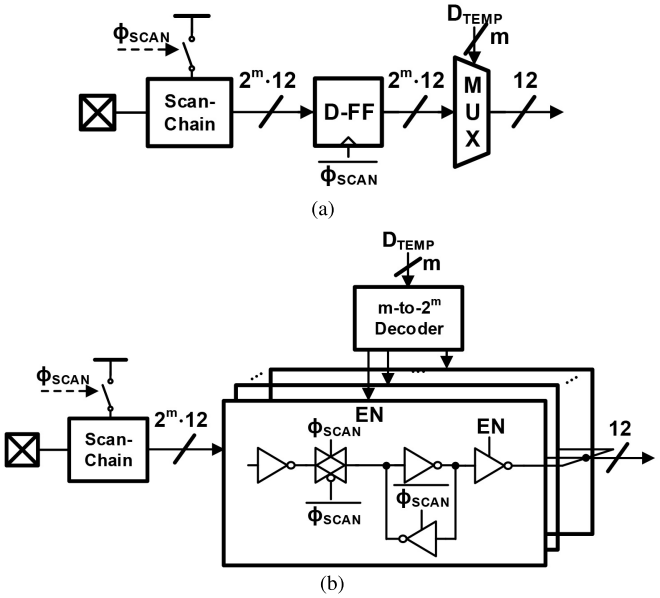

Fig. 16. Block diagram of (a) conventional LUT, and (b) proposed low power LUT.

can be expressed as follows:

$$\mu_{\mathrm{DSM}} = \frac{a \cdot I_a + b \cdot I_b}{4 \cdot I_b} + \frac{1}{2} \tag{9}$$

where can be seen that μ_{DSM} is proportional to $a \cdot (I_a/I_b) + b$.

For the integrator, the error at the virtual ground node of the amplifier due to offset, flicker noise, and finite dc gain is an important issue. To reduce the error due to offset and flicker noise, auto-zeroing using C_{A} is adopted. In addition, to address the error due to finite dc gain, as shown in Fig. 14(a), a folded cascode amplifier is used, which achieves a high gain of 95 dB under TT at 25 °C. In addition, an output CMFB circuit is implemented using a differential-difference amplifier structure for high impedance. The folded cascode amplifier which includes the CMFB and a biasing circuit has a power consumption of 7 nW, gain-bandwidth of 6.5 kHz with a load capacitance of 2 pF. For the comparator, a double latched structure [20] is employed to save power, and the input transistor is moved to the bottom to reduce kick-back noise as shown in Fig. 14(b).

We chose a 1st-order $\Delta\Sigma$M because it can achieve sufficient SNR to make frequency error caused by $\Delta\Sigma$M below 1 ppm. T_{XO} with the $\Delta\Sigma$M noise (μ_{noise}) can be expressed as the following equation:

$$T_{\mathrm{XO}} = (\mu + \mu_{\mathrm{noise}}) \cdot \left(\frac{1}{f_1} - \frac{1}{f_0}\right) + \frac{1}{f_0}. \tag{10}$$

To make frequency error caused by μ_{noise} below 1 ppm, μ_{noise} should be below 0.0081, which corresponds to SNR > 42 dB. In a conversion time of 1 s (OSR of 512), the 1st-order $\Delta\Sigma$M can achieve an SNR of about 70 dB which corresponds to a frequency error of less than 0.1 ppm. In addition, 1st-order $\Delta\Sigma$M uses fewer amplifiers and simplifies the design compared to a higher order $\Delta\Sigma$M.

C. Coarse Temperature Sensor

A coarse temperature sensor divides the temperature range and selects the PWL segment. Fig. 15 shows the circuit schematic and timing diagram of the temperature sensor. It is implemented using a 4-bit dual slope conversion architecture that reuses I_a and I_b. Dual-slope conversion has the advantage that it is immune to circuit parameter variation such as C_{INT} since such variation affects the up and down conversion in the same way. The conversion takes 2^6 cycles of f_{XO} (~2 ms) and it is performed only once every 2^{12} cycles of f_{XO} (~125 ms) to reduce power consumption.

The operation consists of four phases: $\phi_{\mathrm{RST}}, \phi_a, \phi_b$ and ϕ_{Count}. During ϕ_{RST}, it finds the bias point using unity-gain feedback. During the next phase, ϕ_a, $2 \cdot I_a$ is integrated to C_{INT} for $16 \cdot T_{\mathrm{XO}}$, and then during ϕ_b, I_b is integrated in the opposite direction to C_{INT}. The time t_{temp} for which V_{INT} takes to reach zero can be calculated as follows:

$$t_{\mathrm{temp}} = \frac{2 \cdot I_a}{I_b} \cdot 16 \cdot T_{\mathrm{XO}}. \tag{11}$$

As I_a is proportional to temperature and I_b is temperature-independent, t_{temp} is proportional to temperature. During ϕ_{Count}, which starts 16 cycles after ϕ_b starts, the counter measures the time until V_{INT} becomes zero. As a result, D_{Temp} changes from 2 to 12 between −40 °C to 85 °C with an interval of about 13°.

D. Digital Circuits

The LUT stores 2^4 pairs of PWL parameters which determined the coefficients (a, b) of the 12-bit current DACs.

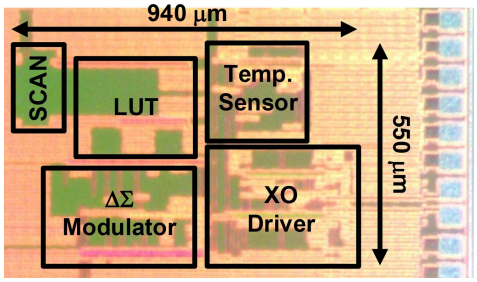

Fig. 17. Die photograph.

The required (a, b) pairs are calculated off-chip and passed to the chip through a scan-chain, and stored in the LUT. Fig. 16(a) shows a conventional LUT which stores 192 (a, b) pairs in D flip-flops and selects (a, b) through the multiplexer according to D_{Temp}. Although the LUT is digital logic which does not dissipate power when inactive, its leakage power can be significant. Simulation shows that a flip-flop consumes 65 pW of leakage power at 85 °C and the conventional LUT implemented using flip-flops consumes 32 nW which is much larger than other parts of the XO. To save power consumption we used a transmission gate and latch instead of flip-flops. In addition, the multiplexer is replaced by tri-state buffers and a 4-to-2^4 decoder as shown in Fig. 16(b). Note that these are static circuits and thus leakage does not affect the stored value even if there is a slow clock or temperature drift. The stored value is changed only when the LUT is updated by Scan-chain ($\phi_{\text{SCAN}} = 1$). One cell including a transmission gate, a latch, and a tri-state buffer consumes about 3.7 pW when V_{DD} is 0.45 V at 85 °C in simulation. As a result, the proposed LUT consumes 6.8 nW at 85 °C which is a 4.5× power reduction at 85 °C.

V. Measurement Results

A prototype chip was implemented in a 40-nm CMOS process. The chip micrograph is shown in Fig. 17 and the area of the chip is 0.517 mm^2. The fabricated chip is mounted on a PCB and directly wire-bonded without any package. The chip is connected to an SMD type crystal (ECX-34Q-S [21]). Both C_{L0} and C_{L1} are implemented using an on-chip metal-oxide-metal (MOM) capacitor with a value of 2.5 pF. A 0.9-V supply is used for the temperature sensor, the ΔΣM, and the XO driver, and a 0.45-V supply is used for the LUT and the XO driver. Four supply voltages used for the dual pulsed-injection driver are $V_{\text{DDH}} = 300$ mV, $V_{\text{SSH}} = 0$ V, $V_{\text{DDL}} = 225$ mV, $V_{\text{SSL}} = 75$ mV and they are provided from off-chip. Note that these supplies are multiples of 75 mV so that they can be implemented on-chip in the future work using a simple switched capacitor ladder-topology from a single supply voltage [2]. Such implementation consumes several nWs to make three pairs of supply voltages and hence we expect that adding an on-chip voltage generator for the proposed TCXO will add less than 10 nW. The measured frequency errors over variations in power supplies are shown in Fig. 18(a)–(d). For each graph, one supply voltage is changed while others are kept constant. It can be seen that the frequency

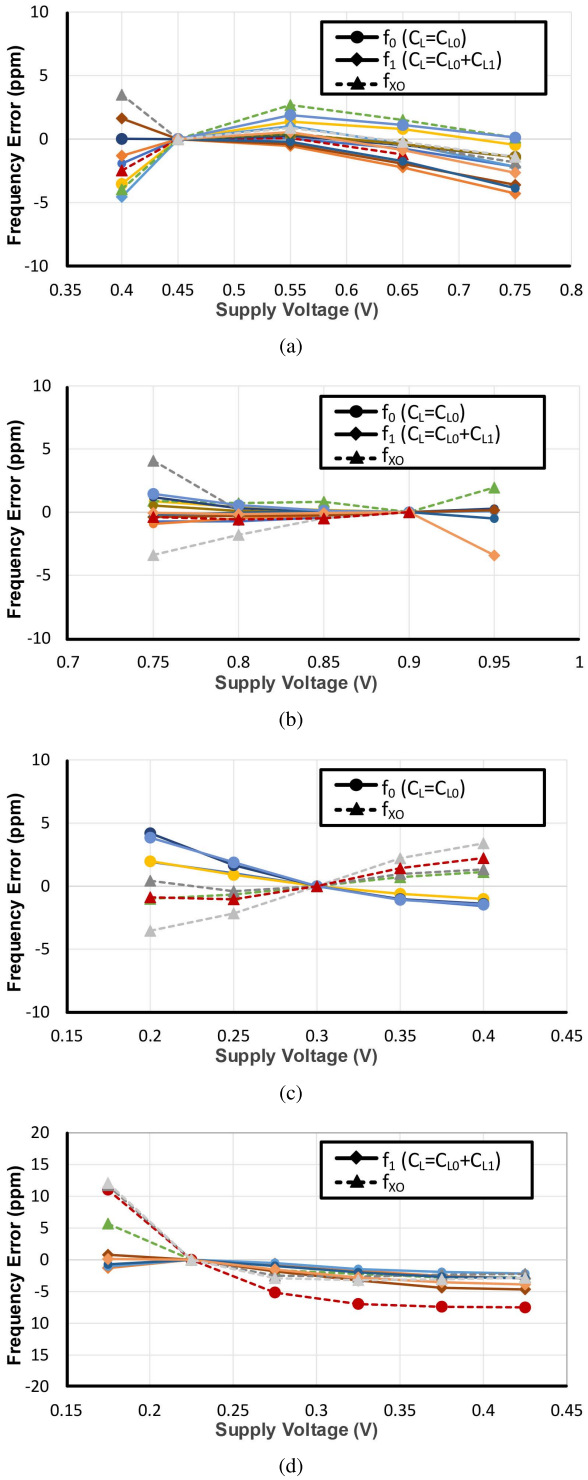

Fig. 18. Measured frequency error for four chips when power supplies are changed. (a) 0.45-V supply for LUT and XO driver. (b) 0.9-V supply for temperature sensor, the ΔΣM, and XO driver. (c) Power supply for C_{L0} driver (V_{DDH}). (d) Power supply for $C_{L0} + C_{L1}$ driver (V_{DDL}).

error is within 5 ppm for all supplies except for V_{DDL}, which results in about 12 ppm across 0.175–0.425 V.

The proposed TCXO consumes 43 and 67 nW at 25 °C and 85 °C, respectively. The measured power breakdown is shown in Fig. 19, where it can be seen that the ΔΣM and

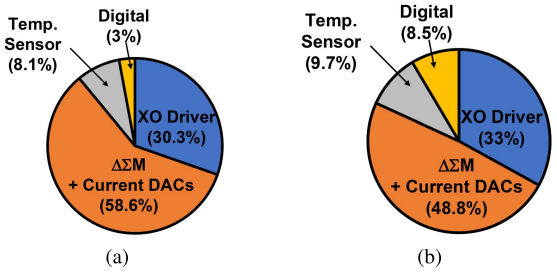

Fig. 19. Measured power breakdown at (a) 25 °C and (b) 85 °C.

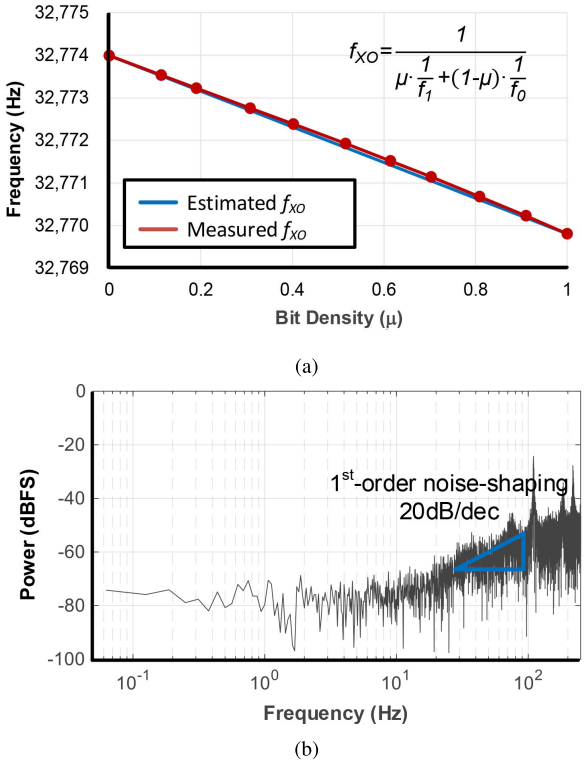

Fig. 20. Measurement results of 1st-order ΔΣM: (a) f_{XO} versus μ of ΔΣM, and (b) 2^{14}-point FFT.

current DACs dominate the power consumption. Since the amplifier of the ΔΣM uses a bias current that is constant over temperature, the power consumption of the ΔΣM does not increase significantly with temperature. Digital circuits, including the LUT, consume 4.4 times more power at 85 °C than at 25 °C.

To test the performance of the C_L modulation by the ΔΣM, μ_{DSM} was swept from 0 to 1 at 25 °C by changing coefficient a with a fixed coefficient b. The measured f_{XO} is shown in Fig. 20(a) which shows that f_{XO} decreases with μ_{DSM} as estimated by (1). Fig. 20(b) shows the measured 2^{14}-point FFT plot of the proposed ΔΣM, demonstrating the 1st-order noise shaping. The FFT is obtained with a sampling clock of 512 Hz (f_{XO}/64) and applying a dc-input. In a conversion time of 1 s (OSR of 512), the ΔΣM achieves an rms resolution of 11 bit which corresponds to a frequency error of less than 0.1 ppm.

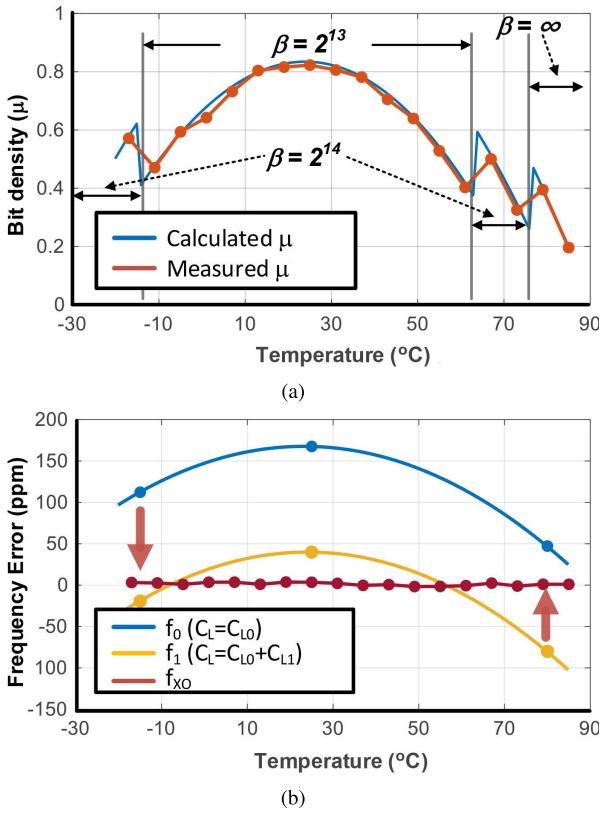

Fig. 21. Measured (a) bit density of ΔΣM (μ_{DSM}) and (b) frequency error of f_0, f_1, and f_{XO}.

To determine the coefficients (a, b) for the LUT, the following method was used.

1) To find the temperature characteristic of the XO, we measure f_0 and f_1 at three temperature points to derive $f_0(T)$ and $f_1(T)$, which is needed to find the parameters of the tuning fork's quadratic function.
2) We compute the required μ using (2), and calculate the PWL $\widehat{\mu}(T)$, while adding ±3 °C margin at the end of each segment to relax the accuracy requirement of the temperature sensor. Since the ΔΣM works properly when $0.1 < \mu_{DSM} < 0.9$, we add an offset to μ if the required μ is less than 0.1 or greater than 0.9. To add an offset to μ, a pulse-swallowing method is used, which removes one pulse every β cycles. Then, the required μ changes as follows:

$$\mu(T) = \frac{\frac{1}{f_{avg}} - \frac{1}{f_0(T)}}{\frac{1}{f_1(T)} - \frac{1}{f_0(T)}} - \frac{1}{\beta} \cdot \frac{\frac{1}{f_{0,25\,°C}}}{\frac{1}{f_{1,25\,°C}} - \frac{1}{f_{0,25\,°C}}}. \quad (12)$$

3) We determine the linear temperature transfer functions of $\mu(I_a)$ and $\mu(I_b)$ by measuring μ when inputs of the ΔΣM are I_a and I_b, respectively, at two temperature points. Note that these temperature points can be the same as the ones used for XO characterization.
4) We calculate the coefficients (a, b) for the LUT to obtain $\widehat{\mu}(T) = a \cdot \mu(I_a) + b \cdot \mu(I_b)$.

Fig. 21 shows the measured μ_{DSM} and frequency errors of f_0, f_1, and f_{XO} for one chip from −20 °C to 85 °C. The target

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH LOW-POWER STATE-OF-THE-ART TCXOS

	This work	S.Zaliasl, JSSC 15	D. Ruffieux ISSCC 16	P. Park, JSSC 15	D. Ruffieux, JSSC 14	J. Gronicz, ISCAS 14	D. Ruffieux, JSSC 10
Process	**40nm**	180nm	350nm	180nm	180nm	180nm	180nm
Resonator Type	**XTAL**	MEMS	XTAL	XTAL	XTAL	MEMS	Silicon
Operating Temp. (°C)	**-20 to 85**	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85	0 to 50
Power (nW)	**43.4@25°C 67.1@85°C**	1500	360	N.A.	400	3600	3200
Freq. Stability (Trim. Method)	**± 4ppm (3-point)**	± 3ppm (5-point)	± 3ppm (3-point)	± 2ppm (3-point)	± 2ppm (5-point)	± 4ppm (3-point)	± 10ppm (3-point)
Allan Dev. (ppb)	**< 34**	N.A.	~ 10	N.A.	~10	N.A.	N.A.
IC Area (mm^2)	**0.517**	0.8	1.296	0.119	N.A.	1.14	0.126
Output Freq. (kHz)	**32.768**	32.768	32.768	32.768	32.768	27	32.768

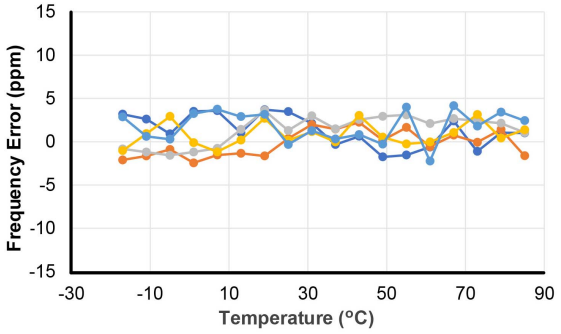

Fig. 22. Measured frequency error of five chips.

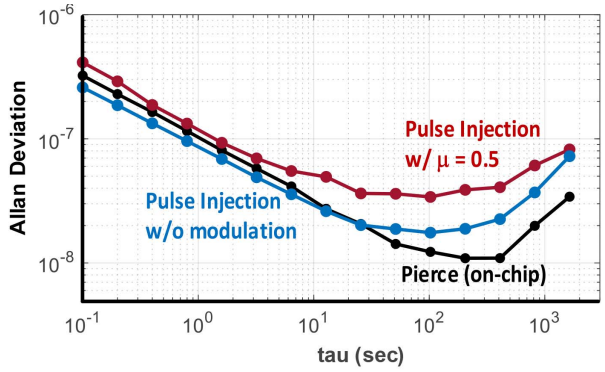

Fig. 23. Measured Allan deviation.

frequency is 32.768 kHz. As shown in the frequency error graph, the proposed TCXO achieves much lower frequency error than f_0 and f_1. The measured frequency errors over −20 °C–85 °C for five chips are shown in Fig. 22. The chips are trimmed individually, and they achieve a frequency error of ±4.16 ppm. It is noted that the pulse-swallowing changes f_{XO} to $f_{XO} \cdot \beta/(1+\beta)$, so the measured f_{XO} is less than both f_0 and f_1 for some temperature region. By adding an offset to f_{XO}, the required C_{L1} is reduced, which saves the power consumption of XO.

Fig. 23 is the measured Allan deviation operating at room temperature during 2 h. Allan deviation confirms the long-term frequency stability of the proposed oscillator. The black line is the conventional Pierce XO used in the startup circuit, but not turned-off after startup. The blue line is the proposed XO without C_L modulation, and the red line shows the proposed XO when μ_{DSM} is 0.5. When enabling the ΔΣM, the long-term stability deteriorates. When ΔΣM is enabled, the noise due to clock feedthrough and charge injection is generated at the switches between C_{L1} and XO. The noise injected into the XO is proportional to the number of switching [1]. Therefore, the Allan deviation is the worst when μ_{DSM} is 0.5 because the C_L transition occurs most frequently. In the worst case, the Allan deviation floor is measured to be 34 ppb, which is about twice as large as the Allan deviation floor when disabling ΔΣM.

The performance of the TCXO is summarized in Table I and compared to other state-of-the-art low power TCXOs. As can be seen, the proposed work achieves the lowest power consumption with an approximate 8× reduction compared to prior state-of-the-art TCXOs, while maintaining an accuracy within ±5 ppm across temperature. If the proposed work uses inexpensive process such as 180 nm which is used in other previous works, power consumption will increase by about 1.3 times due to the increase in supply voltage.

VI. CONCLUSION

In this article, the lowest power 32.768-kHz TCXO with a pulse-injection XO driver was presented. The proposed TCXO achieves an accuracy of ±4.2 ppm from −20 °C to 85 °C with three-point trimming and an Allan deviation floor of 34 ppb while consuming 43 nW at room temperature which is 8× lower than the prior work. Temperature compensation is achieved with a single-bit switched C_L which is modulated by a 1st-order ΔΣM. To reduce the cost, complexity and power consumption, the ΔΣM digitizes a PWL approximation of μ required to make XO frequency constant over temperature. The correct PWL segment for the temperature is selected by a coarse dual-slope-based temperature sensor. For high-energy efficiency of the XO, a pulsed-injection XO driver is implemented, which was designed to accommodate the differing amplitudes of the two states of C_L.

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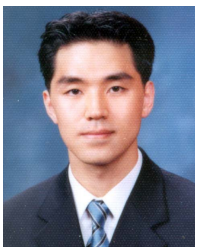

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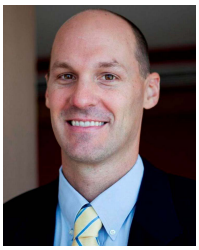

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He held research staff positions at Synopsys, Mountain View, CA, USA, and Hewlett-Packard Laboratories, Palo Alto, CA, USA; and visiting professorships at the National University of Singapore, Singapore, and Nanyang Technological University, Singapore. He is currently the Edward S. Davidson Collegiate Professor of electrical and computer engineering with the University of Michigan, Ann Arbor, MI, USA. His research interests include the design of miniaturized ultralow power microsystems, touching on analog, mixed-signal, and digital circuits. He has published over 500 articles and holds more than 50 U.S. patents in these areas. His research has been commercialized via three major venture capital-funded startup companies: Ambiq Micro, Cubeworks, and Mythic.

Dr. Sylvester is also a member of the Administrative Committee for IEEE Solid-State Circuits Society. He was an IEEE Solid-State Circuits Society Distinguished Lecturer. He received 14 best paper awards and nominations and was named a Top Contributing Author at ISSCC and most prolific author at IEEE Symposium on Very Large Scale Integration (VLSI) Circuits. He is also an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS.

David Blaauw (Fellow, IEEE) received the B.S. degree in physics and computer science from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 1991.

Until August 2001, he worked with Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology group and won the Motorola Innovation Award. Since August 2001, he has been the Faculty Member with the University of Michigan, Ann Arbor, MI, USA, where he is currently the Kensall D. Wise Collegiate Professor with electrical engineering and computer science (EECS). He is also the Director of the Michigan Integrated Circuits Laboratory, Ann Arbor. He has published over 600 articles and holds 65 patents. He has researched on ultralow-power wireless sensors using subthreshold operation and low-power analog circuit techniques for millimeter systems. This research was awarded the MIT Technology Review's "one of the year's most significant innovations." His research group introduced the so-called near-threshold computing, which has become a common concept in semiconductor design. Most recently, he has pursued research in cognitive computing using analog, in-memory neural networks for edge devices, and genomics for precision health.

Dr. Blaauw received numerous best paper awards. He also received the 2016 SIA-SRC Faculty Award for Lifetime Research Contributions to the U.S. Semiconductor Industry. He was the General Chair of the IEEE International Symposium on Low Power and a member of the IEEE International Solid-State Circuits Conference (ISSCC) analog program subcommittee.