A 43nW 32kHz Pulsed Injection TCXO with ±4.2ppm Accuracy Using ΔΣ Modulated Load Capacitance

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Abstract

This paper presents an ultra-low power temperature-compensated crystal oscillator (TCXO) with a pulsed injection XO driver for IoT applications. Temperature compensation is achieved using a single switched load capacitance, modulated by a ΔΣM. The ΔΣM digitizes a piece-wise linear (PWL) approximation of the XO temperature dependence where a coarse 4-bit temperature sensor selects the PWL segment. The proposed 32.768kHz TCXO achieves an accuracy of ±4.2ppm from -20℃ to 85℃ with 3-point trimming and Allan deviation floor of 34 ppb while consuming 43nW.

Introduction

A real time clock (RTC) is essential in battery-operated IoT sensors as they cannot afford to keep time through frequent communication with devices with accurate time references. Since an RTC is always on, its power consumption must be much lower than other components that can be duty cycled. Moreover, timing uncertainty yields longer radio on-time during synchronization, incurring high energy penalties [1] and hence, RTC accuracy must be high. To meet these needs, a number of ultra-low power (ULP) 32kHz oscillators have been proposed [1-6]. In [1-3], sub-10nW oscillators are introduced using a pulsed-injection driver that directly replenish energy of the XO load capacitors. Unfortunately, their frequency accuracy across temperature is more than 100ppm. In [4-6], temperature compensated XOs and MEMS oscillators with frequency error of less than ±5ppm were introduced, but these approaches consume more than 300nW. In this paper, we propose a pulsed injection TCXO with a single-bit load capacitance driven by a ΔΣ modulation (ΔΣM) digitizing a PWL current source, achieving ±4ppm frequency accuracy and consuming only 43 nW.

Proposed Architecture

The concept of the proposed TCXO exploits the fact that different XO load capacitances (C_0, C_1) generate different frequencies (f_0, f_1) (Fig. 1). Hence, we can obtain a constant output frequency over temperature if these two frequencies are appropriately weighted and summed in time, similar to the divider driven by a ΔΣM in a fractional-N PLL. That is, connecting C_1 and C_0 to the XO for the ratio of μ : (1-μ) results in a period of $1/f_{avg} = \mu/f_1 + (1-\mu)/f_0$. To ensure constant f_{avg} over temperature, μ must follow the temperature characteristics of the XO, which is a high-order function (Fig. 1). To avoid the cost and complexity of accurately implementing this function on-chip, we instead approximate it with an n-segment PWL function. We achieve frequency error of less than ±5ppm across −20 to 85℃ with n = 8.

The overall architecture (Fig. 2) includes a coarse temperature sensor that selects the appropriate PWL segment to match the higher order XO frequency function. PWL parameters are stored in an n-entry LUT as coefficients (*a,b*) where *a* sets the magnitude of a current-steering DAC with unit current I_a that is temperature-proportional and *b* sets the magnitude of a DAC with unit current I_b which is temperature-independent. The combined current of $a \cdot I_a + b \cdot I_b$ is then digitized by a ΔΣM such that its output, D_{DSM}, has a bit density of μ over temperature. The D_{DSM} then controls the single-bit XO load capacitance (C_{L1}), thereby compensating f_{TCXO} over temperature. To improve the range of the ΔΣM, we add an offset to μ by removing one pulse every β cycles.

The advantage of the approach is that, unlike conventional TCXOs, temperature is never explicitly determined or used to index a large LUT modulating a fine-grain CDAC connected to the XO. Instead, only n PWL parameters are stored, which are directly converted by the ΔΣM to the single bit XO load capacitance modulation.

Fig. 3 shows the circuit implementation. A Pierce XO provides startup. The T/4-delay clock slicer performs both zero-crossing detection and the T/4-delay generation for proper pulse injection at peak and the valleys of the XO oscillation. Since the XO amplitude is inversely proportional to $\sqrt{C_m \parallel (C_p + C_L/2)}$, it changes with the D_{DSM} value. Hence, D_{DSM} selects between two drivers operating at V_{DDH} & V_{SSH} when D_{DSM}=0 and V_{DDL} & V_{SSL} when D_{DSM}=1. To ensure a constant DC voltage which is necessary for proper slicer operation, D_{DSM} is synchronized to the XO oscillation and transitions when $V_{X,IN}$ is at 0° or 180° degrees. To reduce injection timing error, pulse injection is performed only one-sided at $V_{X,DR}$ instead of two-sided as in [1,3]. By using a 1/64 duty-cycled clock (Fig. 5), the energy and noise from transitions are greatly reduced.

Fig. 4 shows the single-bit 1st-order ΔΣM architecture. The current, $a \cdot I_a + b \cdot I_b$, is accumulated on C_{INT} during ϕ_2 with a period of $32/f_{TCXO}$. Auto-zeroing reduces offset and flicker noise, and a clocked dynamic comparator saves power consumption. The sign of coefficients (*a,b*) determines the current direction, the MSBs set the number of current sources (thermometer code), while the LSBs modulate the duty cycle of a single unit current for fine-grain control. The unit currents, I_a and I_b, are set by the threshold voltages and W/L ratios of M_1 and M_2 (Fig. 6). PMOS transistors are used to remove body effect and a switched-capacitor resistance generates a large resistance (~1.3GΩ) to reduce power.

The temperature sensor that indexes the LUT is built around a 4-bit dual-slope temperature sensor and reuses I_a and I_b (Fig. 7). The conversion takes ~2ms ($2^6/f_{TCXO}$) and is performed only once every 125ms ($2^{12}/f_{TCXO}$), reducing power consumption. The LUT uses latches and tristate buffers instead of flip-flops which saves about 4.5× power (simulation).

The trimming process is performed as follows: (1) We measure XO frequency at 3 temperature points, which is sufficient to characterize the frequency of a tuning fork XTAL. (2) We automatically compute the PWL approximation of μ, adding ±3℃ margin beyond the end of each segment to relax the accuracy requirement of the temperature sensor. (3) We determine the linear temperature transfer functions of $\mu(I_a)$ and $\mu(I_b)$ by measuring μ when inputs of the ΔΣM are I_a and I_b, respectively, at 2 temperature points (can be combined with XO characterization temperatures). (4) We calculate the coefficients (*a,b*) for the LUT to obtain $\mu = a \cdot \mu(I_a) + b \cdot \mu(I_b)$.

Experimental Results

The proposed TCXO was fabricated in 40nm CMOS with an area of 0.517mm^2 (Fig. 14 shows the chip micrograph). Fig. 8 shows the measured $f_{XO,0}$, $f_{XO,1}$, bit density, and frequency error for one chip (ECX-34Q-S XTAL) over −20℃ to 85℃. The measured frequency error of 5 chips is less than ±4.16ppm with 3-point trimming (Fig. 11). The TCXO consumes 43nW and 67nW at 25℃ and 85℃, respectively. Fig. 12 provides the power breakdown at 25℃. The worst-case Allan deviation floor (Fig. 9) is measured to be 34ppb when μ=0.5 (C_{L1} switches most frequently). Fig. 10 also shows measured frequency across μ at 25℃. Table I provides a comparison with other low-power TCXOs. The proposed work achieves the lowest power consumption, which is ~8× lower than prior state-of-the-art TCXOs, while maintaining an accuracy within ±5ppm across temperature.

Acknowledgment

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References

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[2] L. Xu, *ISSCC*, 2020
[3] K-J. Hsiao, *ISSCC*, 2014
[4] S. Zaliasl, *JSSC*, 2015
[5] D. Ruffieux, *ISSCC*, 2014
[6] P. Park, *JSSC*, 2015

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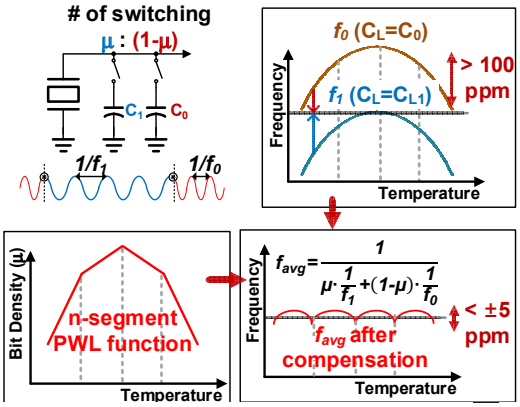

Fig. 1. Concept of the proposed TCXO

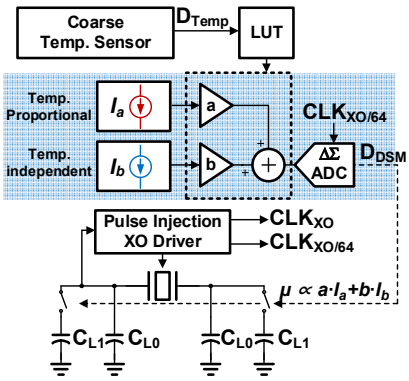

Fig. 2. Block diagram of the proposed TCXO

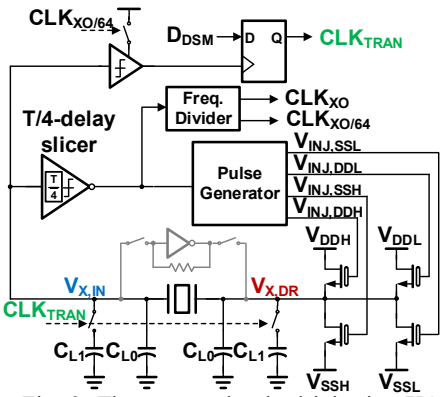

Fig. 3. The proposed pulsed injection XO driver architecture

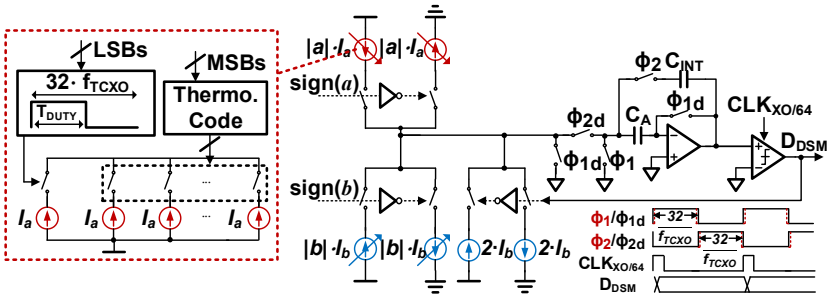

Fig. 4. The single-bit 1st-order ΔΣ TDC architecture

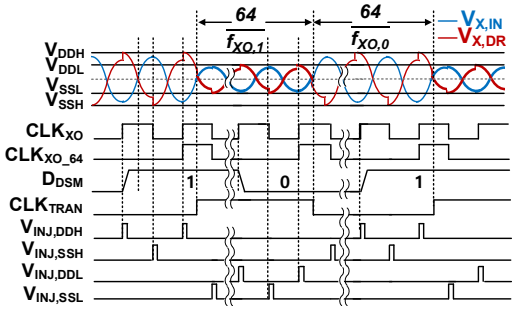

Fig. 5. The oscillation waveform of the XO

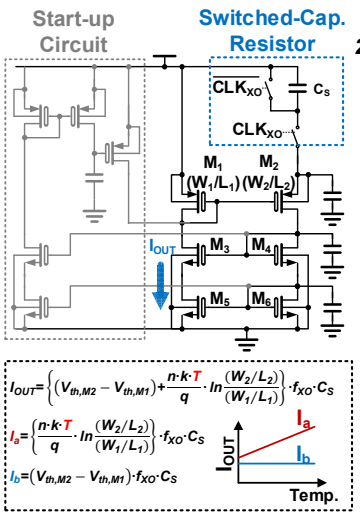

Fig. 6. Circuit schematic of I_a and I_b

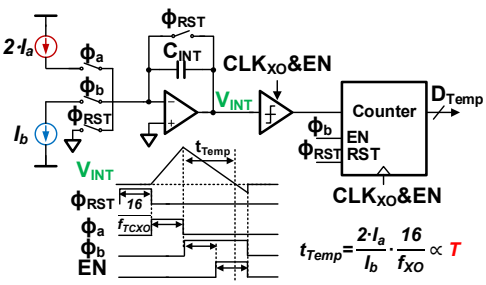

Fig. 7. Dual-slope temperature sensor

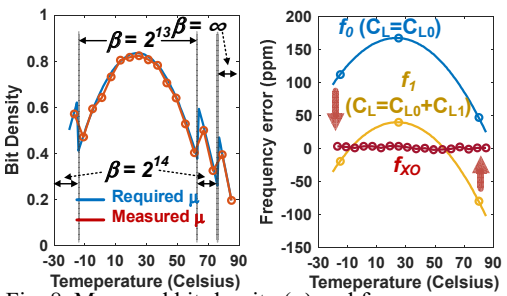

Fig. 8. Measured bit-density (μ) and freq. error

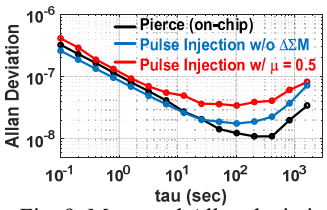

Fig. 9. Measured Allan deviation

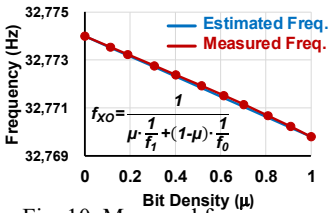

Fig. 10. Measured freq. vs. μ

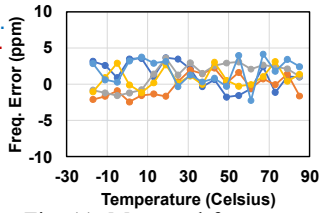

Fig. 11. Measured freq. error of 5 chips

	This work	[4] JSSC 15	[5] ISSCC 16	[6] JSSC 15	D. Ruffieux, JSSC 14	J. Gronicz, ISCAS 14	D. Ruffieux, JSSC 10
Process	**40nm**	180nm	350nm	180nm	180nm	180nm	180nm
Resonator Type	**XTAL**	MEMS	XTAL	XTAL	XTAL	MEMS	Silicon
Operating Temp. (°C)	**-20 to 85***	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85	0 to 50
Power (nW)	**43.4@25°C 67.1@85°C**	1500	360	N.A.	400	3600	3200
Freq. Stability (Trim. Method)	**± 4ppm (3-point)**	± 3ppm (5-point)	± 3ppm (3-point)	± 2ppm (3-point)	± 2ppm (5-point)	± 4ppm (3-point)	± 10ppm (3-point)
IC Area (mm^2)	**0.517**	0.8	1.296	0.119	N.A.	1.14	0.126
Output Freq. (kHz)	**32.768**	32.768	32.768	32.768	32.768	27	32.768

* The temperature range is limited by the equipment set-up

Table I. Performance summary and comparison

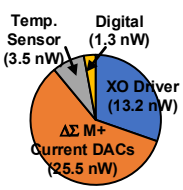

Fig. 12. Measured power breakdown

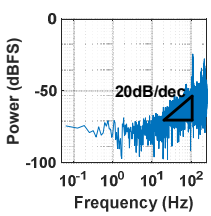

Fig. 13. Measured 2^{14}-point FFT of ΔΣM

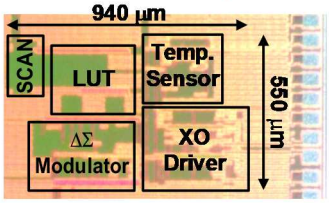

Fig. 14. 40nm die photograph

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