# A Fully Integrated, Automatically Generated DC–DC Converter Maintaining >75% Efficiency From 398 K Down to 23 K Across Wide Load Ranges in 12-nm FinFET

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***Abstract*—This letter presents a fully integrated recursive successive-approximation switched capacitor (RSC) DC–DC converter implemented using an automatic cell-based layout generation in 12-nm FinFET technology. A novel design methodology is demonstrated based on the theoretical analyses of the optimal energy operation of the switched-capacitor (SC) DC–DC converter and directly finds the optimal design parameters from the given input specifications. The converter maintains >75% efficiency across a vast range of output currents and temperatures. Our design targets voltage scaling for applications, such as cryo-computing, cryo-sensing, and parts of quantum computing, to achieve high-system power efficiency.**

***Index Terms*—Cryogenic, DC–DC, switched-capacitor (SC), wide temperature.**

## I. Introduction

There has been a renewed interest in utilizing cryogenic CMOS electronics to realize performance enhancements in various applications, including high-performance computing [1], [2], qubit systems [3], sensors, superconductivity, and other low-temperature applications in sectors, such as those found in aerospace [4]. Fig. 1 summarizes practical applications that require operation from normal conditions down to cryogenic temperatures and would benefit from cryogenic CMOS design techniques. To satisfy the low-thermal limit of dilution refrigerators, improved power efficiency is required for circuit components located within the cooling chamber as well as circumvent electrical noise generated due to self-heating. This requirement demands efficient power distribution and conversion. Ring-oscillator (RO) simulations, shown in Fig. 2(a), display temperature effects on digital circuit performance: as we get closer to cryogenic conditions, mobility ($\mu$) increases, resulting in both a higher speed and higher-power consumption, yet having generally a better-energy efficiency. Fig. 2(b) illustrates how the recursive switched capacitor DC–DC (RSC) DC–DC converter proposed in this letter can be integrated into a cryogenic IC system close to the extreme temperature region to help facilitate voltage scaling. We experimentally demonstrate our 3-stage converter targeting operation temperature from 398 K down to 23 K, with efficiency >75%.

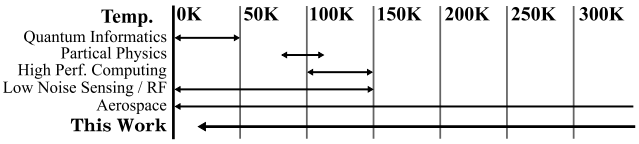


Fig. 1. Typical applications of cryo-electronics.

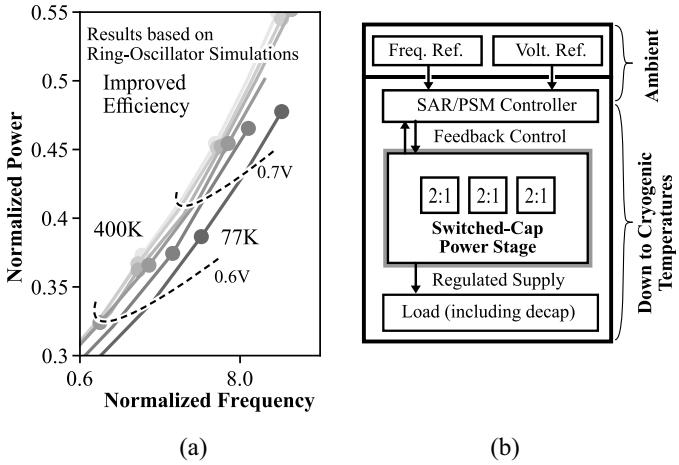


Fig. 2. Power scaling and cryogenic system power hierarchy. (a) Simulated power saving using voltage scaling from 400K to 77K. (b) Cryogenic electronic system power hierarchy design.

## II. RSC DC–DC Implementation and Methodology

A RSC consists of a chain of 2:1 switched capacitor conversion cells [5]. In addition to the power efficiency advantage demonstrated in [5], the RSC architecture is chosen because it contains parallel multiples of exactly two manually designed unit cell layouts, making it easy for us to analyze and implement automated layout generation.

### A. Circuit Implementation

Fig. 3 shows the schematic of a 2:1 cell. We propose to drive the switches with bootstrap drivers to provide a higher-gate voltage ($V_{\text{boost}}$) and reduce source-drain resistance ($R_{DS,ON}$). A higher-$V_{GS}$ over larger device sizing is preferred. This is advantageous when the temperature is extremely low because The transistor threshold voltage ($V_{TH}$) increases drastically at cryogenic temperatures [6], leading to a massive increase in $R_{DS,ON}$ for regular switches as shown in Fig. 4(a). The effectiveness of this design choice is illustrated

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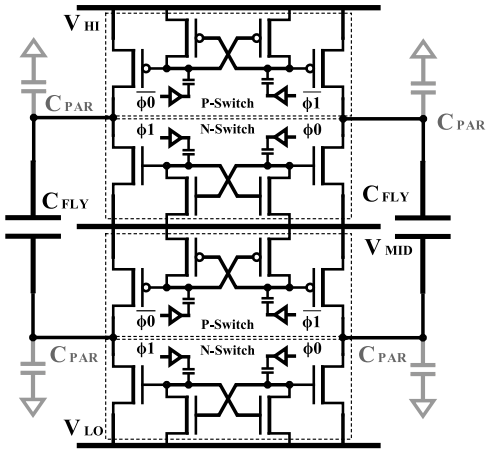


Fig. 3. Circuit implementation of the 2:1 conversion cell.

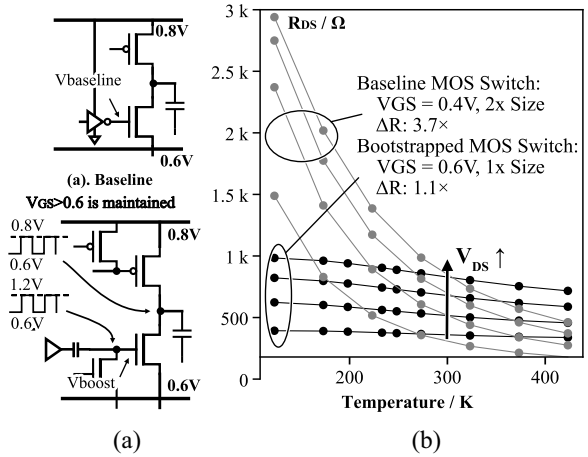


Fig. 4. Bootstrapped RSC switch. (a) Baseline. (b) Bootstrapped. (c) Regular versus bootstrapped switch RDS comparison.

in our simulation results Fig. 4(c).[1] Since e did not have access to cryogenic SPICE models in the 12-nm finFET technology node. we relied on prior publications to estimate the behavior of all elements in our circuit, such as MOSFETs [7] and passive components [8]. This allowed us to estimate the circuit's performance. Our circuit validation was post-fabrication. Additionally, since all the transistors in our design are isolated using deep-Nwell, the parasitic diode has no risk of turning on or causing significant deviation from the expected results.

### B. RSC's Design Parameter Optimization

*1) Capacitive Loss Analysis:* The derivation starts with analyzing the switching waveform, shown in Fig. 5: when the load current is zero, the 2:1 converter output equals $V_{\mathrm{IN}}/2$; when a current draw occurs, the $V_{OUT}$ will decrease by $\Delta V$. In an ideal switched capacitor system with zero resistive loss, the power loss comes from two sources: 1) the sharing loss ($L_S$) when injecting charges from the flying capacitor into the output capacitor and 2) the loss in the parasitic capacitance ($L_P$). Analysis of the two main capacitive loss mechanisms has shown an optimal $\Delta V$ that corresponds to the maximum efficiency [9]. This is shown graphically in Fig. 6.

[1]This simulation uses an extrapolated model. The vendor guarantees accuracy from 218K to 423K. The $R_{DS,ON}$ discussion is mainly based on [6] instead of this plot.

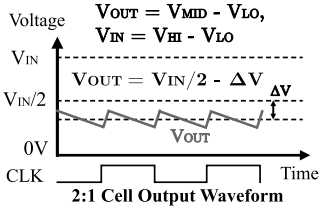


Fig. 5. Switching waveform.

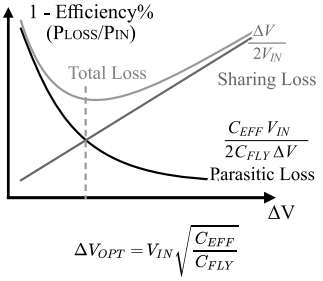


Fig. 6. Switched capacitor loss analysis.

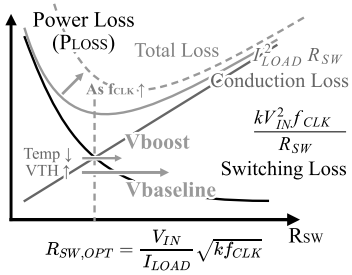


Fig. 7. MOSFET switch loss analysis.

Equation set (1). is the equation extended for N-stage RSC converters based on the assumption that $\Delta V$ is averaged evenly across all stages.

$$P_{\mathrm{IN}}(N) = \left(\sum_{i=1}^{N} 2\alpha_i C_i \left(\frac{\Delta V}{N}\right)^2 f_{\mathrm{CLK}}\right) V_{\mathrm{IN}} \tag{1a}$$

$$L_S(N) \approx \sum_{i=1}^{N} C_i \left(\frac{\Delta V}{N}\right)^2 f_{\mathrm{CLK}} = C_{\mathrm{FLY}} \left(\frac{\Delta V}{N}\right)^2 f_{\mathrm{CLK}} \tag{1b}$$

$$L_P(N) \approx C_{EFF} V_{\mathrm{IN}}^2 f_{\mathrm{CLK}} \tag{1c}$$

$$\Delta V_{OPT} = N \cdot V_{\mathrm{IN}} \sqrt{\frac{C_{EFF}}{C_{\mathrm{FLY}}}}. \tag{1d}$$

*2) Optimization of Switch Sizing:* The goal of transistor sizing is to balance the loss due to switch resistance (conduction loss) and the loss due to the capacitive parasitic (switching loss). This is shown graphically in Fig. 7. The dashed curve shows how the curve will move as frequency increases. An ideal feedback controller provides a maximum efficiency point tracking (MEPT) mechanism that modulates the clock frequency to track the lowest point on this curve for the least loss. From Fig. 7, the optimal switch impedance is given by (2) where $k$ is the coefficient relating to the parasitic capacitance and resistance of a unit-size MOSFET switch

$$R_{\mathrm{SW,OPT}} = \frac{V_{\mathrm{IN}}}{I_{\mathrm{LOAD}}} \sqrt{k f_{\mathrm{CLK}}}. \tag{2}$$

*3) Process/Temperature Variation Considerations:* As shown in (1b), the optimal $\Delta V$ is expressed as a ratio. Where $C_{\mathrm{EFF}}$ is primarily contributed by routing capacitance while $C_{\mathrm{FLY}}$ variations

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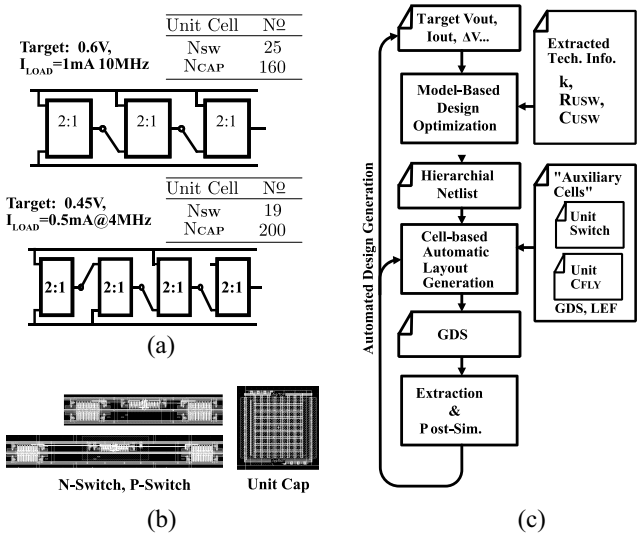


Fig. 8. Diagram of the automated flow [10]. (a) Some example configurations. (b) "Auxiliary Cell" building blocks. (c) Automated design flow.

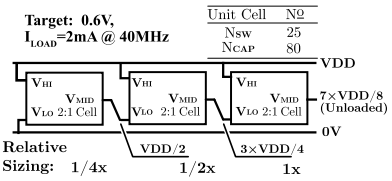


Fig. 9. RSC fixed-ratio 7:8 converter for tapeout.

TABLE I
CONSTANTS USED DURING DERIVATION

| Symbol | Meaning |
|---|---|
| $\alpha_i$ | Up/Down Configuration of Stage $i$ |
| $\Delta V$ | Voltage Delta due to Current Draw |
| $C_{EFF}$ | Effective Parasitic Capacitance |
| $C_{FLY}$ | Flying Capacitance |
| $k = R_{USW} \cdot C_{USW}$ | Approximated relationship of switch resistance & capacitance |
| $C_{UFLY}$ | Unit Capacitor Cell Capacitance |
| $R_{USW}$ | Unit Switch Cell On-State Resistance |
| $C_{USW}$ | Unit Switch Cell Parasitic Capacitance |

are attenuated and result in a nearly constant $\Delta V$ across process variation. The relationship between $R_{\mathrm{SW,OPT}}$ and $f_{\mathrm{CLK}}$ is not constant due to the change in mobility under different corners. To achieve optimal efficiency when the switch resistance is the limiting factor (technology dependent), calibration has to be done on a prechip basis.

### C. Cell-Based Layout Generator

Now that $\Delta V$ is fixed as a meta-parameter, the optimized capacitor and switch sizing can be expressed in an integer amount of unit cells. The extended synthesis formula set (3) is converted into a Python-based design generation flow Fig. 8(c). Fig. 8(a) shows some example synthesized optimal designs

$$I_{\mathrm{LOAD}} = 2C_{\mathrm{FLY(laststage)}} \frac{\Delta V}{N} f_{\mathrm{CLK}} \tag{3a}$$

$$N_{\mathrm{CAP(laststage)}} = \frac{N \cdot I_{\mathrm{LOAD}}}{2\Delta V f_{\mathrm{CLK}} C_{\mathrm{FLY(unit)}}} \tag{3b}$$

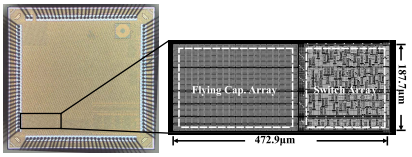


Fig. 10. Die photograph and GDS top view.

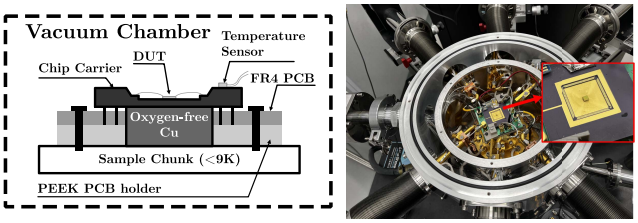


Fig. 11. Test setup. (a) Test setup diragram. (b) Test setup photograph.

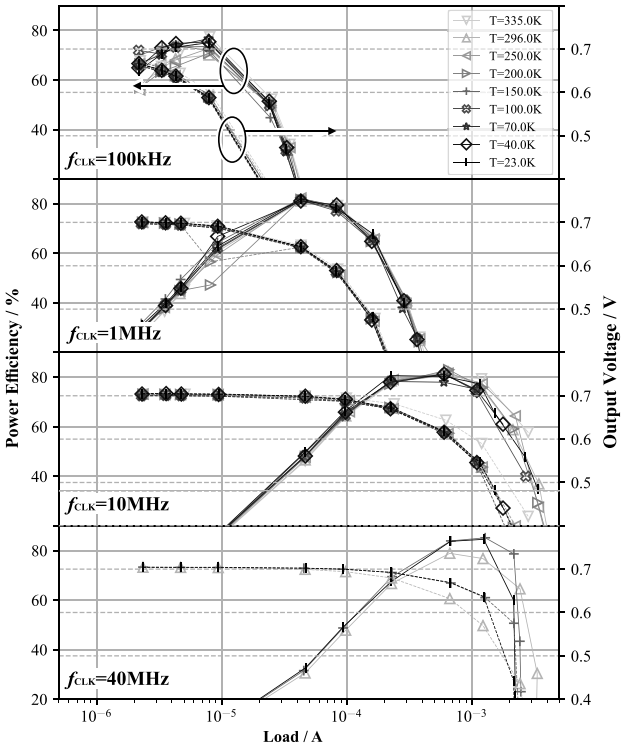


Fig. 12. Power efficiency and output voltage swept across load current, frequency, and temperature.

$$N_{\mathrm{SW(laststage)}} = \frac{I_{\mathrm{LOAD}} R_{\mathrm{SW(unit)}}}{\sqrt{k} V_{\mathrm{IN}} \sqrt{f_{\mathrm{CLK}}}}. \tag{3c}$$

A 3-stage converter optimized for 0.6 V, 2-mA output at 40 MHz, shown in Fig. 9, is taped out in a 12-nm FinFET process. The fabricated chip is shown in Fig. 10.

## III. CRYOGENIC MEASUREMENTS

The chip setup was placed in a cryo-chamber and cooled by a closed-cycle refrigerator (CCR). Limited by the physical size of the assembly, the lowest temperature achievable is 22.5K. Before the test, >1-h soaking is given to ensure temperature stability. Fig. 11(a) shows the detailed measurement setup.

The converter's power efficiency and output voltage are measured across a wide range of frequencies, temperature (398K to 23K), and output loads (2 $\mu$A to 4 mA). A passive variable resistor is used as

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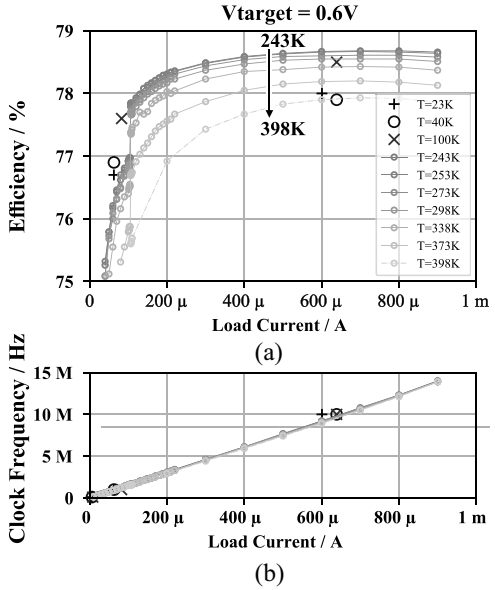


Fig. 13. Closed-loop efficiency and clock frequency plots across a wide temperature range. (a) Maximum efficiency versus load current. (b) Frequency versus load current at maximum efficiency tracking.

TABLE II
COMPARISON WITH RELATED WORKS

| Metric | This Work | [13] | [14] | [11] | [5] | [12] |
|---|---|---|---|---|---|---|
| Architecture | RSC - Fixed | Tunable or Fixed | Fixed 2:1 LC Reson. | RSC - Tunable or Fixed | RSC - Tunable or Fixed | LDO |
| Wide Temp. Range | Yes (23K-400K) | - | - | - | - | No (4K Only) |
| Technology | 12nm | 22nm | 45nm SOI Integ. Ind. | 350nm HVCMOS | 250nm | 22nm SOI |
| Input Voltage | 0.8V | 1.23V | 1V | 2∼13V | 2.5V | 1.8V |
| Output Voltage | 0.6V | 0.45∼ 1V | 0.35∼ 0.41V | 5V | 0.1∼ 2.2V | 1.5V |
| Reported Efficiency Range | 75% @ 400K, 0.1mA; 80% @ 23K, 1mA | <70% @ 0.55V 84% @ 1.1V | 75.5%@ 0.44A/mm$^2$ 70.2%@ 0.92A/mm$^2$ | 81.5% @10.7V in 1.3mA; <30% @2V in 0.2mA | 85% Peak; <70%@ 0.1A/mm$^2$ | - |
| Load Range | $<1\mu A$ ∼2mA | 88mA | 25∼295mA | 0.2mA & 1.3mA | 2mA | 64mA @ 3.7K |
| Current Density | 0.02 A/mm$^2$ | 0.38 A/mm$^2$ | 0.92 A/mm$^2$ | 0.0013 A/mm$^2$ | 0.0028 A/mm$^2$ | 1.43 A/mm$^2$ |
| Drop-Out | 0.2V | 0.68V | 0.65V | - | 0.3V | 0.3V |

a load, with a 1-$\mu$F capacitor in parallel. The measurement results plotted in Fig. 12 show the peak efficiency points at each input clock frequency. The output voltage $V_{\text{OUT}}$ remains close to the design target of 0.6V. Fig. 13 shows the measured efficiency when an external feedback loop is applied to regulate the output using pulse density modulation (PDM) [5]; the design's efficiency varies by less than 3% across the tested temperature range, with a high-control linearity of $R^2 = 0.99$.

## IV. CONCLUSION

This letter presents an automated framework for a cryogenic switched-capacitor (SC) DC–DC converter design generation, based on an innovative optimal sizing methodology, demonstrated by silicon measurement results under cryogenic temperatures. Measure results of our proposed design are highlighted in comparison Table II. The converter delivers comparable power efficiency to prior art [11] across wide load ranges at very low-drop-out voltage due to the low-$R_{DS,ON}$ design. Compared to a previously reported high-performance cryogenic LDO design [12], our converter is able to cover a much wider [23K, 398K] temperature range and was measured at NIST.

*Code Availability:* The source code is available in [10].

## ACKNOWLEDGMENT

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