A Reconfigurable Analog FIR Filter Achieving -70dB Rejection with Sharp Transition for Narrowband Receivers

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Abstract

We present a compact, highly reconfigurable charge-domain analog-FIR (AFIR) filter for high channel selectivity receivers such as BLE, Zigbee, and IoT applications. This architecture demonstrates excellent power-scaling with reconfigurability to different bandwidth and desired stopband rejection. The charge-domain FIR filter modulates both pulse width and transconductance which multiply to generate the charges of the FIR coefficient. Varying both time and transconductance achieves high programmability enabling a wide range of bit-resolution and FIR tap number combinations to achieve a customizable filter response at optimal power. Fabricated in 28nm CMOS, the filter achieves -70dB stopband rejection with a sharp transition and a low power consumption of 0.356mW.

Introduction

The need to adapt to various wireless standard has increased with expansion of programmable receiver front-ends, making a reconfigurable baseband filter an critical component. For multi-channel narrowband applications, these systems require high channel selectivity, narrow bandwidth with tunability, low power consumption, and good linearity. Fig. 1 shows a typical zero-IF receiver with at least one gain stage followed by a high selectivity low-pass filter (LPF) at receiver baseband. The gain stage is commonly embedded with at least 1st-order low-pass filtering, which is sufficient to provide high frequency out-of-band (OOB) signal rejection. Therefore, the high selectivity LPF must mostly filter the close-in frequency band. Moreover, the gain stage can suppress input-referred noise of the LPF, making the gain and noise requirement of LPF less important. Instead, the LPF needs to provide maximal flexibility in terms of bandwidth, stopband rejection, and transition sharpness.

Recently, many high selectivity LPF techniques have been proposed [1-7]. A coupled source-follower [1] suffers from poor bandwidth tunability as it is fixed by the combination of transconductance(gm) and capacitance. Charge-sharing infinite-impulse-response (CS-IIR) techniques [2-4] are not able to achieve a sharp transition necessary for high-selectivity while bandwidth-reconfigurability requires large capacitance area. A full-rate cascaded-AFIR filter [5] requires very high-power consumption to achieve a sharp transition. Similar AFIR approaches [6-7] that integrate time-varying current on the capacitors followed by down-sampling demonstrate a sharp transition and good OOB rejection. However, [6] requires high power consumption which is not suitable for IoT application, and [7] does not achieve a sharp transition for -70dB OOB rejection.

Proposed Charge-domain Hybrid DAC AFIR Filter

The proposed AFIR filter structure leverages similar principles as in [6-7]. However, to achieve a high stopband attenuation and a sharp transition, a high-resolution DAC is necessary to quantize the FIR coefficients. The straightforward way is to increase the number of bits in gm-DAC. However, several issues emerge in doing this: 1) The finite output impedance results in charge leakage, which requires additional coefficient calibration. 2) Increased parasitic caps result in charge-sharing IIR effects between marching-taps, making FIR coefficients time-dependent. 3) Increased gm mismatch degrades DAC linearity.

To address these issues, we propose a hybrid charge- and time-domain DAC which realizes 11-bit FIR coefficients (Fig. 2). The accumulated charge per tap is the multiplication of on-time of gm, the gm value, and the input signal. We use dual gm-DAC paths (Gm_{msb} / Gm_{lsb}) with individual timing controls (T_{msb} / T_{lsb}) to balance the time/charge dimensions. While leveraging time domain control signals loses the embedded sinc anti-aliasing filter, it introduces the benefit of odd-order f_{clk} (input sampling frequency) alias frequency cancellation observed twice at both edges of the sampling clock. Note that out-of-band rejection from the bandwidth to 1st f_{clk} alias frequency is mainly governed by the AFIR filter assuming the residual tones at $n \cdot f_{clk}$ are filtered out by an LPF placed before the AFIR filter (in the gain stage).

Fig. 3 shows the proposed AFIR filter architecture. We split the 11-bit charge-domain DAC into a 7-bit time-DAC and a 4-bit gm-DAC. This resulted in only 16 (Gm_{msb}) + 1(Gm_{lsb}) gm units interacting with the output integration capacitors. This small number of gm unit allows further enhancement of linearity by placing a resistor (2kΩ) on the source-side. Time-interleaving paths were implemented to increase the output sampling rate by a factor of 2, and dedicated common-mode feedback circuits are used to set individual path's output common-mode to resolve path mismatch. The time-DAC is realized with a ring-DTC structure to generate different pulse-widths to control the on-time of gm-DAC. An inverter-based DTC is used for its high linearity and to match the pulse-width (~30ps) with the gm-DAC settling time. Noise reduction was less emphasized since it can be suppressed with total receiver gain. Two single-port SRAMs with 64 13-bit words store the weight coefficients. The flexibility of FIR filtering is controlled by programming different number of FIR taps/bits in the digital controller.

Fig. 4 shows the multi-lap ring-DTC structure. It consists of a 33-stage inverter ring, a delay control loop for setting unit delay(~60ps), a lap counter, a ring mask, and a pulser. The inverter outputs are connected to a 33:1 multiplexer (MUX), and the MUX output clock signal is sent to the lap counter. The lap counter counts the target number of times the edge passes and outputs a delayed edge to the pulser. Lap control significantly increases the time-DAC range. Odd-stage inverter paths need to be masked with proper delay to avoid a false initial trigger. Extra delay contributing from trace routing, MUX and lap counter are calibrated out at reference edge of the pulser. A total of 7-bit DTC is implemented on T_{msb}, while a 4-bit DTC sharing the same unit delay is implemented on T_{lsb}. The time-interleaved paths share the same ring to mitigate path mismatch and reduce the power consumption.

Measurements

The prototype of the proposed AFIR filter was fabricated in 28nm CMOS process with compact area of 0.05mm^2. Die micrograph is shown in Fig. 11. Fig. 5 shows the measured normalized frequency response of the filter. It demonstrates a tunable bandwidth ratio of 6.8 while maintaining the same f_{clk} alias frequency at 48MHz. The ratio increases to 12.4 with 80MHz clock frequency. Using ≥96 taps with 11-bit resolution, -70dB stopband rejection is achieved. The measured reconfigurability of stopband rejection and transition sharpness is shown in Fig. 6. The f_{clk} aliasing frequency cancellation achieves -40dB rejection. Having a 0.5MHz bandwidth -30dB/dec low-pass filter (-59.5/-68.5dB rejection at 48MHz/96MHz) in front of the AFIR filter would be sufficient to eliminate the residual peaks at $n \cdot f_{clk}$. Fig. 7 shows the out-of-band OIP2 and OIP3 power measurement. Fixing the intermodulation signal at 50kHz, two tones at 4.01MHz and 7.97MHz were applied for OIP3 measurement, and 4.01MHz and 4.06MHz for OIP2 measurement. Fig. 10 shows the result of sweeping the frequency offset from 2MHz to 40MHz for both OIP2 and OIP3 measurement. The average result is shown in Table. 1. The power optimization trade-offs for desired out-of-band rejection and clock aliasing frequency are shown in Fig. 8. All results are measured under 1MHz output sampling rate and similar bandwidth (0.46MHz). Fig. 9 shows the power consumption of the AFIR filter as a function of reconfigurable parameters. Table 1 summarizes the chip performance measured with 800mV supply voltage. Given matching output sampling rate (1MHz) and similar bandwidth (0.46MHz) as [7], the proposed AFIR shows its reconfiguration ability with two with two FIR coefficient configurations: 1) a stopband rejection 10 dB better than previous works and a sharp transition to -70dB and, 2) a low power consumption of 90uW while achieving -60dB rejection matching state-of-the-art.

References

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[3] P. Payandehnia *et al*., *TCAS-I*, 2018.
[4] A. Bozorg *et al*., *JSSC*, 2022.
[5] M. Huang *et al*., *JSSC*, 2013.
[6] S. Hameed *et al*., *JSSC*, 2018.
[7] B. Thijssen *et al*., *JSSC*, 2020.

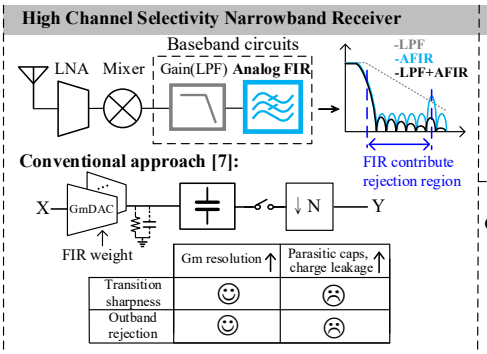

Fig. 1 High channel selectivity narrowband receiver and conventional approach

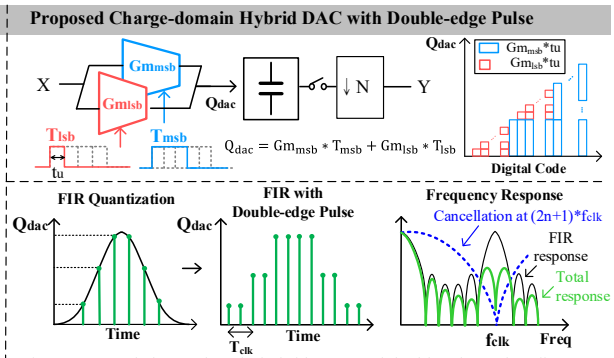

Fig. 2 Proposed charge-domain hybrid DAC and double-edge pulse alias frequency cancellation

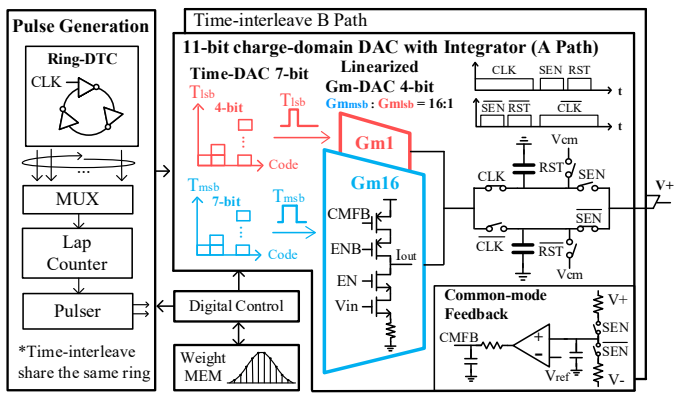

Fig. 3 The proposed 11-bit charge-domain AFIR architecture

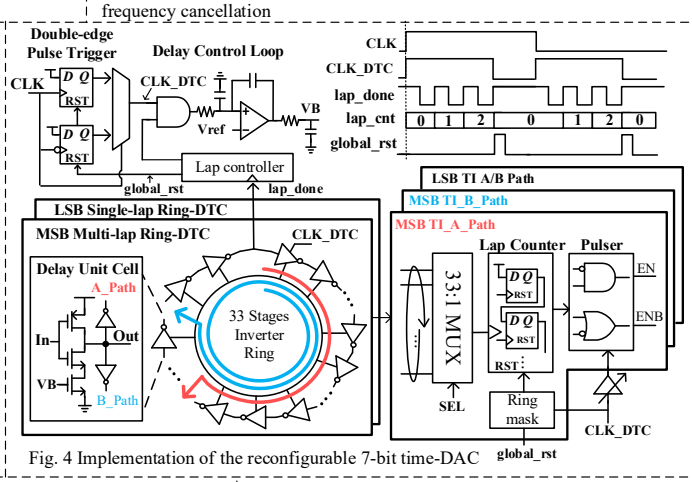

Fig. 4 Implementation of the reconfigurable 7-bit time-DAC

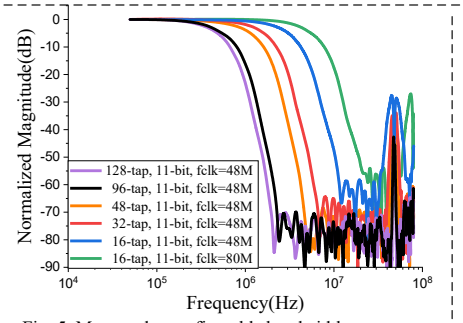

Fig. 5 Measured reconfigurable bandwidth

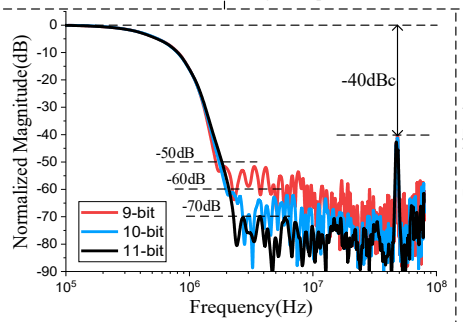

Fig. 6 Measured reconfigurable stopband rejection

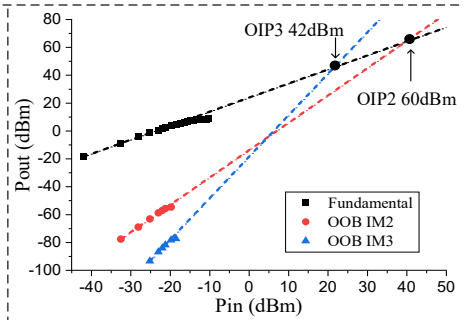

Fig. 7 Measured OIP2/OIP3 versus input power curve

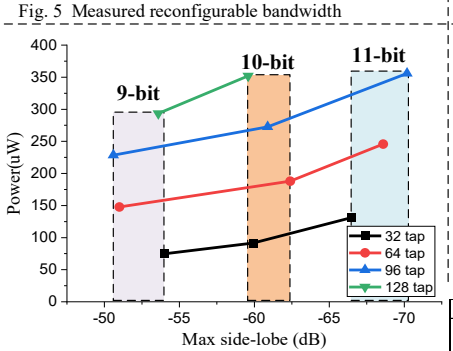

Fig. 8 Power/rejection optimization with different taps/bits

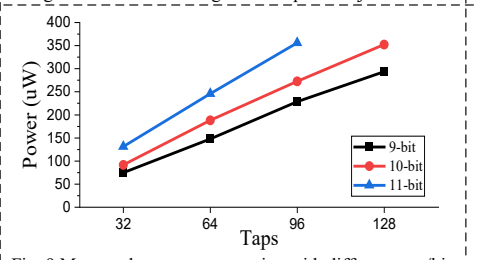

Fig. 9 Measured power consumption with different taps/bits

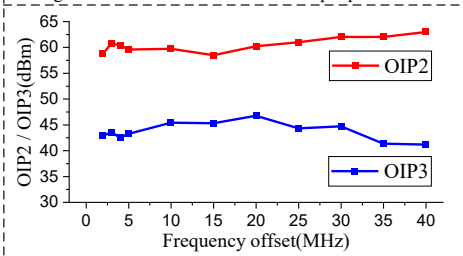

Fig. 10 Measured OIP2/OIP3 versus frequency offset

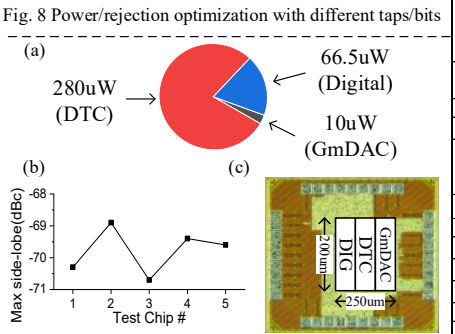

Fig. 11 (a) Power breakdown (b) Measured max. side-lobe across 5 chips (c) Die photo

Table. 1	This work		JSSC'20[7]	JSSC'13[5]	JSSC'18[6]	JSSC'14[2]	TCAS'18[3]	JSSC'22[4]
Topology	CD-AFIR		AFIR	Cascade-AFIR	FA	CS-IIR	CS-IIR	CS-IIR
Reconfigurability#	9/10/11-bit + 16~128-tap		10-bit + 16~128-tap	3-bit delay(D_T)	10~70pF caps	0.25~64pF C_H+ 0.4~2.2pF C_S	1~68.5pF C_H+ 0.5~4pF C_S	1~19pF C_H+ 0.5~4pF C_S+ 1~6pF C_{IH}
Technology	28nm CMOS		22nm FDSOI	65nm CMOS	65nm CMOS	65nm CMOS	180nm CMOS	28nm CMOS
Supply (V)	0.8		0.7	1.2	1.2	1.2	1.8	0.9
Tunable BW (MHz)	0.37-4.6		0.06-3.4	5-26	1.25-20*	0.4-30	0.49-13	1-9.9
Max. side-lobe(dB)	Low power (32-tap/10-bit)	Max rejection (96-tap/11-bit)	-60 (128-tap/10-bit)	-65.3	-70	-	-	-
	-60*	-70						
f_{-60dB}/f_{-3dB}	4.15*	4.5	3.8	1.5	3.3†	7.8†	7.5†	14†
Power(mW)	0.09*	0.356	0.092	8.4	76.8~100.8	1.98	4.3	0.92
IB OIP3‡ (dBm)	25		-	13	31	31	28.7	32.4
OB OIP3‡ (dBm)	43.7		28	-	44	21	32.6	41.3
OB OIP2‡ (dBm)	60.5		-	-	87	69.3	73.5	-
Gain (dB)	23.5		31.5	41	23	9.3	17.6	14.7
IRN (nV/√Hz)	26§		12	12.3	-	4.57	6.54	3.5
Area (mm²)	0.05		0.09	0.52	0.23	0.42	2.9	0.192

#Fix clock frequency; *For 32-tap/10-bit/clk=16MHz; †Estimate from figure; §Integrated over 50k-460kHz; ‡Baseband BW; ‡OIPn=IIPn+Gain