A Sub-mm^3 Wireless Neural Stimulator IC for Visual Cortical Prosthesis With Optical Power Harvesting and 7.5-kb/s Data Telemetry

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***Abstract*— This article proposes StiMote, an untethered, free-floating and individually addressable stimulator mote designed for visual cortex stimulation, aimed at vision restoration. The system is optically powered by a custom photovoltaic (PV) layer. In addition, the photodiode (PD) layer captures the light modulation and forwards it to the optical receiver (ORX) including a tranimpedance amplifier. Translated instructions can assign a unique slot, up to 1024 available, to each mote within the time-division multiple access (TDMA) framework. In this work, we propose an automatic charge balance (CB) technique that monitors the injected charge to balance in bi-phasic switched-capacitor stimulation (SCS). The chip was confirmed fully functional when operated completely wirelessly using harvested light. Measurement results revealed a power consumption of 4.48 μ W with a 7.5-kb/s optical downlink data rate, corresponding to continuous updates at 2.5 Hz of 1024 motes to their individual 3-b stimulation intensity levels. The dc–dc converter, responsible for providing high voltage for stimulation, demonstrated 4.3-V output voltage when unloaded, with a maximum efficiency of 67.4%. The proposed CB circuit exhibited linear controllability of stimulation charge up to 16 nC, with a charge imbalance of less than 0.2 nC. Furthermore, in vitro testing confirmed the absence of chemical reactions at electrodes, and in vivo experiments conducted on live rats verified the effectiveness of the stimulation through StiMote.**

***Index Terms*— Bio-implant mote, brain–machine interface (BMI), charge balance (CB), flip chip bonding, low-power optical receiver (ORX), Manchester encoding, switched-capacitor stimulation (SCS), transimpedance amplifier (TIA), visual cortical prosthesis (VCP).**

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I. Introduction

RESTORING vision stands as one of the most sought-after and impactful pursuits in the field of biomedical research. Retinal prostheses aim to restore vision by stimulating the retina. However, achieving high-resolution stimulation is particularly challenging since the "high-acuity" area of the retina, known as the fovea, encompasses only the central 1° of vision and measures a mere 0.35 mm in diameter, (0.1 mm^2) [1]. Conversely, this same high-acuity region is magnified in the human visual cortex by over three orders of magnitude [2], expanding to an area of 1 cm^2, providing sufficient space for high-resolution microstimulation. Cortical stimulation can also treat optic nerve disease, whereas retinal prostheses require a healthy optic nerve to send signals to the brain [3].

A visual cortical prosthesis (VCP) requires a high electrode count (>100) to achieve reasonable visual resolution. As estimated in [4], a 25 × 25 array of intracortical electrodes positioned within the 1-cm^2 area of the primary visual cortex, also known as area V1, can enable 20/30 vision.

This implies that practical visual acuity can be accomplished with a stimulating electrode spacing of 400 μm, a dimension achievable with the current state-of-the-art electrode array technology [5]. However, it is important to highlight that the challenge of wiring such large arrays remains unsolved, emphasizing the need for a wireless system.

A number of remarkable miniature wireless brain stimulation systems have been recently proposed [6], [7], [8], [9], [10], ranging in size from 6 to 500 mm^3. While these dimensions are suitable for applications that demand only a few stimulation channels, such as deep brain stimulation and restoring mobility, they do not provide the required implantation density for VCP.

A key challenge for VCP is the requirement for each of the hundreds of stimulation channels to be independent, capable of variable output (with a minimum of seven levels or 3 bits), and able to update at a minimum rate of several Hz, while maintaining a stimulation frequency exceeding 50 Hz for flicker fusion in humans [11]. The motes must therefore be individually addressable, and the mote cluster must support a high data rate (>5 kb/s). One approach is to use a single cm^2-sized electrode array with 100 s of electrodes; however, the resulting rigidity will evoke brain scar tissue formation due to brain micro-motion, limiting electrode lifetime [12], [13]. Hence, there is an unaddressed need for a sub-mm^3, free-floating stimulation unit that is designed for high-density placement (>100 s of units in a 1-cm^2 area), with individual addressing and stimulation control.

Hence, we propose an optically powered stimulation mote, called StiMote, which is individually addressable and can support up to 1024 units operating with seven intensity levels at 50-Hz stimulation rate and 2.5-Hz intensity update rate. StiMote uses a custom-designed GaAs chip [14] for near-infrared (NIR) power transfer and bi-directional optical communication. Using a single discrete 100-nF charge storage capacitor (0.004 mm^3), StiMote generates a balanced biphasic stimulation current using switched capacitor charge injection. Ultra-low-power design results in 4.48-μW power consumption allowing a system size of $0.25 \times 0.25 \times 0.3$ mm^3 (0.02 mm^3). The complete StiMote system was bench-top-tested and is fully functional. Stimulation capability was confirmed using an in vivo stimulation test using a live rat brain.

This article is an extended version of [15] and offers more comprehensive explanations and in-depth analysis. The organization of this article is as follows. Section II provides an overview of the system. Section III delves into the detailed circuit implementation and its analysis. Section IV presents the results of the measurements, and Section V concludes this article.

II. System Overview

A. Free-Floating Stimulator Motes

The concept of a two-step power and data transfer is illustrated in Fig. 1. Numerous StiMotes are positioned in a free-floating manner on the cerebral cortex surface with 400-μm pitch to activate neurons using a 8.4-μm-diameter platinum–iridium (PtIr) tip-coated, Parylene-C-insulated, carbon fiber electrode (CF) [16]. These motes receive global power and control from a cm-sized repeater unit (RU) situated in the epidural space or skull. The RU uses an array of light-emitting diodes (LEDs) of peak wavelength at 850 nm that emits both dc light for chip power and modulating ac signals to provide instructions or stimulation intensities. Furthermore, the RU uses an array of single-photon avalanche diodes (SPADs) to decode optical uplink signals originating from individual motes. The optical link consists of approximately 1 mm for the dura mater, with an additional 0.2 mm of cerebrospinal fluid (CSF) on either side [17], [18]. This work shares the system architecture proposed in [19] while introducing a novel mote structure designed for neural stimulation, as opposed to neural recording in [19].

Each StiMote incorporates a custom-integrated GaAs epitaxial structure consisting of a dual-junction photovoltaic (PV) layer and a dual-purpose photodiode and LED (PD-LED) layer [14]. The PV layer supplies a sufficient 1.55-V voltage, effectively powering the CMOS layer. Simultaneously, the modulated photocurrent produced by the PD-LED in its default PD mode is directed into the receiver and subsequently translated into digital data. When a received instruction translates into an LED firing command, the PD-LED briefly switches to the LED mode, enabling the mote to promptly identify itself to the RU through its unique ID-based pattern.

The intermediate CMOS layer interfaces with the PV layer, serving as the central controller for three key functions: 1) energy harvesting; 2) signal transceiver; and 3) stimulation driver. The two chip layers, comprising the optical and CMOS layers, incorporate through-wafer vias and are thinned down to a thickness of 50 μm. These layers are then securely bonded using solder bumps and a flip-chip solder reflow process. From a bottom perspective, the CF electrode is electrically and mechanically integrated with the CMOS layer via a through-silicon via that terminates at the bottom metal within the CMOS layer. In addition, metal-deposited pads beneath other vias function as bonding pads for discrete 008004 footprint 100-nF capacitors [20], facilitating charge storage, and for a stimulation counter electrode. A mote structural prototype with bonded layers, excluding the storage capacitor, is depicted in Fig. 2. This article focuses on the CMOS layer.

Each StiMote independently controls a 3-b stimulation charge parameter Q_{STIM}. The system uses time-division multiple access (TDMA) communication to achieve a 30× reduction in the required bandwidth compared with addressing each mote individually with an address followed by its modulation level. This approach not only reduces receiver power but also contributes to mote size reduction.

Upon stabilization, all the motes synchronize with a global optical clock continually emitted by the RU. During the initial mote configuration, each mote is individually addressed based on its unique 16-b physically unclonable function (PUF) ID [21]. The motes start to listen to instructions from the RU, and the RU systematically cycles through the available 16-b chip IDs, commanding the motes to fire the LED if the PUF ID matches with the ID included in the command. This process enables the mapping of the spatial placement of motes

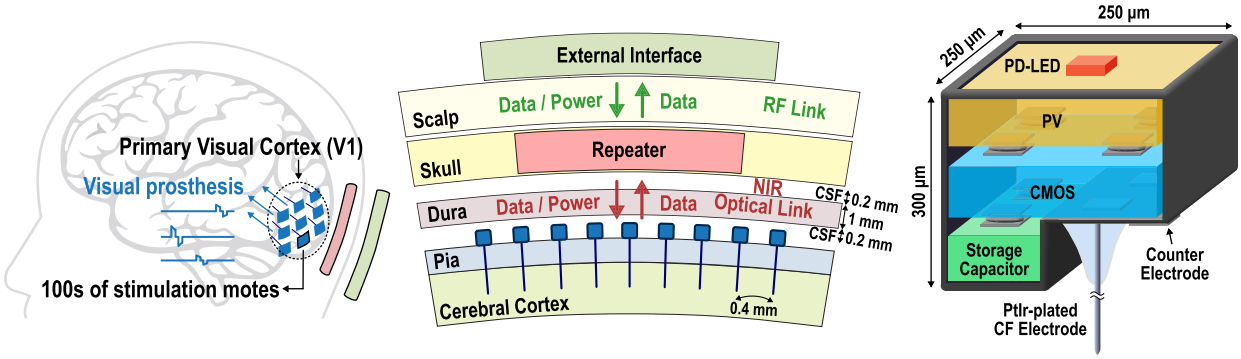
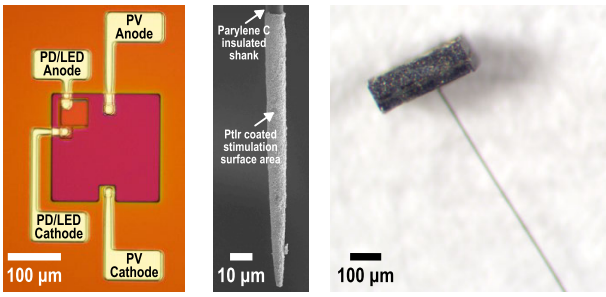


Fig. 1. Conceptual overview of the proposed free-floating stimulator motes and cross-sectional view of stacked layers.



(a) (b) (c)

Fig. 2. (a) GaAs PV/PD-LED cell for the NIR-based optical link. (b) PtIr-coated CF electrode tip. (c) Dummy mote featuring bonded GaAs and CMOS chip layers with an anchored CF.

across the cortex. Subsequently, the RU assigns each mote a unique TDMA time slot. After all the motes are configured, the RU communicates images by repeatedly transmitting an initial 10-b synchronization preamble followed by up to 1024 sets of 3-b TDMA data slots, which continuously update the stimulation intensities per site. A more comprehensive description of the communication protocol is provided later in Section III-C.

Regarding the biocompatibility of the completed mote, while the chronic intracortical use of CF has been studied [16], [22], [23], hermetic packaging of the bonded chips is needed to limit patient exposure to toxic materials in the silicon microelectronic components and GaAs PV cells. The maximum health risk related to arsenic for an areal coverage of 1 cm and a GaAs liftoff solar cell is approximately 1.5 mg of arsenic. While the toxicity of local exposure to arsenic via an implanted device is currently unknown and will depend on the solubility of GaAs-related materials in the body, the minimum lethal dose of arsenic falls within the range of 1–3 mg/kg of body weight, or 60–180 mg for an average human mass of 60 kg.

B. Single Mote System and Operations

The building blocks and their connections in the CMOS layer are illustrated in Fig. 3. Comprising three main segments, it consists of: 1) the optical link; 2) the digital controller; and 3) the stimulation controller. The optical link interfaces directly with the PD-LED layer. To support dual modes, the PD-LED layer's anode and cathode are designed for reverse bias in PD or forward bias in LED. These connections are selectively linked to either the optical receiver (ORX) front-end through I_{PD} or the LED driver through I_{LED}. Its default configuration links to the ORX, receiving the Manchester-encoded modulation signal. Only upon receiving LED firing commands, it switches to the LED mode to emit a distinctive chip ID-based pattern and returns back to the PD mode if completed.

The digital controller encompasses a clock and data recovery (CDR) block, an instruction processor, and an LED pulse pattern generator. The CDR obtains an encoded signal oversampled by the oscillator clock from the ORX, delivering recovered signals CLK_{ORX} and $DATA_{ORX}$ to the instruction processor. This processor translates bit serial $DATA_{ORX}$ into specific instructions. The LED pulse pattern generator uses the 16-b PUF ID_{CHIP} to generate the corresponding pattern SW_{LED} when enabled by the processor.

The stimulation controller includes a phase controller, a charge balance (CB) circuit, and a driver. The finite state machine (FSM) dedicated to stimulation phase control facilitates switching between stimulation phases and shorting the electrodes at the resting phase. The CB circuit equalizes bi-phasic charges, preventing electrode degradation caused by metal-ion diffusion. The stimulation driver directly interfaces with the storage capacitor and electrodes, promptly drawing 10 s of μA stimulation current I_{STIM} from the capacitor to the electrodes, and it alternates the current direction based on the stimulation phases.

Both instantaneously high currents, I_{LED} and I_{STIM}, should not be directly drawn from V_{DD} but from the storage capacitor V_{STORE}. A dc–dc 1:3 upconverter was used to convert the PV layer output 1.55 V to 4.3 V. In addition, the CMOS layer uses a two-transistor voltage reference (2T-VR) [24] to provide a process, voltage, and temperature (PVT) tolerant voltage V_{REF} around 230 mV to the ORX for PD regulation and the CB for monitoring the stimulation current.

C. Optical Power Downlink

The primary limitation on light intensity is determined by brain safety concerns. In our application, we focus light on a specific tissue area to induce the essential PV effect of the PV layer for self-powering the CMOS layer. While the dura functions as a transparent window within the NIR range [17], [18], it is imperative to ensure that all the delivered power, both in the dura and cortex, is safely absorbed within the tissue without causing a significant increase in temperature. As a

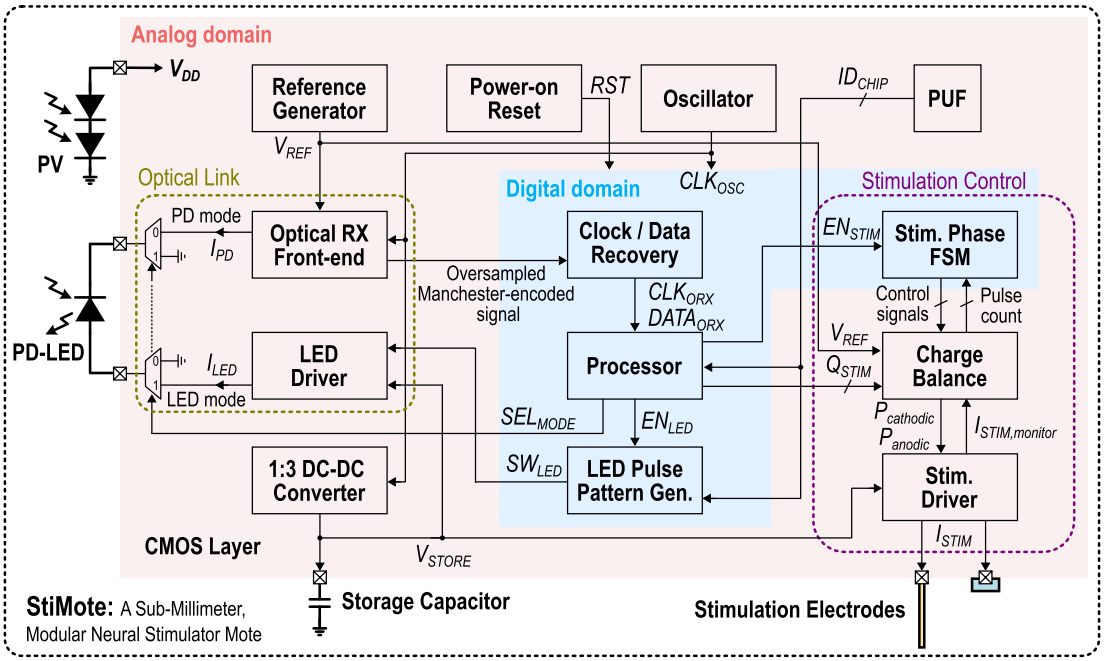


Fig. 3. Top-level diagram of the StiMote system, with emphasis on CMOS layer blocks.

result, establishing a meticulous upper limit for light irradiance becomes crucial to mitigate any potential harm to the tissue.

The American National Standards Institute (ANSI) has established an NIR irradiation limit of 1.36 mW/mm^2 to prevent tissue heating [25]. An independent ex vivo experiment [14] revealed that the nonhuman primate dura exhibits optical transmittance exceeding 35%. The multiplication of these values yields an incident power of 475 μW/mm^2 on the PV layer.

Our proof-of-concept custom PV cell was initially designed to deliver 1.5 μW at the maximum power point under NIR illumination of 150 μW/mm^2 across a 200 × 200 μm^2 area [14]. This translates to 7.4 μW at 475 μW/mm^2 (75% of the tissue limit) for the proposed StiMote's 250 × 250 μm^2 optical layer. The measured power of the CMOS layer 4.48 μW falls below this limit, underscoring the feasibility of an optical power harvesting-based bioimplant application.

Another aspect to consider is the loss due to misalignment in the optical path. In this respect, the optical scattering within the dura can actually be advantageous as it helps mitigate variations by diffusing the light. Our prior experiments measuring optical transmittance through non-human primate dura suggest a vertical variation of approximately 5% from incident flood illumination from the repeater [14]. We also estimated that a lateral misalignment of 1 mm would result in a 28% loss [14]. When conservatively taking into account the cumulative loss of 33%, the harvested power at the PV layer still meets the chip's power requirements; however, there is potential for improvement in this margin with an optimized repeater design [26].

III. Circuit Implementation and Analysis

A. Stimulation Driver and Automatic Charge Balance

The overall simulation structure should comprehensively consider the target simulation current, charge density, and

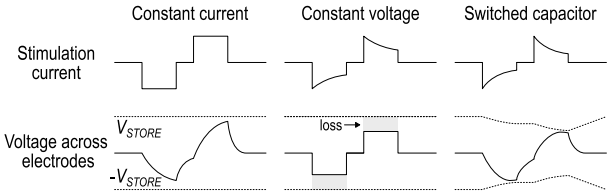


Fig. 4. Comparison of three electrical stimulation types.

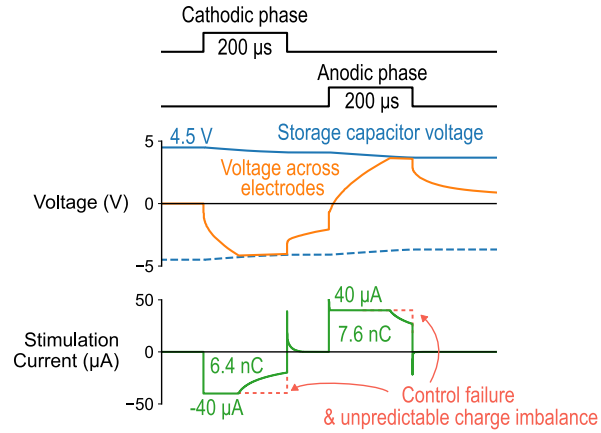
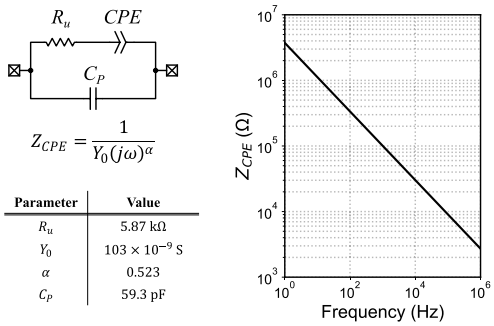


Fig. 5. Simulation on the conventional CCS method using the StiMote component models, illustrating its failure case attributed to the high impedance of electrodes.

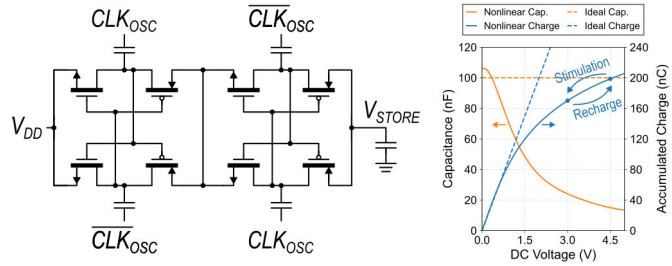
pulsewidth along with electrode impedance to ensure the stimulation pulse effectively evokes a practical biological response. In our application aimed at visual prostheses through brain stimulation, the threshold charge per phase is known to be approximately 4 nC with 200-μs pulsewidth [27]. To effectively evoke neuronal responses, we have chosen a nominal simulation charge of 8 nC, which is twice the threshold. This translates to 40 μA flowing for 200 μs, assuming constant current flow. As biphasic stimulation is required to prevent continuous chemical reactions at the electrode tips and their effects on the human body, a total



Parameter	Value
R_u	5.87 kΩ
Y_0	103×10^{-9} S
α	0.523
C_P	59.3 pF

(a) (b)

Fig. 6. (a) Circuit model of electrodes and tissue for fitting EIS impedance data. (b) CPE impedance across frequency.



(a) (b)

Fig. 7. (a) Schematic of the 1:3 dc–dc converter and (b) nonlinear characteristics of the 100-nF storage capacitor used in the StiMote system illustrating the repeating points between stimulation and recharging cycles.

of 16 nC (40 μA for 400 μs), including current flow in the opposite direction, needs to be drawn from the CMOS layer.

In addition to the current level, the impedance of the electrode is also an important consideration. To minimize bleeding in tissue, we use 8.4-μm-diameter CF, with a tapered tip down to 2 μm, as a stimulation electrode [16]. However, even after coating with PtIr, the electrochemical impedance spectroscopy (EIS) measurement results show a high impedance [16].

To determine the best method for stimulation, we considered several approaches and opted for switched-capacitor stimulation (SCS) (see Fig. 4). First, in the case of conventional constant-current stimulation (CCS) [6], [28], [29], it is relatively straightforward to generate the desired pulse shape using a well-defined current source and timing circuitry. However, in high-impedance cases, a high voltage across the electrode interface is required to generate the desired current level. Fig. 5 illustrates a failure case in CCS. Simulations were conducted using a constant phase element (CPE) model fit to the parameters in Fig. 6, and the current was drawn from a storage capacitor precharged at 4.5 V. It shows the voltage development across the electrodes and the stimulation current as we generate biphasic pulses of 40 μA with 200 μs. In this case, as each phase continues, the required applied voltage increases, and eventually, it becomes challenging to maintain a constant current as the transistor of the current source enters the triode region. Due to the non-linear effect of the electrode, the charge delivered in both the phases cannot be the same. This means that CCS not only cannot precisely control the stimulation current but also struggles to achieve CB between the two phases in a high-impedance electrode case.

Second, constant-voltage stimulation (CVS) [8], [9] requires a higher voltage to generate the regulated voltage needed to prevent the same failure mechanism. Therefore, power losses caused by the voltage gap are unavoidable, and the area problem due to increased dc–dc converter stages cannot be resolved in an ultra-small form factor implant.

In comparison, SCS can significantly reduce concerns about electrode impedance because it delivers the stimulation current by simply shorting the charged storage capacitor to the electrode. The only drawback of this stimulation type is that the switching structure can be complex as the stimulation current is delivered in a shape that closely resembles exponential decay. In a state-of-the-art stimulator using SCS [30], this problem is addressed by placing two different storage capacitors, both charged at the same level, and controlling the stimulation phases by alternately connecting them to the electrodes. However, even if the starting values of the storage capacitors are the same, the voltage charged to the electrode capacitor in two phases can differ, requiring a separate charge monitoring circuit for balancing the two phases [30].

We addressed this issue with a proposed automatic termination mechanism for each phase through a dynamic stimulation monitoring circuit. The proposed circuit exhibits two significant novelties: 1) it is designed to use only one storage capacitor which is important in scenarios where the implant volume is extremely limited and 2) it minimizes the power consumption overhead of the monitoring itself using attenuated current instead of direct current copy.

V_{DD} of 1.55 V is first converted to a voltage of 4.3 V through a dc–dc conversion. The converter uses a two-stage conventional cross-coupled charge pump [see Fig. 7(a)]. During stimulation with a charge of 16 nC, to maintain a V_{STORE} drop of less than 1.5 V, for instance, a capacitance of 10 nF or more is required. Implementing this capacitance on-chip would necessitate an area of over 5 mm^2, making it infeasible. Instead, we leverage recent advancements in high-density discrete capacitors, which have increased the capacity of the 008004 footprint capacitor [0.25 mm (L) $\times$ 0.125 mm (W) $\times$ 0.125 mm (T)] from 10 to 100 nF [20]. The output terminal of the dc–dc converter is directly connected to this capacitor.

Note that this capacitor is a type X5R ceramic capacitor, which exhibits nonlinear behavior across different dc bias voltages. In the high-voltage region, the effective capacitance drops to around 20% of the nominal value, which is approximately 20 nF. An illustration of the cycling of the operating points for stimulation during bi-phases with a totaling charge of 32 nC is provided in Fig. 7(b).

The proposed stimulation driver and CB circuit are illustrated in Fig. 8. To alternate the current direction between two phases, an H-bridge switching circuit is implemented using thick-oxide I/O devices whose gates are controlled by level shifters. These level shifters translate the core-voltage control signals to V_{STORE} level. The H-bridge is followed by a tail NMOS diode for the purpose of monitoring I_{STIM}. A charge monitoring circuit mirrors I_{STIM} to a 0.4-pF on-chip

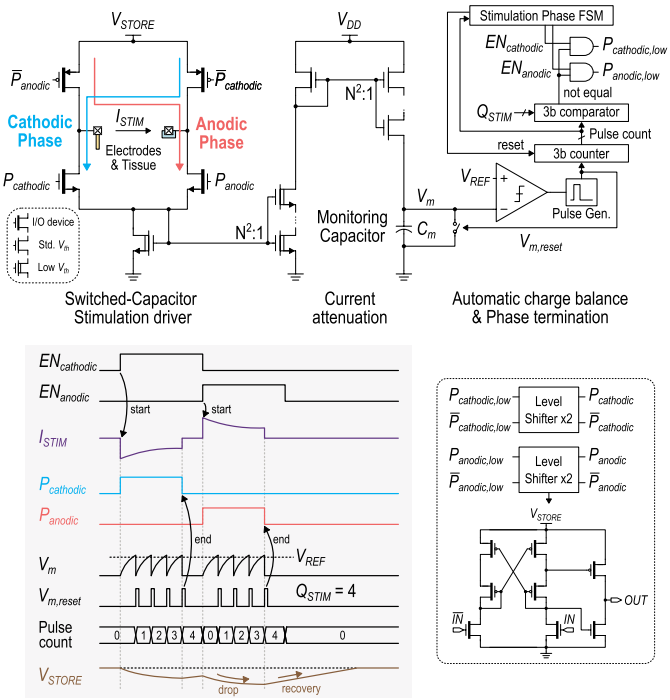
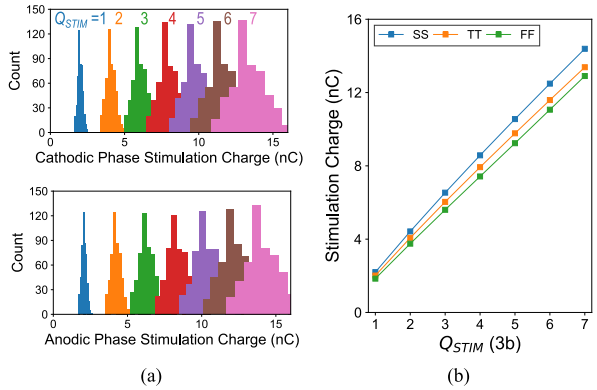


Fig. 8. Proposed stimulation control stages for automatic CB in SCS and their operation.



(a) (b)

Fig. 9. (a) Histogram of the results of a Monte Carlo simulation (500 runs) on stimulation charges during cathodic and anodic phases using the proposed stimulation controller and (b) variations in averaged stimulation charge observed across different corners.

capacitor C_m by dividing it 16.6k times to reduce the on-chip capacitor area and prevents drawing a large current of the same order of magnitude as I_{STIM} from V_{DD}.

When V_m exceeds V_{REF}, C_m is reset by a continuous comparator followed by a pulse generator. The reset pulses are counted and compared with Q_{STIM} to automatically terminate each phase, irrespective of the system clock. When the FSM detects termination, it transitions between cathodic, interphase, anodic, and resting phases, and this cycle repeats.

To analyze the performance of indirect monitoring using attenuated current, a Monte Carlo simulation was conducted. The results demonstrate clear stimulation charge control based on Q_{STIM} [see Fig. 9(a)]. The monitoring current reaching C_m in the proposed CB scheme is determined by the ratio of MOSFETs (N^2:1 or N:1/N), showing effective control capability even under process variation corner cases [see Fig. 9(b)].

B. Optical Receiver

For StiMote's data downlink, modulation light is superimposed onto the ambient light for power transmission. To extract the desired modulation signal, it is crucial to remove the dc component. To address this, we propose an ORX front-end based on a transimpedance amplifier (TIA) that incorporates two closed loops (see Fig. 10).

Given that Manchester encoding, used for data downlink, ensures an equal ratio of 0 and 1 s in all data, we implement the first loop through an ambient light cancellation amplifier. This amplifier averages the modulation signal, facilitating the subtraction of the dc component. During this process, the gate voltage of M4 adjusts in response to the modulation signal, aligning V_{signal} with $V_{\text{signal,ref}}$. Consequently, the dc component of the PD current, I_{ambient}, is subtracted out from the M4 current.

Concurrently, a diode regulation amplifier operates to regulate V_{DIODE} to V_{REF}. In addition, the common-gate amplifier M3 converts the ac component of the PD's current-mode signal, I_{signal}, into a voltage-mode signal, V_{signal}, through the load diode M1. Following this, V_{signal} is input to a dynamic comparator alongside $V_{\text{signal,ref}}$, subjected to 10–20× oversampling using CLK_{OSC}. The comparator output V_{COMP} enters the CDR block, and then the CDR distinguishes the rising and falling transitions of Manchester encoding, leading to the recovery of clock and data appropriately.

The primary determinant of the TIA's speed is the parasitic capacitance of the PD. The bandwidth is dominated by

$$\omega_{\text{TIA}} = \frac{g_{m3}}{C_D} \tag{1}$$

where g_{m3} is the transconductance of M3, and C_D is the parasitic capacitance of the PD. The gain of the proposed TIA is determined by

$$A_{\text{TIA}} = \frac{1}{g_{m1}} \tag{2}$$

where g_{m1} is the transconductance of M1. The proposed TIA has been designed for a gain of 129.1 dBΩ to amplify a PD current-mode signal (10 s of nA) to a voltage-mode signal (10 s of mV) and a bandwidth of 46.8 kHz under C_D of 3.5 pF.

C. Instruction Processor

The state diagram is depicted in Fig. 11(a). The processor listens to serial bits through recovered clock and data signals. Upon encountering the 10-b synchronization preamble code *SYNC*, the processor begins decoding the instruction. The instructions consist of four main types: 1) fire LED; 2) configure chip; 3) update Q_{STIM}; and 4) enable/disable stimulation. The definitions of each instruction packet are provided in Fig. 11(b).

Initially after chip booting, since a large array of chips possess random unique 16-b ID_{CHIP} values [21], self-identification is necessary through the LED. When the decoded instruction is "fire LED," the PD-LED layer switches its mode from PD to LED. The LED packet is then pulse-gap-modulated [31] according to the ID_{CHIP} specified in the instruction, and the LED is activated using the modulated

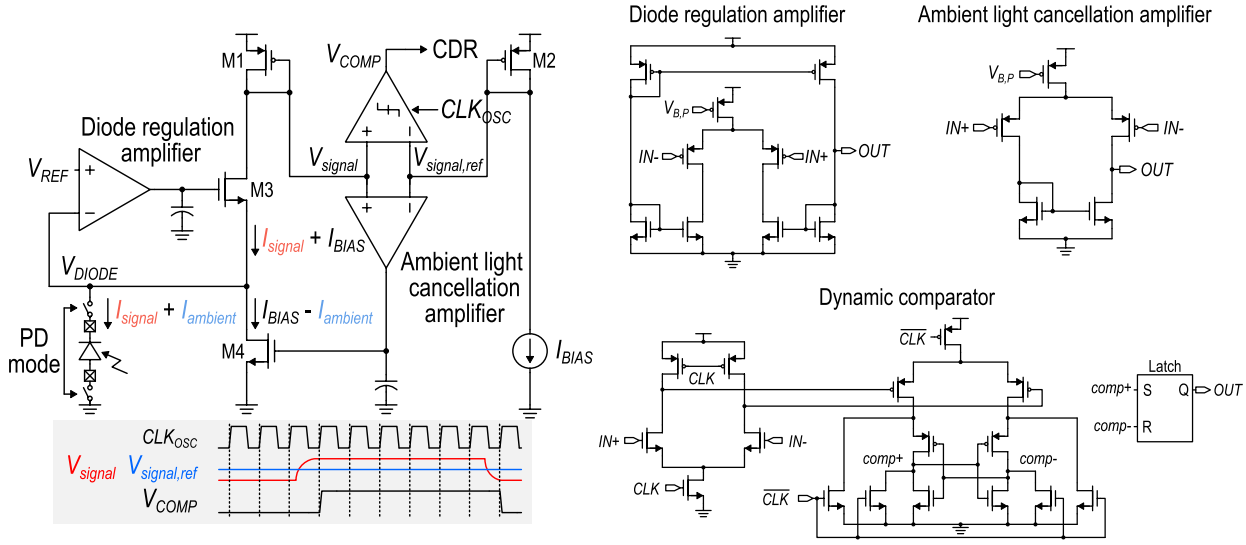
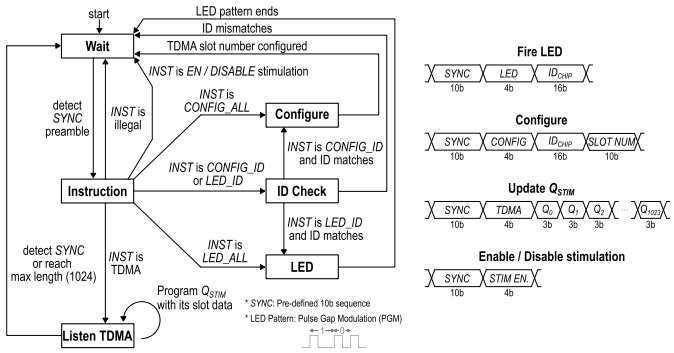


Fig. 10. Schematic of the proposed TIA structure with individual components and its operation for ORX with ambient light cancellation.



(a) (b)

Fig. 11. (a) State diagram of the processor for communication between StiMote and RU. (b) Detailed composition of instruction packets for different operations.

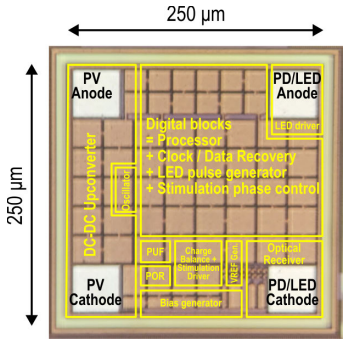


Fig. 12. Die photograph.

pattern. After recognizing the termination of the pattern, the PD-LED returns to the PD mode, and the processor enters the waiting state.

Once the placement of StiMotes in the cortex and the mapping of ID_{CHIP} are completed, the RU assigns a 10-b TDMA slot number to each chip using the *CONFIG* instruction and the following bits. Subsequently, the RU sends repetitive TDMA commands followed by up to 1024 3-b data slots, which update Q_{STIM} of the matched chip. In cases where the number of implanted motes is less than 1024 and an increased array update rate is desired, e.g., from 1024 slots at 2.5 Hz to 625 slots at 4 Hz, the *SYNC* can be transmitted again to early terminate a single TDMA packet. To ensure that *SYNC* does not occur in an actual TDMA data stream, any matching modulation sequence is modified by flipping one LSB of Q_{STIM}, which has a negligible impact on image quality.

The activation and deactivation of stimulation are controlled by independent global enable/disable instructions.

Under the system clock frequency of 150 kHz, the blocks were synthesized by taking into account harsh conditions of the supply variation that can result from the direct power harvesting from the PV cell, without a separate regulator in the system. In addition, to withstand the digital peak currents, special efforts have been devoted to the layout, ensuring an overall V_{DD} decoupling capacitor of 140 pF. The measured PV cell capacitance of 51 pF further contributes to this advantage.

IV. Measurement Results

The proposed CMOS layer of the stimulator mote was fabricated in 180-nm CMOS (see Fig. 12). The components that constitute the StiMote were wire-bonded and subjected to bench-top testing, confirming their full functionality.

A. DC–DC Converter

The output of the dc-dc converter is connected to the storage capacitor, and a dc load sink current is generated using a Sourcemeter (Keithley 2400) and swept to analyze the measured V_{STORE} results as shown in Fig. 13(a). Fig. 13 also includes the power dissipation of both the chip and the load, along with the corresponding calculated efficiency [see Fig. 13(b)]. The power measurement encompasses all other circuits, as their power consumption increases together with the chip frequency. When unloaded, V_{STORE} was measured at 4.33 V with a conversion ratio of 2.79. The power efficiency increases with the load until reaching 2.5 μA, beyond which it decreases due to the decline in V_{STORE}. The maximum efficiency was measured at 67.4% at the on-chip

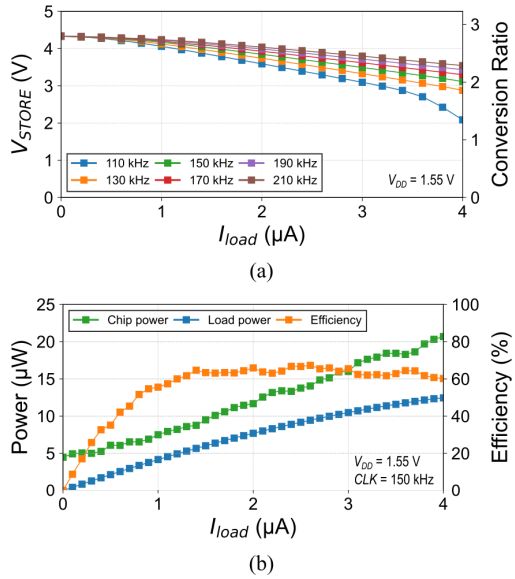


Fig. 13. (a) Measured V_{STORE} with different frequencies and (b) measured chip and load power dissipation with calculated power efficiency across dc load currents of μA range.

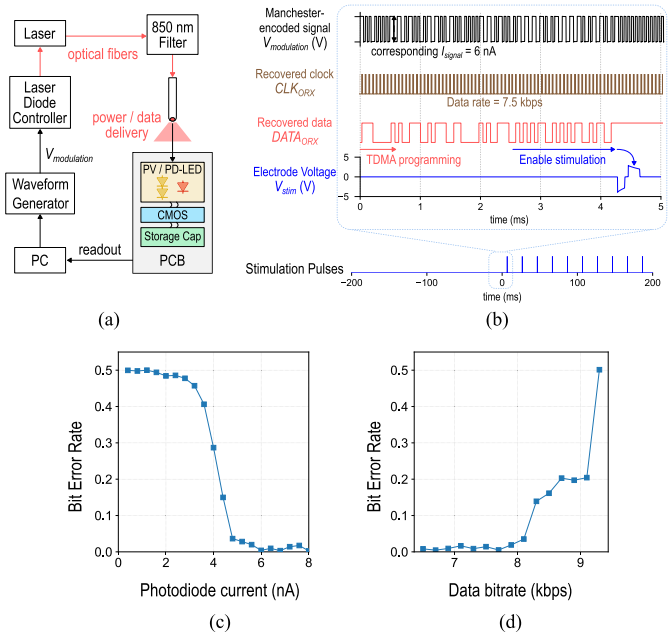


Fig. 14. Measurement results on the optical downlink. (a) Testing setup. (b) Measured waveforms showing an achieved data rate of 7.5 kb/s. (c) Measured BER across different PD currents. (d) Measured BER across different data bitrates.

clock frequency of 150 kHz. Under the nominal bi-phasic charge target of 16 nC with a 50-Hz stimulation frequency, translated to I_{load} of 0.8 μA, the chip exhibited an overall power consumption of 6.54 μW, a load power of 3.38 μW at V_{STORE} of 4.22 V, and an efficiency of 51.6%.

B. Optical Testing

Optical testing was conducted using an 850-nm laser diode source, diode controller, and an arbitrary waveform generator for modulating diode current, as depicted in Fig. 14(a). The CMOS layer exhibited full functionality when operated entirely wirelessly through harvested light.

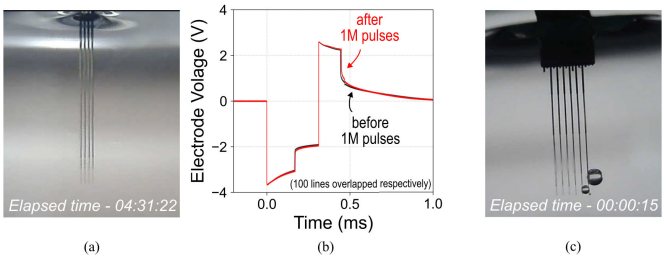


Fig. 15. In vitro measurements demonstrating (a) absence of bubble formation with the proposed CB circuit, (b) comparison of electrode voltage transients before and after the 1 million pulse test in saline showing no significant charge accumulation at electrode interface, and (c) rapid occurrence of bubble formation with the direct application of dc voltage.

In this study, measurements were conducted using the current proof-of-concept custom PV cell (200 × 200 μm^2), which has a smaller form factor than the StiMote chip. Work is currently underway to develop a new PV cell that aligns with the StiMote chip's form factor 250 × 250 μm^2 [see Fig. 2(a)]. For the current experiment, the anticipated future increase of 1.6 times in the PV cell active area was considered. Therefore, the results are presented based on an irradiance of 750 /mm^2, approximately 1.6 times the NIR limit of 475 /mm^2. This test condition represents the expected equivalent increase in power generation of the PV cell due to increased active area for the StiMote chip at the maximum irradiance limit.

The data downlink achieved a data rate of 7.5 kb/s with a PD current I_{signal} of 6 nA. Fig. 14(b) illustrates the effective recovery of both clock and data through laser irradiance modulation. At the captured time, it demonstrates the activation of StiMote's crucial function, stimulation, via measured waveforms resulting from light-based instructions. Fig. 14(c) and (d) illustrates how the bit error rate (BER) of the recovered data changes with the PD current and modulation data bitrate, respectively. For PD currents above 6 nA and modulation data bitrates up to 7.5 kb/s, the BER was below 2%, which is acceptable for StiMote application.

C. Stimulation and Charge Balance Characteristics

To assess the performance of the proposed CB circuit in vitro, 1 million pulses, each with a charge of 16 nC for both the phases (twice the nominal stimulation charge) and a stimulation frequency of 50 Hz, were applied to a PtIr-CF electrode immersed in saline solution. While voltage transients were consistently observed, no bubble formation was detected in the captured video footage [see Fig. 15(a)], and recorded voltage transients across electrodes before and after the test showed no significant changes [see Fig. 15(b)]. Post-experiment impedance measurements of the electrodes confirmed their integrity. In contrast, when the same 4.5 V was applied as a dc voltage, bubble formation was immediately observed at the CF tip within a matter of seconds [see Fig. 15(c)].

The bench-top measurement results illustrate the exponentially decaying transient pulse shape characteristic of the stimulation via the SCS method [see Fig. 16(a)]. The stimulation charge measured at each Q_{STIM} was linearly controlled according to the operational principle of the CB

TABLE I
COMPARISON TABLE

		This Work	JSSC '14 [28]	ISSCC '16 [6]	ISSCC '18 [7]	CICC '18 [8]	ISSCC '20 [29]	ISSCC '20 [32]	JSSC '21 [9]	JSSC '22 [10]
Application target		**Brain (Visual Cortex)**	Retinal	Spinal Cord	Brain	PNS	Subretinal	Subretinal	Epiretinal	Spinal Cord, Cardiac
Power / Data downlink		**Optical**	Inductive	Inductive	Inductive	Ultrasonic	- / Optical	RF / Optical	Optical	Magnetoelectric
Process		**180 nm**	65 nm	180 nm HV	350 nm	65 nm	180 nm	180 nm	65 nm LP	180 nm
Implant volume (mm^3)		**0.02**	-	500	12.15	6.5	-	-	-	6.2
Chip area (mm^2)		**0.0625**	8	25.1	1	0.06	17.25	5	8.68	0.8
External components		**1 Cap 1 PV/PD-LED**	3 Cap	6 Cap 2 Coil	4 Cap 1 Coil	1 Cap 1 Piezo	-	1 Coil	1 Crystal, 1 PV, 1 RF TX, 3 Cap	1 Cap 1 ME Film
Multiple access		**Yes**	No	No	No	No	No	No	No	Yes
Stimulation	Supported number of stimulation sites	**1024**	1	1	1	1	1	1	1	128
	Stimulation Channels per chip	**1**	256	160	16	1	1225	1512	288	1
	Stimulation Shape	**Biphasic**	Biphasic	Biphasic	Monophasic	Monophasic	Biphasic	Biphasic	Biphasic	Biphasic
	Stimulation Type	**Switched Cap. Current**	Constant Current	Constant Current	Switched Cap. Optical	Constant Voltage	Constant Current	Constant Voltage	Constant Voltage	Adaptive Constant Voltage
	Max. stimulation frequency	**50 Hz**	60 Hz	20 kHz	10 Hz	2 kHz	-	-	-	1 kHz
	Max. stimulation amplitude	**0.4 mA**	0.465 mA	0.5 mA	10 mA	0.4 mA	1 mA	3 mA	0.255 mA	3.5 V
	Stimulation resolution (bit)	**3**	5 + 8	7	2 + 2	3	3	-	8	4 + 4 + 9
Power w/o stimulation (μW)		**5.5**	10000	864	300	4	-	-	3100	9
Supply voltage (V)		**1.55**	3.3	±6 – ±12	1.8	2.5	-	0.5 - 3	3.1 – 3.6	1.5 – 3.5
Max Data rate		**7.5 kbps**	600 kbps	2 Mbps	50 kbps	-	-	100 bps	2 Mbps	5.16 kbps

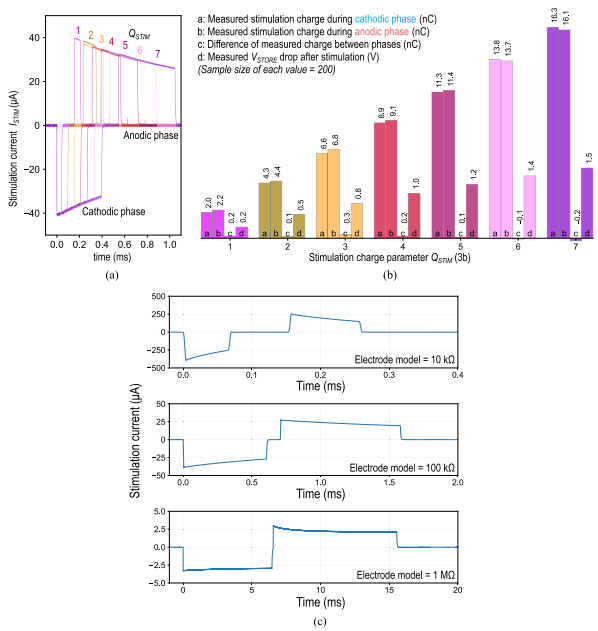


Fig. 16. (a) Measured waveforms, (b) CB characteristics including integrated charge during each phase for different Q_{STIM} with a 100-kΩ electrode model, and (c) stimulation pulse shapes measured with different electrode models showing different peak currents and time span.

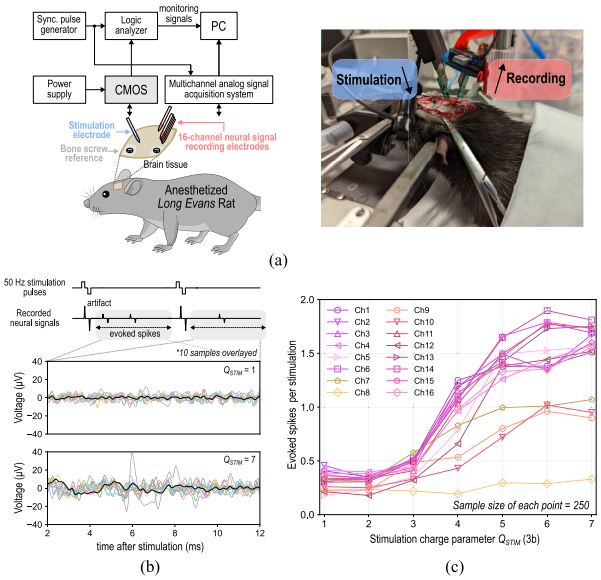


Fig. 17. (a) In vivo testing setup, (b) evoked neural signals after a stimulation pulse, and (c) average evoked spikes per stimulation across different Q_{STIM} for 16 recording electrodes.

circuit, and the charge mismatch was also minimal, below 0.2 nC [see Fig. 16(b)]. At the highest Q_{STIM}, a charge of 16 nC was injected for each stimulation phase, resulting in a measured voltage drop of 1.5 V in the final V_{STORE}. Fig. 16(c) demonstrates that the proposed CB circuit operates effectively across a wide impedance range, from 10 kΩ to 1 MΩ, showing the versatility of the SCS approach.

D. In Vivo Measurement

All the animal procedures were approved by the University of Michigan Institutional Animal Care and Use Committee. In an anesthetized male Long Evans rat, visual cortex was exposed by craniotomy and two CF electrode arrays [33] with small-site sharpened tips [16] were implanted. On one array, a PtIr-CF electrode wire-bonded to the StiMote CMOS chip (see Fig. 17) applied stimulation. On the other array, 16 other PtIr-CF electrodes were positioned in close proximity to

record neural signals using a wireless headstage (multichannel systems). Stimulation was applied at a frequency of 50 Hz. Within a stimulation window lasting 20 ms, the initial 2 ms following stimulation was omitted to remove any potential artifacts. The subsequent 18 ms was analyzed for the presence of evoked neural spikes across all the recording channels and Q_{STIM} levels. We first recorded signals for seconds before the stimulation was applied, calculated the standard deviation of the channel individually, and then recorded signals during the stimulation. Any spikes exceeding three times the previously calculated standard deviation were counted as evoked spikes. A clear and consistent increase in the count of evoked spikes per stimulation demonstrates compelling evidence for the effectiveness of the stimulation in activating local neuron in visual cortex.

V. Conclusion

This article introduces StiMote, a free-floating stimulator mote with a form factor of 0.02 mm^3. The proposed ORX successfully recovered Manchester-encoded signals corresponding to PD currents of 6-nA amplitude. The received signals were accurately decoded, enabling functions such as mote assignment to specific TDMA slots and updating stimulation charge parameters. This verification was achieved at a data rate of 7.5 kb/s. The implemented dc–dc converter boosted V_{DD} voltage of 1.55 V to 4.3 V for V_{STORE}, achieving a maximum load to chip power efficiency of 67.4%. In this study, we proposed an automatic phase termination technique through a monitoring circuit for SCS. The proposed technique demonstrated linearity in stimulation charge control across seven levels ranging from 2 to 16 nC, achieving CB with differences of less than 0.2 nC. The effectiveness of the proposed stimulation system is confirmed through in vivo testing. A comparison with other state-of-the-art wireless stimulation approaches is provided in Table I. In the future, we anticipate the complete integration of the implantable floating mote with the proposed system and components, enabling true wireless long-term deep brain stimulation for visual prostheses.

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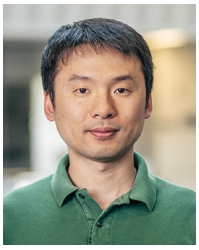

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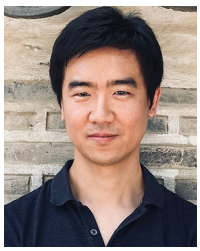
He was a Post-Doctoral Researcher with the Chestek Laboratory, University of Michigan, from 2015 to 2019, and continued in the same laboratory as an Assistant Research Scientist from 2019 to 2022. His primary research focus was to develop, test, and oversee the distribution of high-channel-count carbon fiber electrode arrays capable of electrophysiological or dopaminergic recordings.

Dennis Sylvester (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 1999, where his dissertation was recognized with the David J. Sakrison Memorial Prize as the most outstanding research in the UC-Berkeley EECS Department.

He is currently the Edward S. Davidson Collegiate Professor and the Interim Chair of electrical and computer engineering at the University of Michigan, Ann Arbor, MI, USA, and was the Founding Director of the Michigan Integrated Circuits Laboratory (MICL), a group of ten faculty members and 70+ graduate students. He has held research staff positions at the Advanced Technology Group, Synopsys, Mountain View, CA, USA, and Hewlett-Packard Laboratories, Palo Alto, CA, USA, and a Visiting Professorship at the National University of Singapore, Singapore, and Nanyang Technological University, Singapore. He has authored more than 550 articles along with one book and several book chapters. He holds 51 U.S. patents. He co-founded Ambiq, Austin, TX, USA, a fabless semiconductor company developing ultralow-power mixed-signal solutions for compact wireless devices. His research interests include design of millimeter-scale computing systems and energy-efficient near-threshold computing.

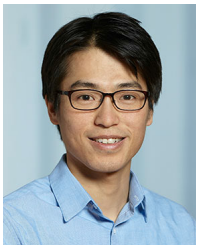
Dr. Sylvester is a fellow of the National Academy of Inventors. He received the NSF CAREER Award, the Beatrice Winner Award at ISSCC, the IBM Faculty Award, the SRC Inventor Recognition Award, and 16 best paper awards and nominations. He was named a top 5 Contributing Author all-time at ISSCC in 2023 and the most prolific author at the IEEE Symposium on VLSI Circuits, and received the University of Michigan Henry Russel Award for distinguished scholarship. He is the current Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He previously served on the Administrative Committee for the IEEE Solid-State Circuits Society, was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (CAD), and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and served as an IEEE Solid-State Circuits Society Distinguished Lecturer.



Hun-Seok Kim (Senior Member, IEEE) received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2001, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2010.

He is currently an Associate Professor with the University of Michigan, Ann Arbor, MI, USA. His research focuses on system analysis, novel algorithms, and VLSI architectures for low-power/high-performance wireless communications, signal processing, computer vision, and machine learning systems.

Dr. Kim was a recipient of the DARPA Young Faculty Award in 2018 and the National Science Foundation (NSF) CAREER Award in 2019. He is an Associate Editor of the IEEE TRANSACTIONS ON MOBILE COMPUTING.



Taekwang Jang (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2006 and 2008, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2017. His Ph.D. dissertation was titled "Circuit and System Designs for Millimeter-Scale IoT and Wireless Neural Recording."

From 2008 to 2013, he worked at Samsung Electronics Company Ltd., Yongin, South Korea, focused on mixed-signal circuit design, including analog and all-digital phase-locked loops for communication systems and mobile processors. After working as a Post-Doctoral Research Fellow at the University of Michigan, he joined ETH Zürich, Zürich, Switzerland, in 2018, as an Assistant Professor and he is leading the Energy-Efficient Circuits and Intelligent Systems Group. He holds 15 patents and has (co)authored more than 80 peer-reviewed conference papers and journal articles. His research focuses on circuits and systems for highly energy-constrained applications such as wireless sensor nodes and biomedical interfaces. Essential building blocks such as a sensor interface, energy harvester, power converter, communication transceiver, frequency synthesizer, and data converters are his primary interests.

Dr. Jang is a member of the Competence Center for Rehabilitation Engineering and Science and the Chair for the IEEE Solid-State Circuits Society, Switzerland Chapter. Since 2022, he has been a TPC Member of the IEEE International Solid-State Circuits Conference (ISSCC), IMMD Subcommittee, and the IEEE Asian Solid-State Circuits Conference (ASSCC), Analog Subcommittee. He is the recipient of the 2024 IEEE Solid-State Circuits Society New Frontier Award, the 2022 SNSF Starting Grant, the IEEE ISSCC 2021 and 2022 Jan Van Vessem Award for Outstanding European Paper, the IEEE ISSCC 2022 Outstanding Forum Speaker Award, and the 2009 IEEE CAS Guillemin-Cauer Best Paper Award. He also chaired the 2022 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Frequency Generation Subcommittee. He has been an Associate Editor of the *Journal of Solid-State Circuits* (JSSC) since 2023.

Jamie D. Phillips (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1994, 1996, and 1998, respectively.

He was a Post-Doctoral Researcher at Sandia National Laboratories, Albuquerque, NM, USA, from 1998 to 1999 and a Research Scientist at the Rockwell Science Center, Thousand Oaks, CA, USA, from 1999 to 2001. He joined the faculty of the Electrical Engineering and Computer Science Department, University of Michigan, in 2002, where he was an Arthur F. Thurnau Professor. He joined the University of Delaware, Newark, DE, USA, in 2020, as a Professor and the Chair of the Department of Electrical and Computer Engineering. His technical interests and contributions are in the area of compound semiconductor materials and optoelectronic devices. He has authored more than 150 peer-reviewed journal articles on these subjects.

Dr. Phillips is a fellow of Optica. He received the NSF CAREER Award in 2003 and the DARPA MTO Young Faculty Award in 2007. He currently serves as an Associate Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES and the Chair for the IEEE Electron Devices Society Optoelectronics Technical Committee.

Cynthia A. Chestek (Senior Member, IEEE) received the B.S. and M.S. degrees from Case Western Reserve University, Cleveland, OH, USA, in 2005, and the Ph.D. degree from Stanford University, Stanford, CA, USA, in 2010, all in electrical engineering.

She is currently an Associate Professor of biomedical engineering with the University of Michigan, Ann Arbor, MI, USA, where she joined the faculty in 2012. She runs the Cortical Neural Prosthetics Laboratory, Ann Arbor, which focuses on brain and nerve signals from implantable electrodes to control precise hand movements. Her laboratory also develops carbon fiber electrodes smaller than neurons that could enable even higher density interfaces to the nervous system. She has authored 89 full-length manuscripts and has advised 19 Ph.D. students.

James Weiland (Fellow, IEEE) received the B.S. degree in electrical engineering, the M.S. degrees in biomedical engineering and electrical engineering, and the Ph.D. degree in biomedical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1988, 1993, 1995, and 1997, respectively.

He spent four years in the industry with Pratt & Whitney Aircraft Engines. He joined the Wilmer Ophthalmological Institute, Johns Hopkins University, Baltimore, MD, USA, in 1997, as a Post-Doctoral Fellow. In 1999, he was appointed as an Assistant Professor of ophthalmology at Johns Hopkins University. He was appointed as an Assistant Professor at the Doheny Eye Institute-University of Southern California, Los Angeles, CA, USA, in 2001 and was promoted as the Professor of ophthalmology and biomedical engineering in 2013. In 2017, he was appointed as a Professor of biomedical engineering (medical school) and ophthalmology and visual sciences at the University of Michigan. He has more than 100 peer-reviewed articles. His research interests include retinal prostheses, neural prostheses, electrode technology, visual evoked responses, implantable electrical systems, and wearable visual aids for the blind.

Dr. Weiland is a fellow of the American Institute of Medical and Biological Engineering.

David Blaauw (Fellow, IEEE) received the B.S. degree in physics and computer science from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree in computer science from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 1991.

Until August 2001, he worked for Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology Group and received the Motorola Innovation Award. Since August 2001, he has been on the faculty of the University of Michigan, Ann Arbor, MI, USA, where he is currently the Kensall D. Wise Collegiate Professor of EECS. He has authored more than 600 articles, has received numerous best paper awards, and holds 65 patents. He has researched ultralow-power wireless sensors using subthreshold operation and low-power analog circuit techniques for millimeter systems. This research was awarded the MIT Technology Review's "One of the Year's Most Significant Innovations." His research group introduced the so-called near-threshold computing, which has become a common concept in semiconductor design. Most recently, he has pursued research in cognitive computing using analog, in-memory neural networks for edge devices and genomics for precision health.

Dr. Blaauw received the 2016 SIA-SRC Faculty Award for lifetime research contributions to the U.S. semiconductor industry. He was the General Chair for the IEEE International Symposium on Low Power and a member of the IEEE International Solid-State Circuits Conference (ISSCC) Analog Program Subcommittee.