An Ultralow-Power Triaxial MEMS Accelerometer With High-Voltage Biasing and Electrostatic Mismatch Compensation

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***Abstract*— This article presents a triaxial microelectromechanical system (MEMS) capacitive accelerometer using a high-voltage biasing technique to achieve high resolution with ultralow power. The accelerometer system generates a differential pair of high voltages to bias the MEMS structure, raising the MEMS signal substantially above the noise floor of the analog front-end (AFE) circuits. With the consequent increased signal-to-noise ratio (SNR), the proposed accelerometer system eliminates the need for a power-hungry low-noise amplifier (LNA) and signal chopping which significantly improves the power-noise tradeoff found in conventionally biased MEMS accelerometers. Moreover, by fine-tuning the bias voltages, the proposed method cancels the electrostatic mismatch in the MEMS due to process variation and ensures robust operation. The proposed accelerometer is composed of one integrated MEMS-CMOS chip and one CMOS-only chip. In postfabrication testing, it achieves a 121-μg/$\sqrt{\text{Hz}}$ input-referred noise floor with ±1.5-g dynamic range, <1% linearity error, and 184-nW per-axis power (including high-voltage bias generation). Compared to prior art, the design achieves a 10.3× FoM improvement in both power and noise specifications.**

***Index Terms*— Accelerometer, analog-front-end (AFE), electrostatic force, high-voltage generation, low-noise amplifier (LNA), low-power circuit, microelectromechanical system (MEMS).**

I. Introduction

MICROELECTROMECHANICAL system (MEMS) capacitive accelerometers have become increasingly popular in motion detection (MD) applications such as object monitoring, gesture recognition, and tilt control [1], [2]. Consisting of a micromechanical spring-mass system, MEMS capacitive accelerometers are capable of high acceleration sensitivity while maintaining good linearity, low Brownian (mechanical) noise, and good temperature consistency, all within a miniaturized volume. An analog front-end (AFE) interface circuit is required to amplify the signals generated by the MEMS sensing elements before they can be read out and utilized by other circuits such as analog-to-digital converters (ADCs).

In all capacitive MEMS accelerometers, there is a fundamental tradeoff between the acceleration resolution and readout power consumption, limiting their use to either applications that require high resolution and can accommodate a high power budget [3], [4], [7], [8], or applications where resolution can be sacrificed to accommodate a low power budget [9], [10], [11], [12]. This tradeoff stems from the inverse relationship between AFE noise and power. High-resolution accelerometers require an ultralow noise floor for their AFE circuit so that the signal-to-noise ratio (SNR) does not limit the overall resolution. As a result, low-noise amplifiers (LNAs) and signal chopping techniques are required to reduce thermal noise and flicker noise, respectively, creating a tradeoff between the benefit they provide and the circuit power required for their operation. For a typical accelerometer achieving a resolution of <1 mg with a power consumption of <1 μW remains challenging. For even higher resolution (μg levels), prior works adopt feedback from the AFE output to the MEMS structure [13], [14] to further reduce Brownian noise, or utilizing noise reduction techniques such as oversampling successive approximation [15], correlated double amplifying [16] and closed-Loop hybrid dynamic amplifier [17]. These approaches achieve low noise specification with wide bandwidth and large input acceleration range but require higher power for the front-end circuit and dynamic excitation.

One way to address the resolution-power dilemma is to increase the signal (VIN) directly generated by the MEMS. Instead of reducing the AFE/MEMS noise and accepting the associated AFE power overhead, increasing the sensitivity of the MEMS signal so that it produces a larger signal with the same acceleration would improve the SNR and accelerometer resolution. An increase in MEMS signal sensitivity can be achieved by either: 1) increasing the MEMS sensitivity, such as increasing proof mass or reducing spring stiffness and

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2) increasing the MEMS electrical signal with a higher MEMS bias voltage. The first class of approaches requires redesigning the MEMS structure [18] with the cost of the high-shock survivability and sensing capability (dynamic range). The second approach can be implemented completely in the electrical domain, but it has its own challenges associated with the high power consumption, reliability, and electrostatic feedback to the MEMS sensing element [19], [20]. To address these challenges, we present a triaxial MEMS capacitive accelerometer [21], consisting of one MEMS chip and two CMOS chips, with the following advantages.

1) The proposed accelerometer adopts a >10× higher MEMS bias compared to a conventional biasing scheme, resulting in a >40× larger MEMS signal. Because of the large MEMS signal and nonchopping operation, this approach significantly relaxes the noise and bandwidth requirement for AFE circuits, making it possible to achieve 1-mg sensitivity with nW level power consumption for the first time.
2) We describe an electrostatic mismatch compensation (EMC) technique in this article that addresses the electrostatic feedback from the high-voltage bias to the MEMS structure. It guarantees optimal MEMS biasing, thereby ensuring sufficient dynamic range while compensating for process variation during the MEMS fabrication.
3) The high-voltage bias generation with EMC is implemented with a high-voltage companion (HVC) chip that only consumes sub-μW and generates $\pm$ >40-V bias voltage with <0.1% errors/ripples. The AFE circuit is also customized with ultralow-power amplifier designs and high-voltage protection techniques for robustness with high bias voltage. We perform measurements for multiple chip samples (from different wafers) and validate their functionality, performance, and robustness.

The remainder of this article is organized as follows. Section II presents the advantages and challenges of using a high bias for an MEMS a capacitive accelerometers and the analysis of EMC. Sections III and IV describe the implementation of the HVC chip and the MEMS-CMOS AFE chip, respectively. Section IV shows the measurement results of the proposed accelerometer system. Section V presents our conclusions.

II. Proposed High-Voltage MEMS Biasing With EMC

A. Overview of the MEMS Capacitive Accelerometer

The sensing element of an MEMS capacitive accelerometer is a micromechanical structure consisting of fixed electrodes and movable proof masses. As shown in Fig. 1(a) as a simplified diagram, both the electrodes and the proof masses have multiple fingers that interleave with each other, forming a coupling capacitance network between the fingers. When an acceleration occurs, the proof-mass fingers deflect from their initial position while the electrodes stay stationary (relative to the substrate), changing the gap distance between them and causing a capacitance change that can be detected to determine the acceleration amount. A fully differential MEMS capacitive accelerometer that consists of two proof masses and two electrodes. The proof-masses are anchored to the substrate via the spring, and their displacement x under the acceleration a can be expressed as

$$\frac{dx}{da} = \frac{m}{k_m} = \frac{1}{\omega^2} \tag{1}$$

where m represents the proof mass, k_m is the spring constant of the spring, and ω is the fundamental frequency of this mechanical system, which determines the bandwidth of the MEMS sensing element. The proof-mass displacement causes the capacitance change of C_1 and C_2 between itself and two neighboring electrode plates, as shown in Fig. 1(b). The values of C_1 and C_2 are expressed as follows:

$$C_1 = \frac{\varepsilon_0 A}{g_0 - x} \quad C_2 = \frac{\varepsilon_0 A}{g_0 + x} \tag{2}$$

where ε_0 is the permittivity of vacuum, A is the area of parallel plates, and g_0 is the initial gap distance between the centered proof mass and the electrodes. Taking C_1 as an example, its capacitive sensitivity to displacement can be derived as

$$\frac{dC_1}{dx} = \frac{\varepsilon_0 A}{(g_0 - x)^2}. \tag{3}$$

Combining (1) and (3), we obtain the MEMS sensitivity to the acceleration as

$$\frac{dC_1}{da} = \frac{dC_1}{dx}\frac{dx}{da} = \frac{m\varepsilon_0 A}{k_m (g_0 - x)^2}. \tag{4}$$

To maintain good linearity in sensing accelerations, the MEMS is usually designed with $x \ll g_0$, and both C_1 and C_2 will have constant sensitivities within the accelerometer measurement range

$$\frac{dC_1}{da} = \frac{dC_2}{da} = \frac{m\varepsilon_0 A}{k_m {g_0}^2}. \tag{5}$$

A fully differential MEMS structure shown in Fig. 1(b) produces two pairs of C_1 and C_2 with the opposite sensitivity for accelerations. They are configured as a capacitive Wheatstone bridge that has 2× the MEMS sensitivity compared with a single-ended sensing element.

B. Motivation for High-Voltage MEMS Biasing

To convert the MEMS capacitance change into a signal that is convenient for readout, the MEMS is usually biased with a voltage V_B so that it produces an electrical voltage that reflects the MEMS acceleration. Fig. 2(a) shows a conventional MEMS capacitive accelerometer with V_B applied across the electrode side (EL1 and EL2) and the voltage signal V_{IN} read out from the proof masses (PM1 and PM2). The output voltage sensitivity of the Wheatstone bridge is defined by

$$\frac{dV_{\text{IN}}}{dC} = \frac{V_B}{C_d + C_{\text{par}}} \tag{6}$$

where $C_d = \varepsilon_0 A / g_0$ is the static capacitance of C_1 and C_2 without any accelerations, and C_{par} is the parasitic capacitance between the proof mass and the substrate. Combining (5) and (6), we obtain the MEMS signal sensitivity in the electrical domain

$$\frac{dV_{\text{IN}}}{da} = \frac{dV_{\text{IN}}}{dC}\frac{dC}{da} = \frac{m\varepsilon_0 A V_B}{k_m {g_0}^2 (C_d + C_{\text{par}})}. \tag{7}$$

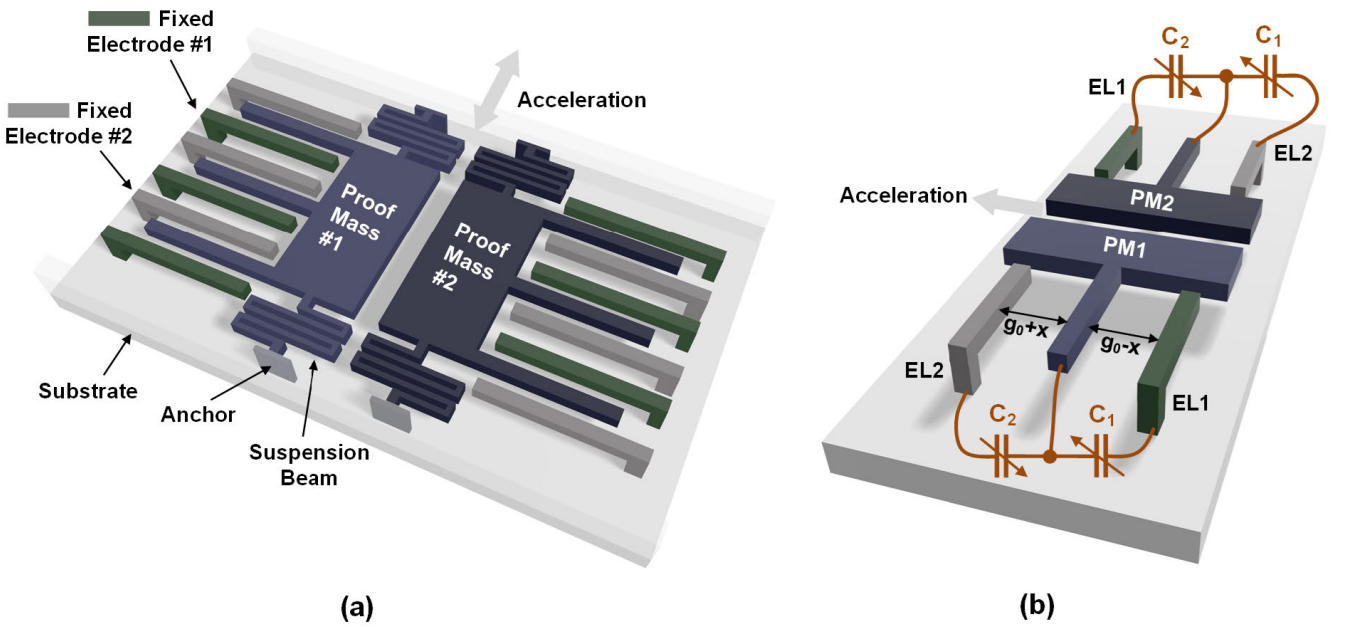

Fig. 1. (a) Simplified diagram of a fully differential MEMS capacitive accelerometer. (b) Zoomed-in diagram showing the coupling capacitance between the MEMS-proof masses and electrodes.

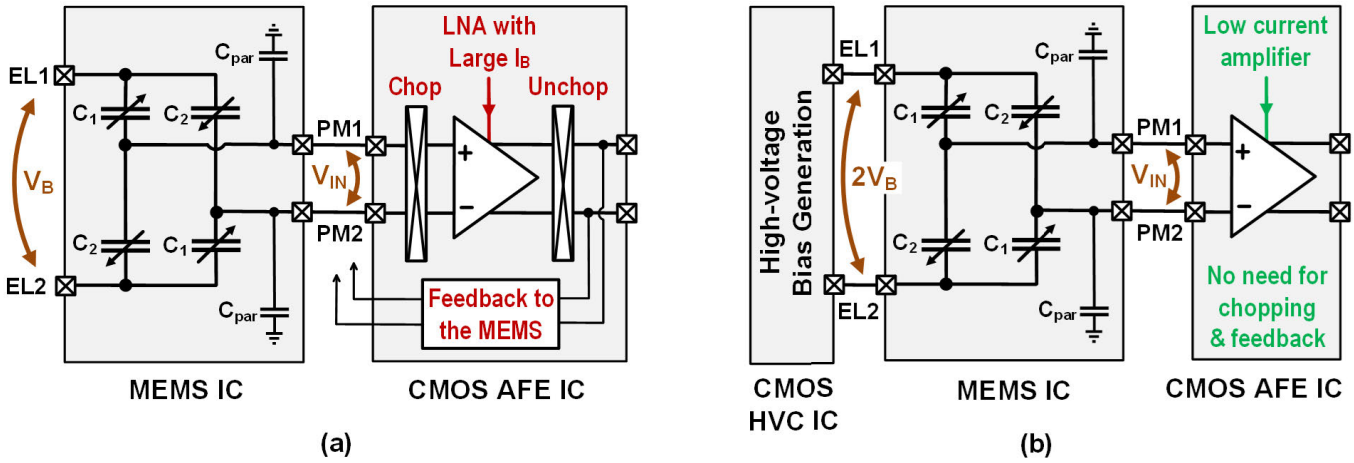

Fig. 2. (a) Conventional scheme for reading out sensing signals from the MEMS capacitive accelerometer. (b) Proposed high voltage biasing scheme that increases the MEMS signal and relaxes the AFE noise requirement for low power operation.

All the right terms in (7) are constant, indicating a linear transformation from input accelerations to the voltage signals produced by the MEMS device. However, the linearity largely depends on the assumption made in (5), that is, that the MEMS displacement is negligible compared to the gap distance, indicating a small MEMS signal amplitude in the μV to mV range. The small signal needs to be conditioned and amplified by the AFE before it can be processed by other circuits (e.g., ADCs). While amplifying the MEMS signals, the AFE circuit also induces electrical noise that adds to the mechanical noise (known as Brownian noise [22]) originating from the MEMS-proof mass.

Fig. 2(a) shows a conventional readout approach for an MEMS capacitive accelerometer, which includes three AFE techniques from prior works to improve the SNR. First, an LNA with a large bias current is necessary in high-resolution accelerometer designs to suppress the in-band thermal noise from transistors and other circuit components. Second, signal chopping is used either at the MEMS bias node or at the amplifier input to reduce the flicker noise that dominates in the low-frequency domain. The MEMS signal is chopped with a higher frequency than that of the input acceleration, and it is later unchopped to be recovered after the AFE circuit. The chopping operation results in large power overhead due to the higher bandwidth requirement for the amplifiers, and also due to the excessive switching loss and the chopped nodes. Third, to further reduce the accelerometer noise floor to ng levels, feedback is used to control the proof-mass displacement. However, all of these techniques require extra power, so there is a tradeoff between the accelerometer resolution and power consumption, which is consistent with the fundamental tradeoff between the AFE

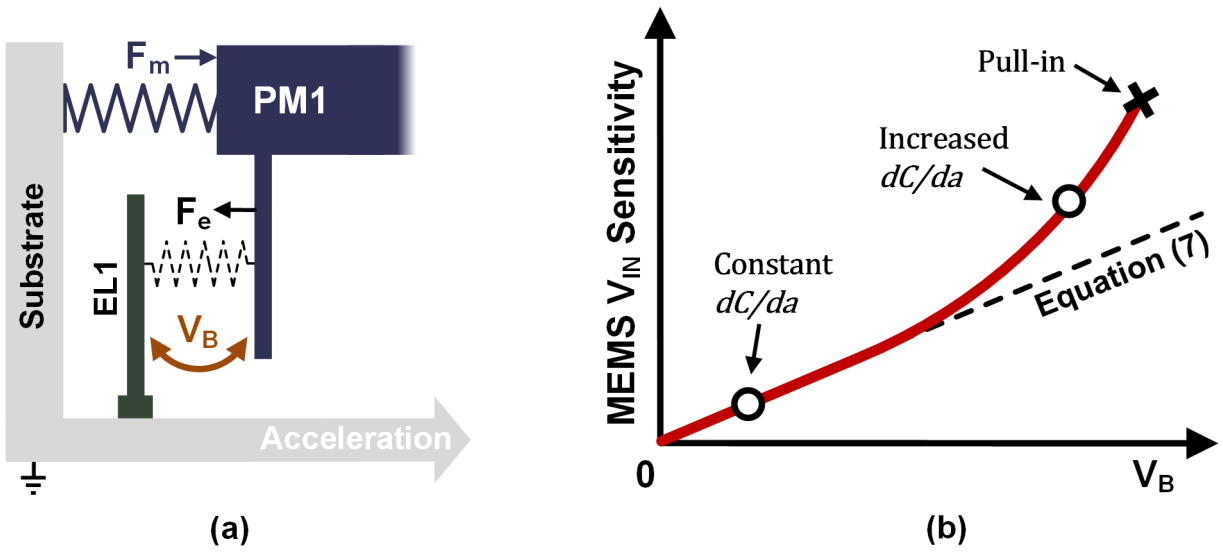

Fig. 3. (a) Stress analysis of the proof mass when considering both mechanical forces F_m and electrostatic force F_e. (b) With a fixed acceleration, the change of MEMS signal V_{IN} with increasing bias voltage V_B.

noise and power. In power-constrained applications such as IoT devices, it, therefore, remains challenging for MEMS capacitive accelerometers to achieve a sub-mg sensitivity with μW-level power consumption.

To overcome this power-noise dilemma, we propose to increase the MEMS signal rather than reduce the noise. From (7), we know that the MEMS signal sensitivity is related to two factors: 1) the capacitive sensitivity to accelerations and 2) the bias voltage being applied on the MEMS. The capacitive sensitivity, as explained earlier, is related to Brownian noise and the linearity of the MEMS design and, thus, is difficult to improve. Instead, using higher bias voltages is the better solution because it can increase the MEMS signal proportionally without changing the MEMS structure. Fig. 2(b) shows the proposed high-voltage biasing scheme for the MEMS capacitive accelerometer. By applying a significantly higher bias voltage (e.g., 10×) than that in a conventional MEMS accelerometer design, the MEMS signal is raised 10× before it hits the input of CMOS AFE. Targeting the same SNR, the 10× MEMS signal lowers the requirement for the AFE input-referred noise, effectively reducing the AFE amplifier's bias power by 100×. Moreover, the increased MEMS signal also lowers the flicker noise requirement and makes it possible to eliminate signal chopping. The nonchopping scheme eliminates the switching loss and it also relaxes the bandwidth requirements for the AFE, which further reduces overall power. Wrapping this all up, we were able to design the AFE with a nano-amp bias current while still maintaining a good SNR with the high-voltage MEMS bias.

Compared to the conventional scheme, the high-voltage biased MEMS accelerometer overcomes the conventional tradeoff between AFE power and noise. Instead, its power-resolution performance is determined by what voltage level is applied to the MEMS for a given power budget. Some of the prior works also utilized a high-than-usual (e.g., 7 V in [4] and 12 V in [8]) drive voltage for MEMS sensing element, but this article first proposes a complete mechanism to generate 10× higher differential bias voltages on the chip and balance the electrostatic mismatch effect with a nano-watt level power overhead. Section III introduces the details about our implementation, but before presenting those circuit details, we first explain the impact of electrostatic feedback, which determines the upper limit of the MEMS bias voltage in a more fundamental way.

C. Electrostatic Feedback of the High-Voltage Biasing

As discussed in Section II-B, one can, in principle, achieve an almost infinite signal gain by applying an extremely high voltage to the MEMS. However, the benefit of high-voltage bias is less straightforward when considering the impact of bias voltage on the MEMS's mechanical movement. The large voltage stress across the proof mass and electrodes generates an electrostatic force between them and results in an additional movement of the proof mass. To quantitatively analyze the impact of the electrostatic force, we again take C_1 as an example to calculate the force between PM1 and EL1, as shown in Fig. 3(a). When a bias voltage V_B is applied across them, the total energy stored in C_1 is expressed by

$$E = C_1 {V_B}^2. \tag{8}$$

The electrostatic force F_e between PM1 and EL1 can be derived by

$$F_e = \frac{dU}{dx} = \frac{dC_1}{dx} {V_B}^2 = \frac{\varepsilon_0 A {V_B}^2}{(g_0 - x)^2}. \tag{9}$$

Note that F_e increases *nonlinearly* with the proof-mass displacement, and it is always a destabilizing (positive feedback) force that fights against the mechanical recovery force F_m from the MEMS spring. In a stable MEMS system, F_e always remains lower than F_m or the electrostatic force will keep moving the proof mass toward the electrode and eventually result in an electrostatic *pull-in* [23]. To maintain a stable

MEMS system, we need to find an upper bound of the displacement x that satisfies

$$k_m x > \frac{\varepsilon_0 A {V_B}^2}{(g_0 - x)^2}. \tag{10}$$

While the complete solution of (10) remains complicated, an important tradeoff between the MEMS bias voltage and the proof-mass displacement range can be found here. The maximum bias voltage that we can use for the accelerometer is determined by the MEMS specifications, as well as the proof mass displacement range x (proportional to the input acceleration). Equivalently, with a larger V_B applied to the MEMS, its proof-mass displacement must be more constrained to maintain $F_m > F_e$ and avoid pull-in. A special case is when V_B exceeds a certain limit, and the MEMS proof mass will destabilize and pull-in even with $x = 0$ (no acceleration), implying a theoretically maximum V_B that can be used to bias a specific MEMS. Section V provides additional results supporting this tradeoff between V_B and the MEMS full-scale (measurement range).

Another way to understand the impact of V_B is through the change in the MEMS sensitivity that was derived in (4). Intuitively, if the proof mass initially moves a distance x_1 with input acceleration, it moves closer to the electrode and experiences a greater attraction force from it. This will move the proof mass an additional distance x_2 so that its overall displacement becomes $x_1 + x_2$ under the same acceleration. The proof mass behaves as it has a "reduced stiffness" from the spring, hence we rewrite (4) as

$$\frac{dC_1}{da} = \frac{m\varepsilon_0 A}{(k_m + k_e)(g_0 - x)^2} \tag{11}$$

where k_m and k_e represent the mechanical stiffness (by the spring) and electrostatic stiffness (by high-voltage bias V_B), respectively, and their values are expressed by

$$k_m = \frac{ma}{x} \quad k_e = -\frac{2\varepsilon_0 A {V_B}^2}{(g_0 - x)^3}. \tag{12}$$

With a larger V_B, the MEMS's overall stiffness $(k_m + k_e)$ decreases, resulting in a higher MEMS sensitivity to acceleration. This further transfers into a nonlinear increase in the MEMS signal V_{IN} at given accelerations as shown in Fig. 3(b). When V_B is small, the electrostatic feedback is negligible, and V_{IN} increases linearly with V_B, as described in (7). When V_B becomes large and generates a strong enough electrostatic force on the proof mass, a super-linear increase in V_{IN} results. This super-linear increase in the MEMS signal has not been utilized in prior work because of the challenges associated with the MEMS full-scale reduction and the risk of pull-in. However, there is a large potential associated with it to improve the accelerometer's SNR without necessarily increasing power consumption and circuit complexity. Section II-D outline the proposed approach to generate the proper high-voltage bias and achieve an optimized accelerometer performance with sub-nW ultralow-power.

D. Electrostatic Mismatch Compensation

To take advantage of the high-voltage bias while mitigating its side effect due to electrostatic feedback, we utilize the MEMS's differential structure and apply balanced +/− voltage on the two electrodes neighboring a proof mass. As shown in Fig. 4(a), EL1 is biased with a positive high-voltage V_{B+}, while EL2 is biased with a negative voltage $V_{B-} = -V_{B+}$. When PM1 is dc coupled to ground/substrate, it will experience equal electrostatic forces F_{e1} and F_{e2} from EL1 and EL2, respectively, but in opposite directions, so they cancel each other out. Then, PM1 will no longer suffer from the mismatch of electrostatic force regardless of the value of V_{B+} and V_{B-}.

However, maintaining a balanced electrostatic force on PM1/PM2 is tricky in practical applications, and electrostatic feedback still exists due to electrostatic mismatch, defined as $F_{\text{mis}} = F_{e1} + F_{e2}$. There are two reasons for a nonzero electrostatic mismatch.

1) During MEMS fabrication, process variation can cause a mismatch in the MEMS's mechanical parameters [e.g., area A or gap distance g_0 in (9)]. Circuit nonidealities also induce electrical mismatches, such as voltage errors and ripples, making it difficult to generate exactly equalized V_{B+} and V_{B-} voltages.
2) Even if we have a perfectly symmetric MEMS and a well-balanced V_{B+} and V_{B-}, we can only guarantee the electrostatic balance under stationary conditions

$$F_{\text{mis}} = F_{e1} + F_{e2} = \frac{\varepsilon_0 A {V_B}^2}{{g_0}^2} - \frac{\varepsilon_0 A {V_B}^2}{{g_0}^2} = 0. \tag{13}$$

Once there is an input acceleration ($x \neq 0$), F_{e1} and F_{e2} will diverge and cause electrostatic mismatch

$$F_{\text{mis}} = F_{e1} + F_{e2} = \frac{\varepsilon_0 A {V_B}^2}{(g_0 - x)^2} - \frac{\varepsilon_0 A {V_B}^2}{(g_0 + x)^2} \tag{14}$$

which is simplified as

$$F_{\text{mis}} = \varepsilon_0 A {V_B}^2 \frac{4g_0 x}{({g_0}^2 - x^2)^2}. \tag{15}$$

When $x^2 \ll {g_0}^2$, F_{mis} increases proportionally with the proof-mass displacement (acceleration). And if x grows large enough under strong accelerations, the increase of F_{mis} becomes more dramatic and eventually converges to the single-ended electrostatic force described in (9).

For both of the reasons listed above, the electrostatic mismatch increases quadratically with increasing V_B, and thus both issues need to be carefully considered in the high-voltage bias scheme for MEMS capacitive accelerometers. This article presents a technique called EMC, which intentionally modulates the bias voltages to address the challenges raised by F_{mis}. The EMC technique has two goals.

1) Extend the linear region of MEMS signal sensitivity to higher V_B levels. As described by (15), the electrostatic mismatch due to MEMS process variation and circuit nonideality is amplified with a larger V_B. To compensate for the mismatch, EMC directly equalizes F_{e1} and F_{e2} by introducing an *intended* voltage skew ΔV_B between V_{B+} and V_{B-} and maintaining ultralow voltage errors and ripples for ΔV_B. As a result, the MEMS signal sensitivity remains linear at a higher V_B threshold, as shown by the blue curve in Fig. 4(b). This implies that

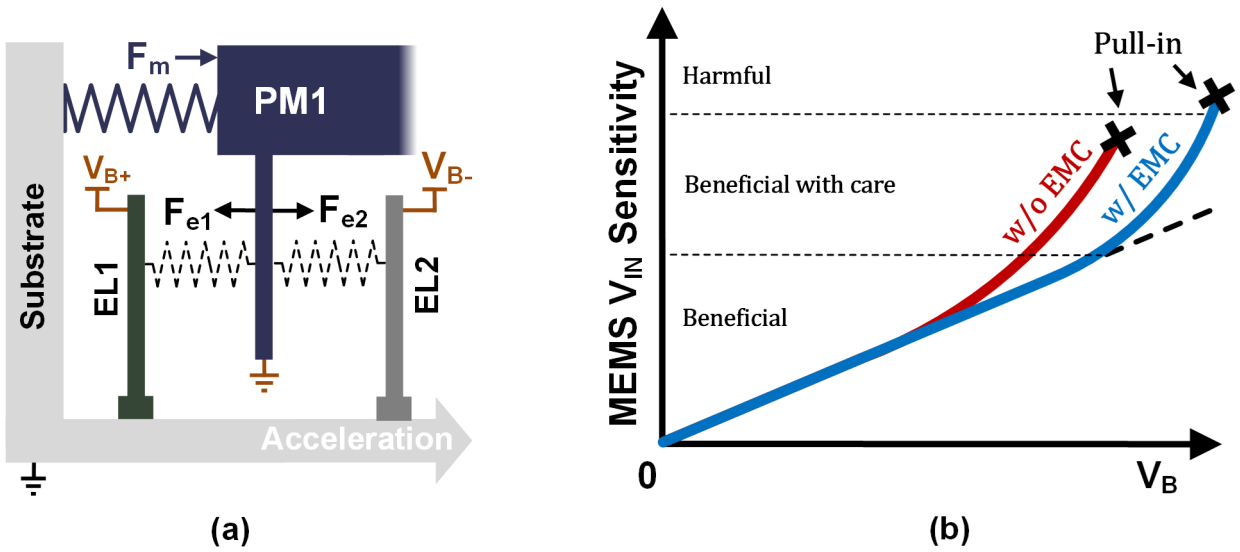

Fig. 4. (a) Stress analysis of the proof mass in a differential MEMS structure. (b) Change in MEMS signal sensitivity with bias voltages for systems with/without EMC.

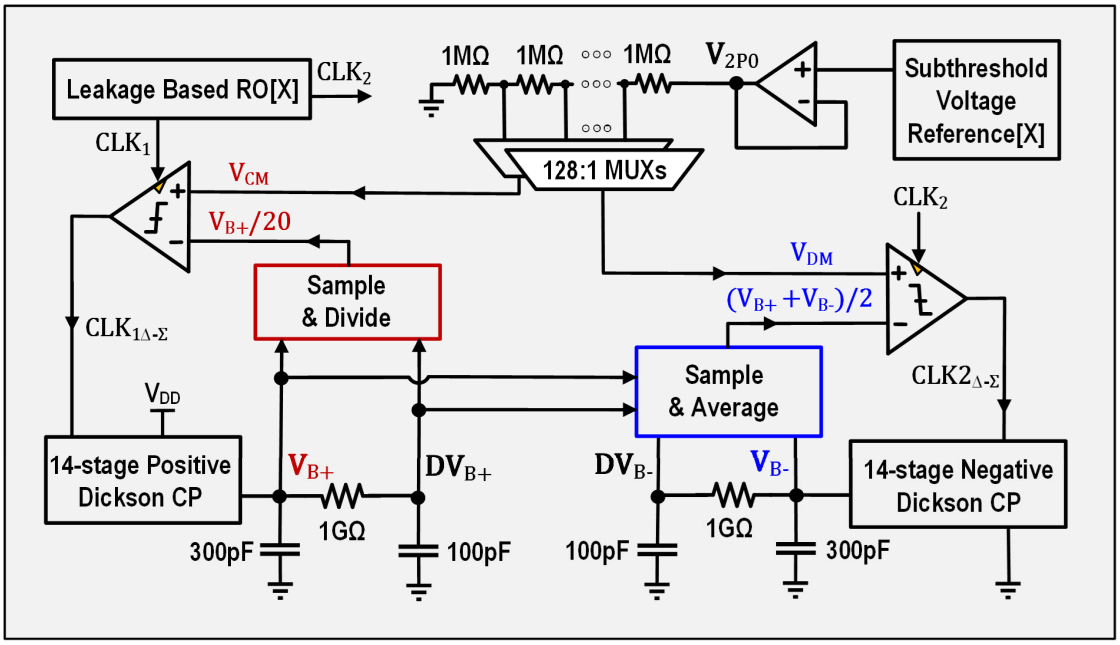

Fig. 5. Top-level diagram of the HVC chip.

we can increase the MEMS signal sensitivity by using higher V_B, but without changing the MEMS sensitivity which results in the reduction of the MEMS full scale.

2) Beyond the linear region, optimize the tradeoff between MEMS sensitivity and full scale. At very large V_B, nonlinearity appears in the MEMS sensitivity, and electrostatic mismatch is mainly caused by the proof-mass displacement (input acceleration). A static EMC approach (e.g., in this article a fixed voltage skew on the bias voltages) cannot compensate for the displacement-induced electrostatic mismatch, but it helps to achieve a better tradeoff between the MEMS sensitivity and dynamic range by properly controlling the linearity increase rate and avoid pull-in. The EMC implementation in this work carefully chooses the values of V_{B+} and V_{B-} so that sufficient dynamic range is achieved, and the pull-in point is pushed to a higher bias voltage. EMC also needs to determine the necessary safety margin on the bias voltages to accommodate variation across MEMS chips/wafers.

In summary, EMC aims to guarantee a more stable, predictable, and variation-robust MEMS operation when utilizing a high-voltage bias for better accelerometer SNR. EMC is realized through the HVC chip that we discuss in Section III.

III. Implementation of the HVC Chip

A. High-Precision Bias Voltage Generation for EMC

The EMC technique relies on generating precisely controlled V_{B+} and V_{B-} with proper values to compensate for the

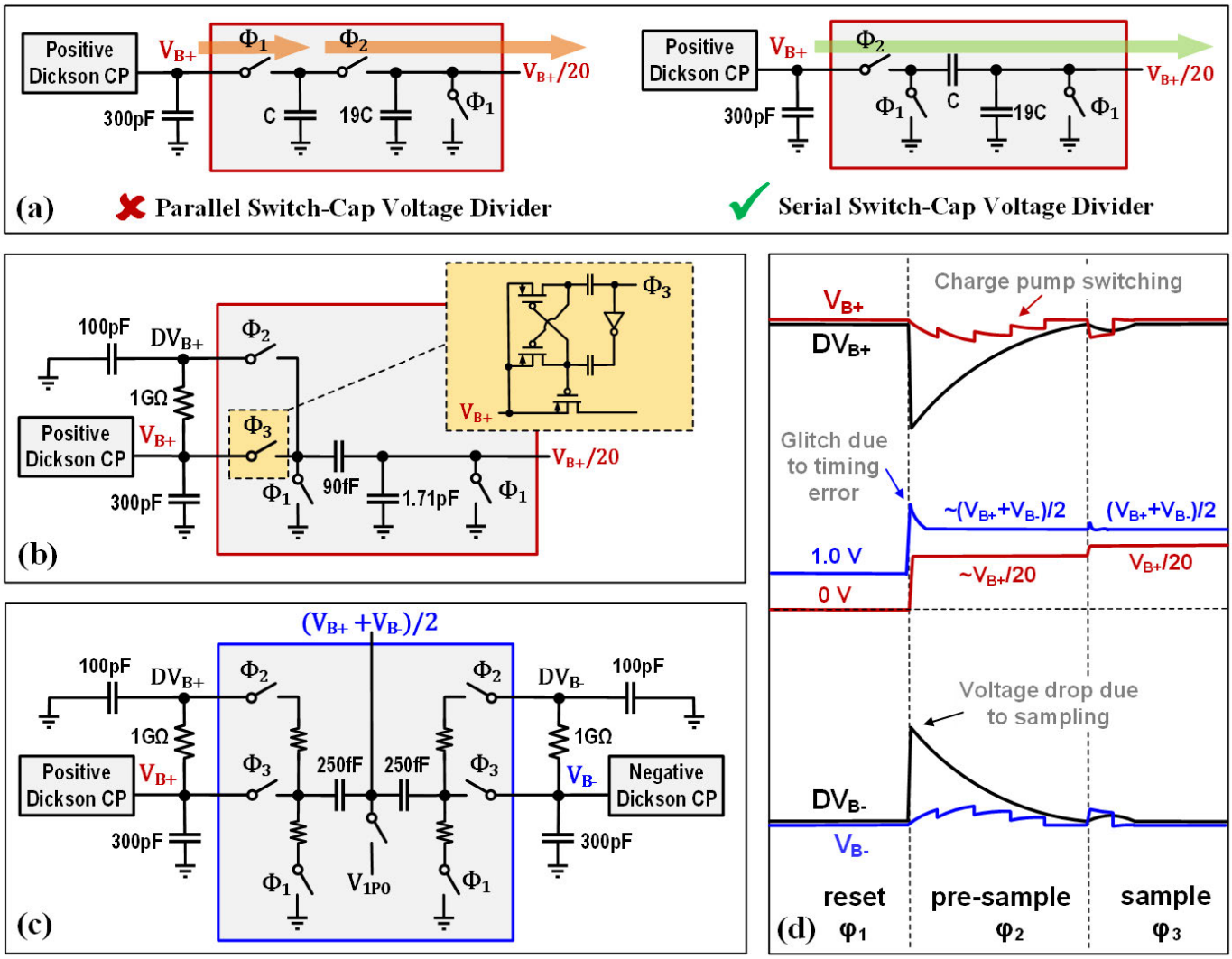

Fig. 6. (a) Comparison between the voltage divider of parallel/serial switched capacitors, showing that the serial structure has a better ac path only controlled by Φ_2. (b) Implementation of the V_{B+} sampling and division circuit, with a separated dirty V_{B+} to precharge the sampling nodes and reduce V_{B+} ripples. (c) Implementation of the V_{B+} and V_{B-} average circuit and (d) conceptual waveform showing transient voltages (b) and (c).

MEMS process variation and CMOS circuit nonideality. In this work, the high-voltage biases are upconverted from V_{DD} using Dickson charge pumps [24] for a large conversion ratio, chip integration, and high efficiency with low load current (V_{B+} and V_{B-} are dc voltages, and EL1/EL2 are purely capacitive).

Fig. 5 shows the positive and negative charge pumps on the HVC chip used to generate V_{B+} and V_{B-}, respectively. The charge pump outputs are sampled and compared with the $+/-$ reference voltages, and the comparison results modulate the charge pumps' operations in a delta-sigma manner to form a closed-loop control on the bias voltages. In addition, V_{B+} and V_{B-} are in the range of 20–30 V, so they must be divided before they can be compared with the on-chip reference voltages (0–2 V). However, any voltage errors from the reference are amplified by the large division ratio (e.g., $20\times$) when they appear in the bias voltages. For example, the programmable reference voltages are multiplexed from a resistive voltage divider that divides 2 V with 128 poly-resistors, and the quantization error is $2\ \mathrm{V}/128 \approx 15$ mV. The resulting error on V_{B+} and V_{B-} will then become $15\ \mathrm{mV} \times 20 = 300$ mV, making it difficult to achieve EMC with the required voltage precision.

To address this challenge, we only perform voltage sampling and division ($20\times$) for V_{B+} to control the positive charge pump. For V_{B-}, we sample its arithmetic mean with V_{B+} and directly compare the mean value with the other reference voltage to determine the negative charge pump operation. As a result, V_{B-} will follow the change of V_{B+} while keeping a programmable voltage skew $\Delta V_B = (|V_{B+}| - |V_{B-}|)$ that is determined by the second comparison. In other words, we refactor the bias voltages into a "common-mode" part and a "differential-mode" part

$$V_{B+} = 20V_{\mathrm{CM}} \tag{16}$$

$$V_{B-} = -20V_{\mathrm{CM}} + 2V_{\mathrm{DM}} \tag{17}$$

where V_{CM} and V_{DM} are the reference voltages that are used by the comparison for the positive and negative charge pumps, respectively. While the voltage error of V_{CM} is multiplied by 20 on both V_{B+} and V_{B-}, the V_{DM} error only has a $2\times$ effect on $(|V_{B+}|-|V_{B-}|)$. This greatly benefits EMC as the electrostatic

mismatch effect is directly associated with the voltage skew ΔV_B. More specifically, when we rewrite (14) with $x \ll g_0$ (which is true within our accelerometer's measurement range), we have

$$F_{\text{mis}} = \frac{\varepsilon_0 A(|V_{B+}| - |V_{B-}|)(|V_{B+}| + |V_{B-}|)}{{g_0}^2} \tag{18}$$

which shows that F_{mis} scales proportionally to $\Delta V_B = (|V_{B+}| - |V_{B-}|)$. With the 128-step voltage divider, the ΔV_B precision is around 30 mV which is comparable to the level of voltage ripples at EL1 and EL2, so increasing the precision (voltage divider step) will not benefit the EMC effect further. Besides, with a pF-level capacitance at the voltage divider, the noise level at ΔV_B is 100 μV which is negligible when compared to the voltage ripples. In future implementations, in case a finer EMC controllability is required, the fine-grain technique proposed by [32] can be utilized to achieve better mismatch compensation with the same voltage variation.

Meanwhile, to mitigate the effect of supply noise/fluctuation on V_{B+} and V_{B-}, we utilize a subthreshold voltage reference [25] to generate a 2-V voltage and divide it with the 128-step voltage divider to obtain V_{CM} and V_{DM}. The designed voltage reference is simulated with a 0.7% line sensitivity (LS) and -41-dB power supply rejection ratio (PSRR), while a $<1\%$ error from 0 °C to 100 °C is also achieved to guarantee a stable V_{CM} and V_{DM} at all temperatures. Considering that the subthreshold voltage reference has a large current variation between temperatures, we buffer its output voltage before applying it to the voltage divider to guarantee a sufficient current that flows through the voltage divider and generates precise V_{CM} and V_{DM}. Since $\Delta V_B = 2 * V_{\text{DM}}$, the voltage/temperature variation will also have a negligible effect on EMC, maintaining the potential sensitivity improvement with proper bias voltages.

B. High-Voltage Sampling Circuits for V_{B+} and V_{B-}

Several circuit challenges are raised with sampling/dividing the high-voltage V_{B+} and V_{B-}. First, the switched-capacitor voltage divider induces a switching loss approximately equal to 0.5 fCV^2, where f is the sampling frequency, C is the sampling capacitance, and V is the voltage swing. For a sufficiently fast charge pump feedback control required by EMC (e.g., $f = 1000$ Hz, $C = 100$ fF and $V = 30$ V), the resulting power losses on V_{B+} and V_{B-} are in the 100-nW range, and it takes even more power consumption from V_{DD} to replenish the bias voltage losses. To mitigate the power overhead that results from frequently sampling/dividing the high-voltage nodes, we implement a serial-connected switched-capacitor voltage converter shown in the right-hand side of Fig. 6(a). Unlike its parallel counterpart on the left, the serial switched-capacitor divider does not rely on the alternative Φ_1 and Φ_2 to update its output voltage ($V_{B+}/20$). Instead, its ac signal division is only activated and maintained by turning on Φ_2. Although, in many cases, this can be a disadvantage because of no isolation between the input and output voltages, it is beneficial for our application because we want the input voltage variation to be reflected in the output. So, in the proposed circuit we highly duty-cycle Φ_2 to keep it on and update $V_{B+}/20$ with any ripples and variations that occur at V_{B+}. Meanwhile, for Φ_1, we only turn it on once after a long time (e.g., seconds), so the sampling frequency will be in the sub-Hz range, significantly saving power.

A second challenge manifests itself when the storage capacitor (300 pF) charge shares with the sampling capacitor, resulting in ripples on V_{B+} and V_{B-}. Even with a large capacitor ratio, the ripples can be in the 100-mV range due to the high-voltage scales of V_{B+} and V_{B-}, causing an unpredictable, transient F_{mis} to the MEMS and increasing the common-mode noise seen by the AFE circuits. To address this issue, we separate V_{B+} and V_{B-} from two "dirty" nodes, DV_{B+} and DV_{B-}, each through a large RC constant ($\tau = 1\ \text{G}\Omega \times 100\ \text{pF} = 0.1$ s). During voltage sampling, DV_{B+} and DV_{B-} will first precharge the sampling capacitors to near V_{B+} and V_{B-} so that the ripples occur on the dirty nodes instead of the actual MEMS bias voltages. The dirty nodes' voltage loss will later be replenished by the charge pump but through the large RC network. As a result, V_{B+} and V_{B-} only see charge pump ripples rather than the much larger sampling ripples.

Fig. 6(b) and (c) shows the final implementation of the high-voltage sampling and division/average circuits, while Fig. 6(d) describes the transient waveform during voltage sampling. The pulsewidth of Φ_1 and Φ_2 remains less than 1% of the sampling clock period, while Φ_3 are turned on for the vast majority of time to maintain an ac path from the input to the output voltage, as we discussed above. Timing switches are implemented with high-voltage transistors with their control signals level-shifted with the capacitive level shifters from [26], mitigating control power with low sampling frequency. Furthermore, in the voltage average circuit in Fig. 6(c), we include current-limiting resistors to reduce voltage spikes on $(|V_{B+}| - |V_{B-}|)/2$ due to the timing difference of the V_{B+} and V_{B-} switches and prevent the spike from damaging the comparator circuit.

C. Electrostatic Pull-In Detection and Protection

When EMC optimizes the tradeoff between MEMS sensitivity and full scale, it applies the highest V_{B+} and V_{B-} with a safe margin for input accelerations and MEMS process variation. However, it is still possible that during the operation/calibration phase, an improper bias voltage is applied and triggers an electrostatic pull-in for the MEMS. While the pull-in is mechanically recoverable and nondamaging for the MEMS chip, it raises issues for the AFE chip because of the electrical contact between the proof mass and electrode. As shown in Fig. 7(a), when PM1 pulls-in with EL1, the large storage capacitor at EL1 will charge PM1 to near V_{B+}. Since PM1 is connected to the amplifier input on the CMOS AFE chip, the high voltage may cause the breakdown of the transistor's gate oxide and permanently damage the AFE circuit.

To prevent this from occurring, we implement a pull-in detection and protection circuit on the HVC chip, as shown in Fig. 7(b). We first connect a smaller (5 pF) capacitor to V_{B+} so that when PM1 pulls-in with EL1, the voltage

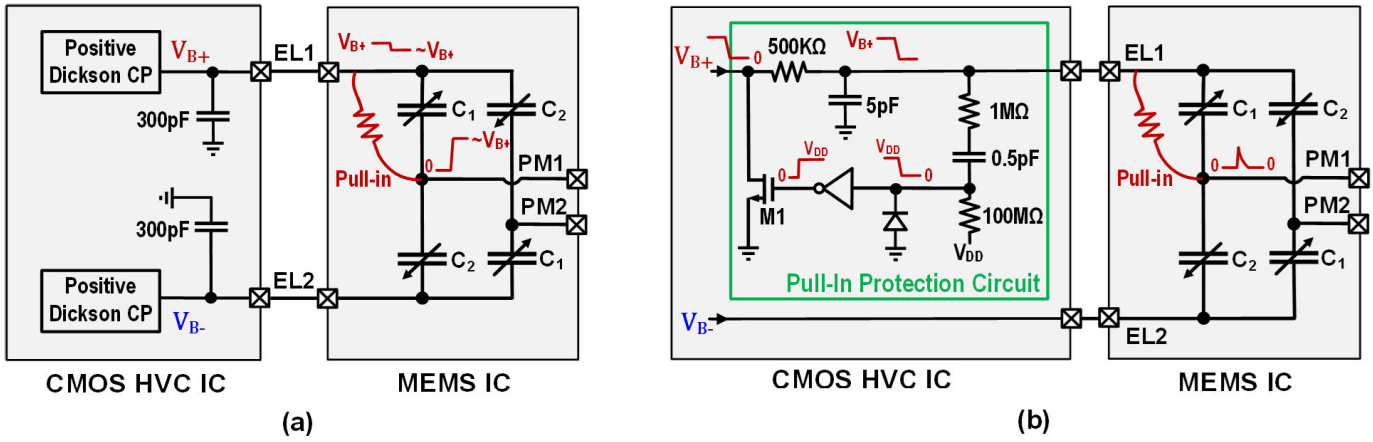

Fig. 7. (a) Without the protection circuit, pull-in results in high-voltage stress in PM1 that can damage the AFE circuit. (b) With pull-in protection, the voltage drop in EL1 will ground V_{B+} and prevent damage to the AFE chip.

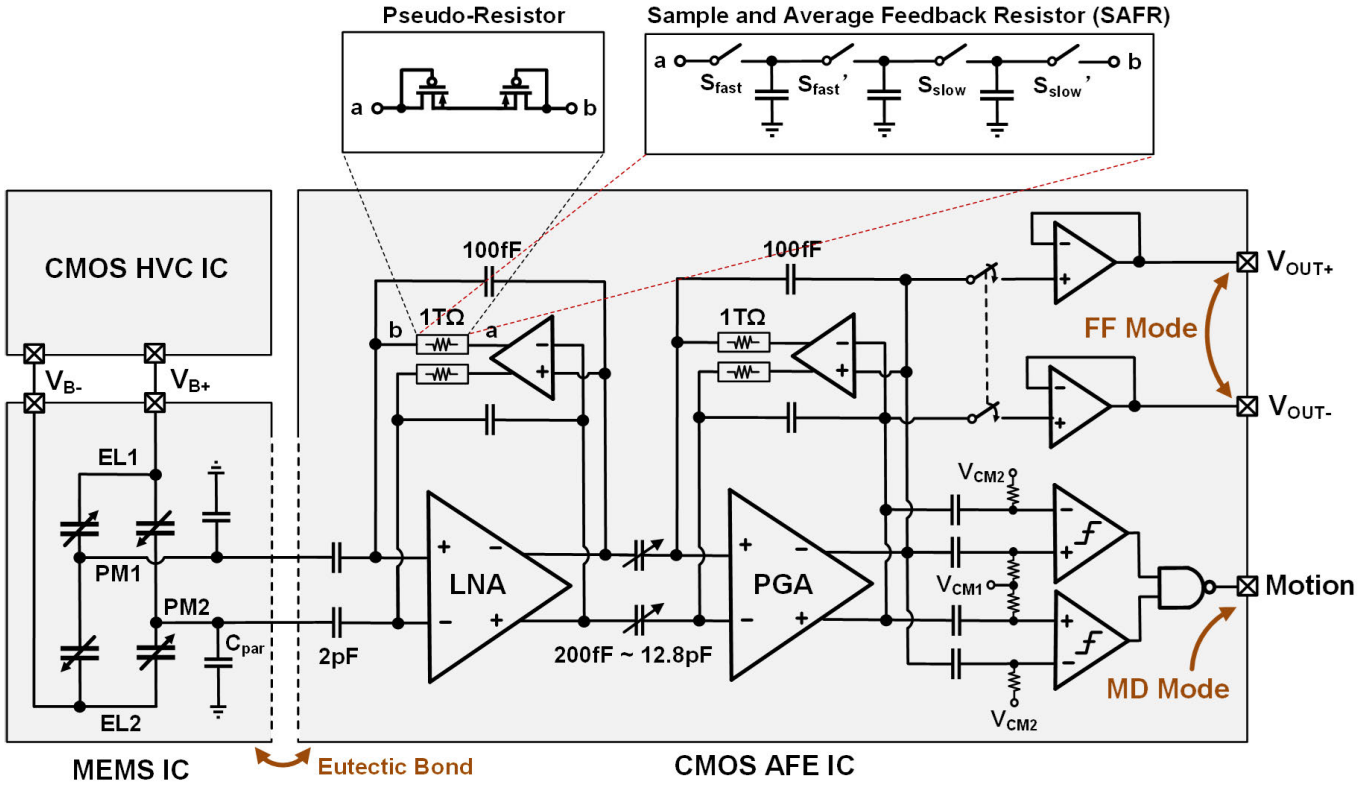

Fig. 8. Top-level diagram showing the MEMS + CMOS AFE chip.

drop at EL1 will be large enough to be detected. The EL1 voltage drop is ac-coupled with a high-pass filter (0.5 pF and 100 MΩ) to generate a reset signal that grounds V_{B+} via transistor M1. By controlling the bandwidth of this feedback, it can detect and ground V_{B+} before it generates a sufficiently high-voltage spike that can damage the AFE circuit. After V_{B+} is grounded to 0, the electrostatic force between PM1 and EL1 disappears, and PM1 is recentered by the spring. Meanwhile, in the pull-in protection circuit, V_{DD} will recharge the 0.5-pF capacitor through the dc path (100 MΩ), and the reset signal is retracted to enable V_{B+} to rebuild its voltage.

IV. Implementation of the MEMS and CMOS Analog Front-End Chip

The HVC chip generates a proper pair of V_{B+} and V_{B-} with EMC and applies the bias voltages to the MEMS electrodes EL1 and EL2, respectively. When acceleration occurs, a differential MEMS signal V_{IN} is generated across PM1 and PM2 due to the MEMS capacitance change, and the signal is amplified by the CMOS AFE chip. Equation (7) shows that the MEMS signal declines with the proof-mass parasitic capacitance C_{par}. Therefore, to reduce C_{par} due to the MEMS-CMOS interconnect, we eutectically bond the MEMS and

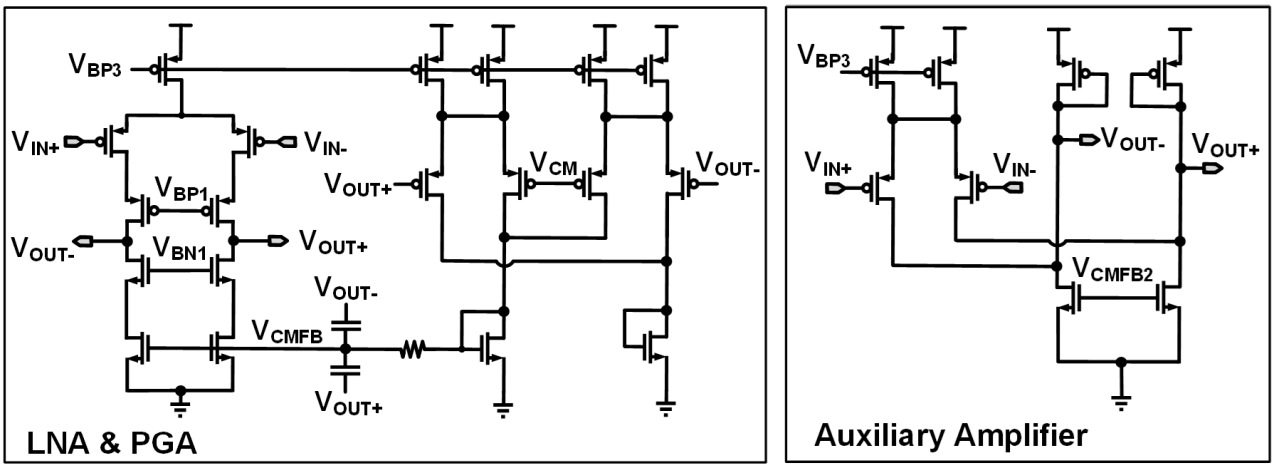

Fig. 9. Schematic of LNA/PGA and the auxiliary amplifier shown in Fig. 8.

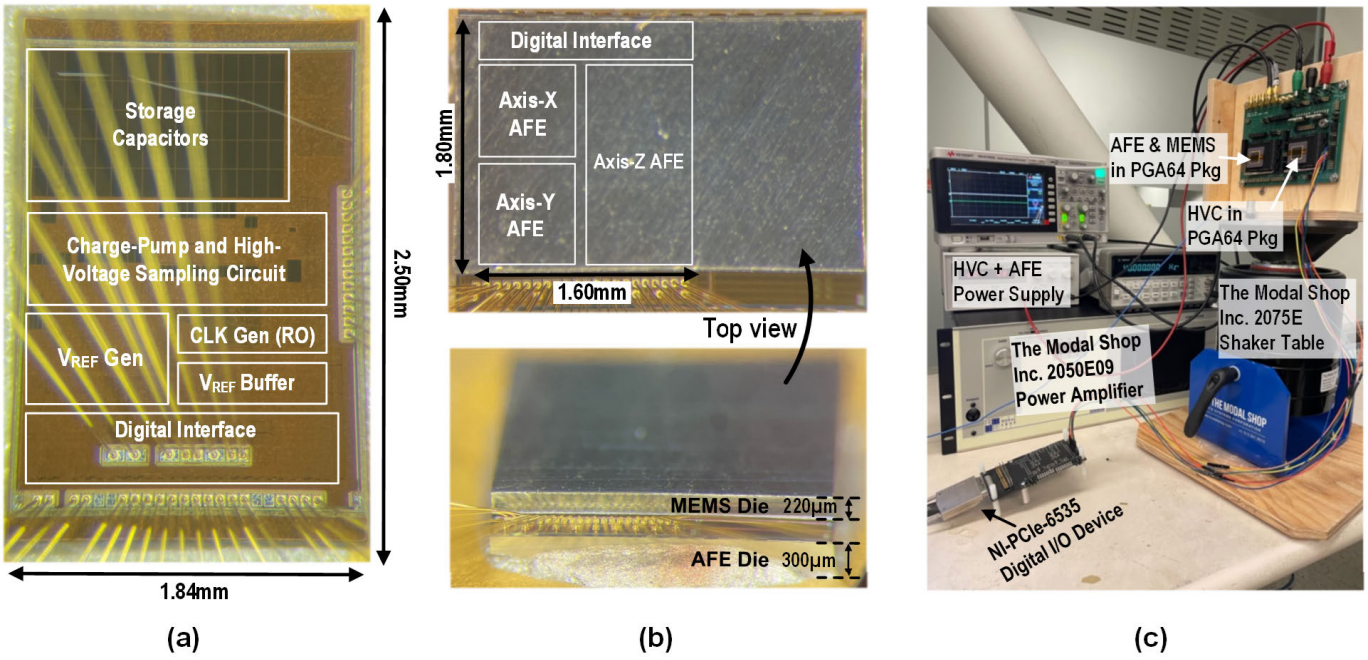

Fig. 10. (a) HVC die photo. (b) CMOS die photo and the eutectically bonded MEMS-CMOS die. (c) Testing setup for the accelerometer measurement.

CMOS AFE circuit at the wafer level and then dice the wafer into two-layer face-to-face bonded MEMS-CMOS chips.

On the CMOS AFE chip, we adopt a two-stage capacitive coupled amplifier design consisting of an LNA followed by a programmable-gain amplifier (PGA) as shown in Fig. 8. The combined LNA and PGA design is similar to [27] with auxiliary amplifiers to shift their output dc-levels to the input for maximized dynamic range. The detailed schematic of the LNA/PGA/auxiliary amplifier can be found in Fig. 9, and we generate tunable bias voltages ($V_{\mathrm{BP1-3}}$) on chip with diode-connected transistor stacks (similar to [27]). The diode-connected transistors are sized identically to the transistors in LNA and PGA, thus providing a similar bias voltage scaling effect through PVT variations. With the default gain and bandwidth settings (consumes about 40-nW amplifier power), the LNA has a 16-kHz unity-gain bandwidth, with a 6.5-μV integrated noise level from 5 to 200 Hz, and a >55-dB PSRR. The PGA has a 6.5-kHz unity-gain bandwidth while its noise characteristics are not critical for the system. For the PGA design, a telescopic structure is used to provide sufficient open-loop gain (>70 dB in simulation) to minimize gain nonlinearity errors [28]. Both the LNA and PGA consume low power, but their noise floor is far below the significantly increased MEMS signals, thus achieving a high SNR. Especially, the size of the LNA input pair is enlarged (W/L = 187/0.42 μm) to achieve a 20-Hz $1/f$ corner. Further decreasing this corner would require even larger devices (extra chip area + larger parasitic at the input, which degrade the signal amplitude) or feedback/chopping techniques (much higher power). This corner frequency is a good tradeoff as we target detecting motions that are mostly at higher frequencies.

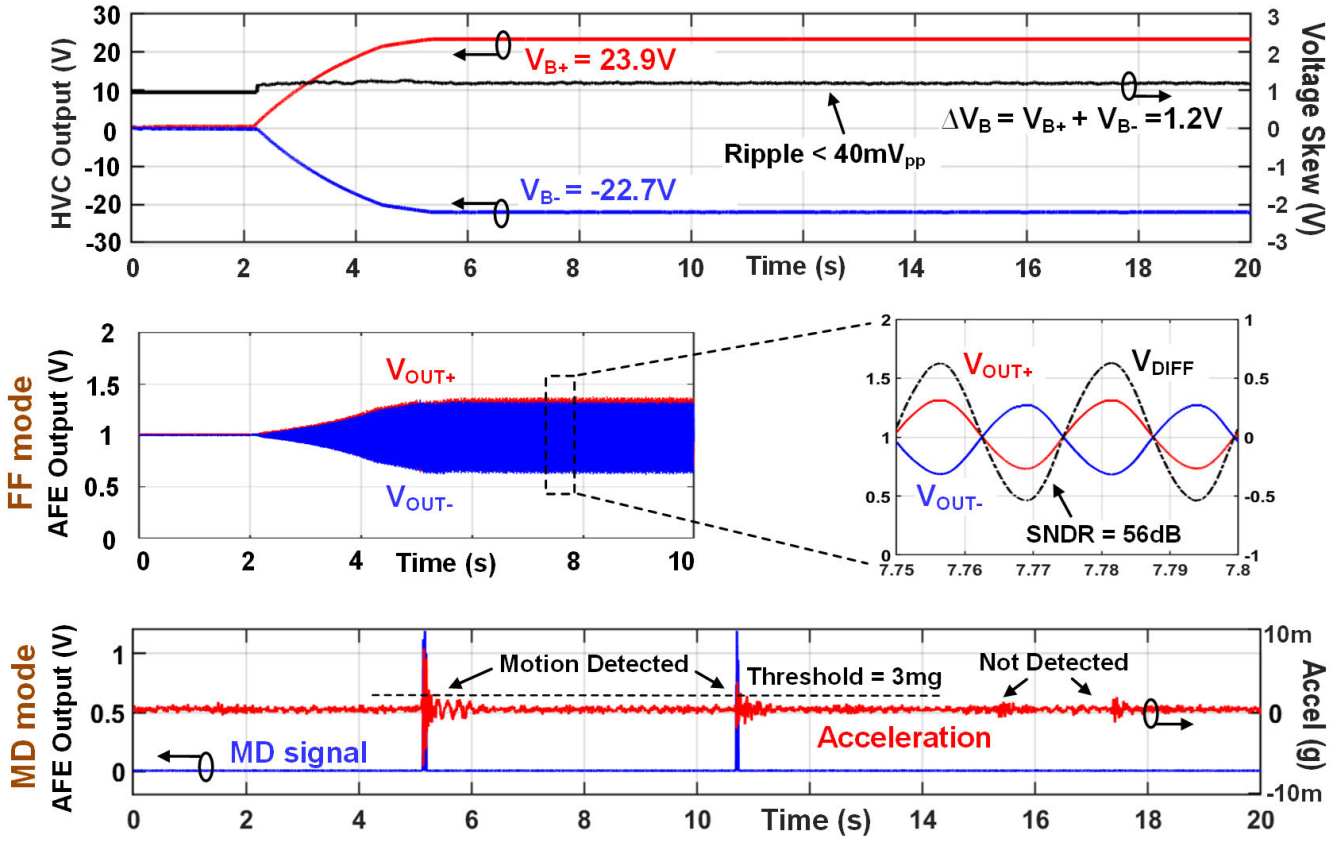

Fig. 11. Measured transient waveform showing the HVC bias voltage generation from cold start, and the AFE output voltage in both FF and MD modes.

The system has two operating modes. In the full-function (FF) mode, the AFE circuit generates a rail-to-rail analog voltage output that covers a ±1.5 g measurement range for accelerations. In the absence of acceleration, it can switch to an ultralow-power MD mode to only output a 1-bit signal when there is an acceleration exceeding a detection threshold. The "threshold" of MD is defined by the application requirement (e.g., 10 mg for a security system), and it is changed with the comparator offset voltages (V_{CM1} and V_{CM2} in Fig. 8) that can be externally configured. During the MD mode, V_{DD} is reduced from 2 to 1.2 V, and the amplifier bias current is further reduced to sub-nA levels to save circuit power.

A main challenge for the AFE chip is its bandwidth design. Although the AFE low-pass corner is defined by the PGA bandwidth and can be directly modulated with the PGA bias current, its high-pass corner design remains difficult to implement. With the dc bias voltages V_{B+} and V_{B-}, the MEMS capacitor bridge can only sense the change of accelerations and produce ac signals. While this approach is acceptable for MD applications, this requires that the AFE circuit define a high-pass corner with the amplifiers' feedback RC networks. With a feedback capacitor of 100 fF for low-power operation, the resistance needs to be at tera-ohm levels to guarantee a sufficiently low high-pass corner. As shown in Fig. 8 (top), we first implemented a 1-TΩ feedback resistor with the pseudo-resistor [29], achieving a near-Hz high-pass corner. To detect very slow motions and reduce frequency variation from pseudo-resistors, we implemented a second version of the AFE that utilizes a sample and average feedback resistor (SAFR, proposed in [30]) for a 100-TΩ equivalent resistance and pushed the AFE high-pass corner to 0.2 Hz. However, with the nonchopping dc bias voltages, it is not possible for the proposed design to detect dc accelerations, and we intentionally trade this ability for a magnitude-lower power consumption than the ac-driving accelerometers. Also, the transducer offset cancellation is not required in our implementation. In future implementations, a possible solution to enable dc sensing is to add a mode where chopping is enabled at a relatively low frequency. Because of the high-voltage bias, the low-frequency chopping will provide good resolution to the dc acceleration while consuming a (reasonably) higher power. In the meanwhile, an offset cancellation technique would be needed with the extra cost of chip power.

V. Measurement Results and Analysis

A. Accelerometer Performance Measurements

We fabricate the HVC chip in a 180-nm HVBCD process and the AFE chip in a 180-nm MEMS-compatible process. Ideally, it would be beneficial to implement both HVC and AFE blocks on the same chip with the HVBCD process, but the HVBCD process does not support the MEMS-compatible design with the required features (e.g., specialized top metal layers) to allow postprocessing of eutectic bonds between the AFE and MEMS die. As a result, HVC and AFE are implemented on two separate dies, as shown in Fig. 10(a) and (b), respectively. The AFE chips are postprocessed and eutectically

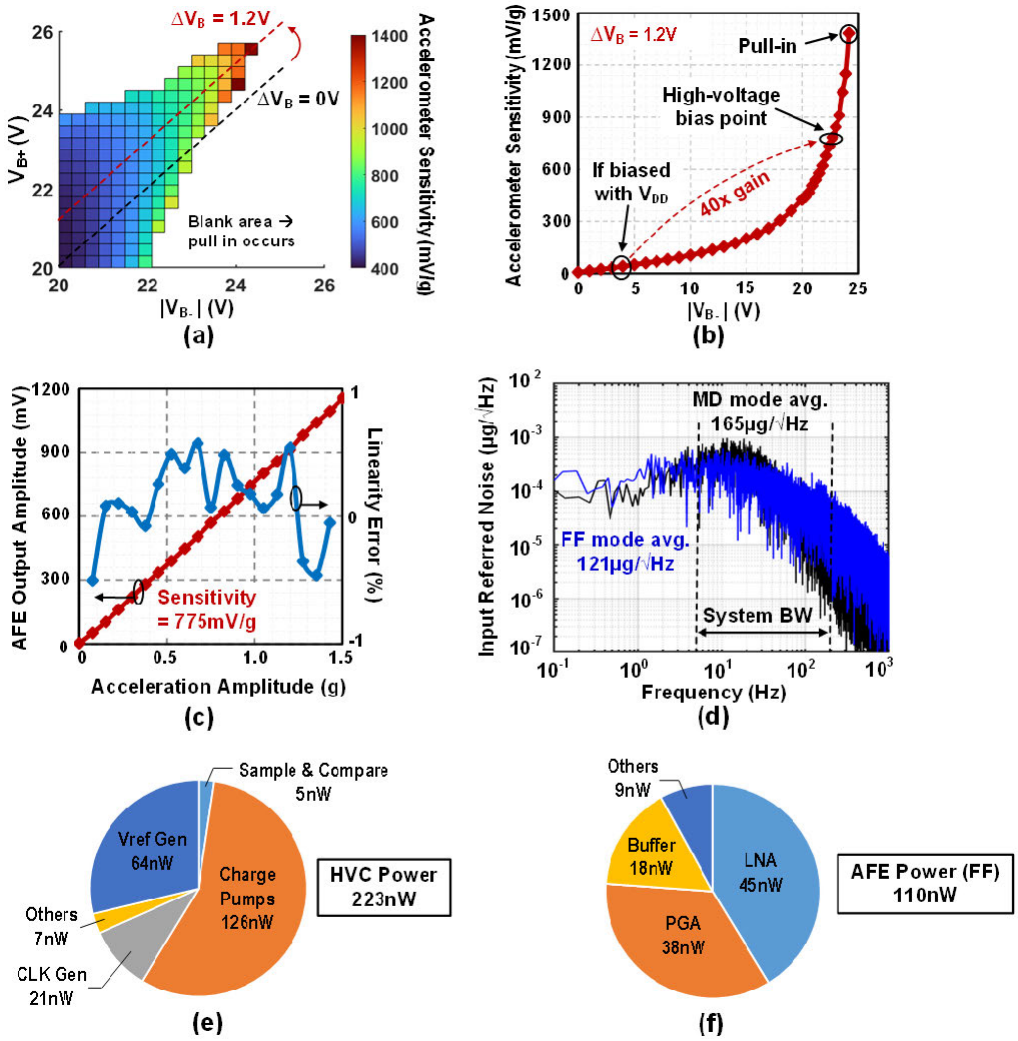

Fig. 12. Measured results for (a) accelerometer sensitivity with >20-V V_{B+} and V_{B-}, showing an optimal 1.2-V voltage skew. (b) Accelerometer sensitivity from 0 to 25 V bias maintaining a 1.2-V skew. (c) Linearity of accelerometer output within the 1.5-g full scale. (d) Accelerometer input-referred noise (determines its resolution) in FF and MD mode. (e) and (f) Power breakdown of the HVC and AFE chip in the FF mode (measured total power * simulated percentage for each subcircuit block).

bonded by InvenSense, Inc. with their designed MEMS chips. The MEMS chip has a 5-kHz resonance frequency, a 100-fF rest capacitance, and a 90 nF/m capacitive sensitivity. To test the fabricated accelerometer system, we mount the PCB with chip packages to a shaker table that gives acceleration excitations in three different angles, covering the X-, Y-, and Z-axes. We verified the performance for all three axes but only show the Z-axis results in this article for brevity. Both the HVC and AFE chips are powered by external sources, while the AFE analog outputs are captured by the Keysight EDUX1002A digital storage oscilloscope and quantized by a MATLAB postprocessing program.

Fig. 11 shows the measured transient waveform of the HVC output and the AFE output in both FF and MD modes. During cold startup, HVC gradually builds up V_{B+} and V_{B-} while always maintaining a constant voltage skew $\Delta V_B = 1.2$ V for EMC. In the steady state, the ripple on ΔV_B is constrained within 40 mV (<0.1% of full-scale voltage between V_{B+} and V_{B-}), which guarantees a <3% transient changes on the EMC effect due to the ripple voltages. In the FF mode, the AFE output increases with the bias voltages as indicated in (7) and stabilizes with a 56-dB signal-to-noise-and-distortion ratio (SNDR) at $V_{B+} = 23.9$ V and $V_{B-} = -22.7$ V. With the same bias condition, the AFE circuit can detect accelerations down to 3 mg in the MD mode, producing a one-bit detection signal at the output.

An important question is how to determine the value of V_{B+} and V_{B-} to achieve maximum signal increase while maintaining sufficient MEMS dynamic range. Since EMC is especially critical in the high-voltage domains, we measure a typical accelerometer sample and plot its sensitivity with all combinations of V_{B+} and V_{B-} that are larger than 20 V, as shown in Fig. 12(a). While significantly unbalanced V_{B+}/V_{B-} results in MEMS pull-in due to the large electrostatic force mismatch, equal-valued V_{B+}/V_{B-} also fails to produce optimized sensitivity due to MEMS asymmetry and process variation. With the MEMS design used in this work, it is advantageous to use a higher positive bias voltage over the negative bias voltage.

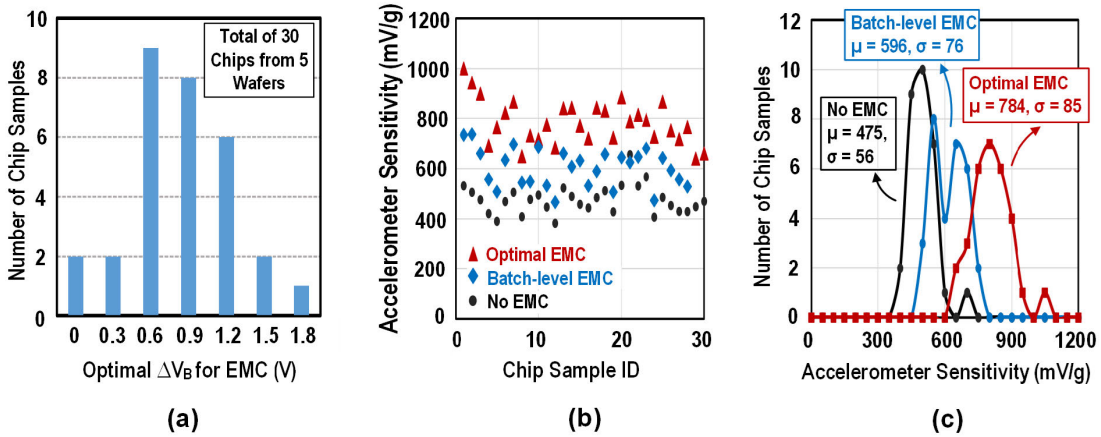

Fig. 13. (a) Distribution of the optimal voltage skews ΔV_B (that achieves the highest bias voltage before pull-in) across 30 different MEMS/CMOS chips. (b) EMC-designated accelerometer sensitivity for the 30 chip samples, with individually chosen ΔV_B (red triangle), wafer-average ΔV_B (blue diamond), and zero ΔV_B (black dot). (c) Distribution of the results in (b).

An optimal $\Delta V_B = 1.2$ V is observed for the highest accessible sensitivity for this chip sample. By keeping the 1.2-V voltage skew, we plot the accelerometer sensitivity increase with V_{B+}/V_{B-} from 0 to 25 V in Fig. 12(b). Similar to that observed in Fig. 4(b), the accelerometer sensitivity first increases linearly with small bias and then becomes super-linear above 15 V, finally pulling-in at around 25 V. The MEMS has zero measurement range at the pull-in point, so EMC backs off a few steps to $V_{B+} = 23.9$ V and $V_{B-} = -22.7$ V at which point it maintains a $\gg$20 g proof mass dynamic range which is well above the AFE dynamic range. The proposed accelerometer gains a $>40\times$ higher sensitivity from its high-voltage biasing (with EMC) compared to biasing with the supply voltage in the conventional accelerometer scheme.

With the EMC-designated bias voltages, the MEMS sensitivity is increased at the cost of a larger variation- or displacement-induced electrostatic mismatch, which reduces its dynamic range. However, the MEMS dynamic range is still significantly larger than the accelerometer's full scale ($\pm$1.5 g which is defined by the AFE chip, thus guaranteeing a good output linearity as given by (5). Fig. 12(c) demonstrates the accelerometer output voltage versus input accelerations, showing a 775-mV/g sensitivity and a $<$1% linearity error. Taking advantage of the large MEMS signal, the accelerometer achieves 121- and 165-μg/$\sqrt{\text{Hz}}$ input-referred noise floors for FF and MD modes [Fig. 12(d)], respectively, while consuming only 110 and 22.4 nW in the AFE chip. Note that in Fig. 12(d), the total noise is dominated by flicker noise, so the high-voltage biasing technique brought fewer advantages in terms of AFE power savings, compared to that in a thermal noise dominated system. Including the 223 nW HVC power used to generate the triaxial MEMS biases, the accelerometer system consumes a total of 184 and 96 nW per axis in the FF mode and MD mode, respectively. Table I summarizes and compares the performance of the proposed accelerometer with that of the prior arts focus on low power [9], [10], [11], [16], [17], high resolution [3], [4], [6], [8], or large bandwidth/dynamic range [31], [32], [33]. Compared to prior art, the proposed accelerometer with high-voltage biasing achieves a 10.3$\times$ improvement in FoM considering the power-noise product over bandwidth.

B. EMC Measurement With Process Variation

The EMC-optimized ΔV_B is 1.2 V for the measured chip sample. The question remains whether this voltage differential is robust across MEMS process variations and how to reliably use high-voltage biasing for mass-produced MEMS accelerometers across different batches. To answer these questions, we repeat the measurement process in Fig. 12(a) for 30 accelerometer samples from five different MEMS/CMOS wafers and plot their optimal ΔV_B in Fig. 13(a). Ideally, it is best to use individually optimized ΔV_Bs for each chip's V_{B+} and V_{B-} because this provides the optimal EMC and results in a higher accelerometer sensitivity (784 mV/g) with sufficient MEMS dynamic range, as shown by the red triangles in Fig. 13(b).

Though each chip only needs a one-time calibration after fabrication, this may still increase the test cost in mass production. Alternatively, a "batch-level EMC" can be performed by measuring the subset of chips on the same wafer (in this test, six samples per wafer) and applying their average ΔV_B for all the chips on that wafer. The blue diamonds show the sensitivity of the accelerometer with this technique. Fig. 13(c) shows that the optimal (individual) EMC yields the highest mean sensitivity of 784 mV/g, a 1.65$\times$ increase over no EMC (simply applying $\Delta V_B = 0$ V). Batch-level EMC incurs a sensitivity penalty of 24% at 596 mV/g compared with the optimal EMC but remains 25% better than with no EMC.

Finally, we perform a long-term, repeated pull-in test to characterize the accelerometer's durability in the case of repeated pull-ins due to large accelerations or improper MEMS bias. We intentionally triggered the MEMS proof-mass pull-in with higher-than-normal V_{B+} and V_{B-}, and we confirmed the pull-in event by observing a dramatic degradation of the accelerometer sensitivity (output amplitude). Then, we retracted the bias voltages to be less than 20 V, waiting for about 15 s until we observed the sensitivity recovery.

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED MEMS ACCELEROMETER AND COMPARISON WITH PRIOR WORKS

Publication	Process	Type	CMOS Area (mm^2)	# of Axis	MEMS-CMOS Integrated	Full Scale (g)	Bandwidth (Hz) [a]	Noise Floor ($\mu g/\sqrt{Hz}$)	Supply Voltage (V)	Power per Axis (μW)	FoM[c] ($\mu W \cdot \mu g/Hz$)
JSSC 2019 [3]	$0.5\mu m$	Capacitive	49.0	1	No	± 0.4	1 - 300	0.03	3.0	20000 [e]	34.6
JSSC 2015 [4]	$0.5\mu m$	Capacitive	7.80	1	No	± 1.2	300	0.2	7.0	23000 [e]	266
JSSC 2012 [6]	$0.35\mu m$	Capacitive	6.66	1	No	± 1.15	200	2	3.6	3600 [e]	509
JSSC 2017 [7]	$0.35\mu m$	Oscillation	6.00	1	No	± 20	40[b]	0.4	1.5	4370 [e]	276
VLSI 2018 [9]	$0.18\mu m$	Capacitive	1.14	1	No	± 8	50	970	1.0	0.181 [e]	24.8
ADXL-362 [10]	-	Capacitive	-	3	Yes	± 8	50	550	2.0	1.2 [e]	93.3
JSSC 2020 [8]	$0.13\mu m$(LV) $0.35\mu m$(HV)	Capacitive	17.6(LV) 26.0(HV)	1	No	± 0.55	400	0.022	1.4(LV) 12(HV)	14800	16.3
VLSI 2020[31]	$0.18\mu m$	Capacitive	-	1	Yes	± 1000	118000	6000	-	110000	1.92×10^6
JSSC 2023[33]	$0.18\mu m$	Capacitive	1.65	1	Yes	± 5000	5700	46.6	1.8	117000	7.2×10^4
TCSI 2022[11]	$0.18\mu m$	Capacitive	1.65	1	No	± 12	2500	270	1.8	117	632
ITIM 2022[16]	$0.18\mu m$	Capacitive	1.65	1	No	± 2	12500	112	1.8	103	103
TCSI 2022[17]	$0.18\mu m$	Capacitive	1.65	1	No	± 6.5	1000	63	1.8	34.6	68.9
This work	$0.18\mu m$(LV) $0.18\mu m$(HV)	Capacitive	2.88(LV) 4.55(HV)	3	Yes	± 1.5	5 - 200	121[d]	2(LV) 2.4(HV)	0.184	1.59

[a] Some works are capable of sensing DC accelerations, but their noise floor is measured starting from a high-pass frequency similar to this work (5Hz).
[b] Estimated with the noise spectrum figure.
[c] A widely used FoM = power $\times$ noise floor $\div \sqrt{BW}$.
[d] FF mode result for a good comparison with prior works. In MD mode, the noise floor is 165μg/$\sqrt{}$Hz with 96nW power, achieving an FoM of 1.13.
[e] Include the ADC power.

We programed the bias voltage changes as a sequence and repeated for more than 10 000 times. After >10 000 pull-ins, we remeasured the accelerometer and confirmed no sensitivity degradation due to the MEMS structure and the AFE circuit. This validates the safety and robustness of the proposed accelerometer, giving its usage of high voltages as bias.

VI. CONCLUSION

This article presents a triaxial MEMS capacitive accelerometer using high-voltage biasing to achieve high resolution with ultralow power. The accelerometer consists of an MEMS sensing chip, an AFE chip, and a high-voltage companion chip to generate the optimized bias voltage for the MEMS chip. By using the high-voltage bias, the MEMS signal is raised above the AFE noise floor, eliminating the power-hungry amplifier and signal-chopping used in the conventional MEMS accelerometers. The HVC chip, in addition to producing programmable MEMS bias voltages, also compensates for the electrostatic mismatch induced by the high-voltage biases. The proposed accelerometer is fabricated and achieves a 121- μg/$\sqrt{}$Hz input-referred noise floor with 184-nW power (including bias generation), demonstrating a 10.3$\times$ FoM improvement over prior art.

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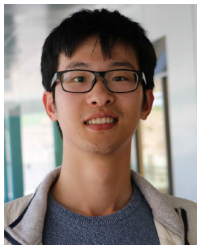

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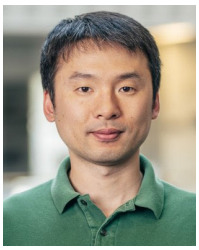

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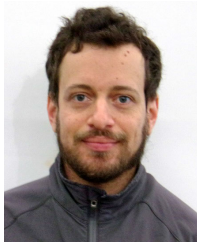

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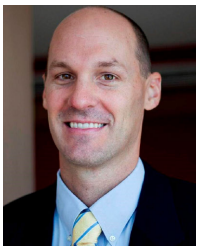

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