An RC Delay-Based Pressure-Sensing System With **Energy-Efficient Bit-Level Oversampling** Techniques for Implantable IOP Monitoring Systems

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Abstract—A pressure-sensing system with a half-Wheatstonebridge-to-digital converter (HBDC) is proposed for implantable intraocular pressure (IOP) monitoring systems. The half-Wheatstone-bridge (H-WhB) sensor uses an RC-delay comparison instead of direct bias of the pressure transducer, allowing it to self-limit the current for efficient operation. To overcome the limited sensitivity of the H-WhB, energy-efficient bit-level oversampling (OS) is introduced. The system achieves 0.24-mmHg (1 σ) resolution with an 8.58-nJ· mmHg² FOM and 12.79- μ W power consumption with a 11.52-ms conversion time. This marks a 2.8× improvement in measured system power, 56.24× improvement in energy consumption, and 2.8× improvement in resolution compared to the prior H-WhB-based pressure sensor. In addition, the HBDC overcomes the low sensitivity limitations of the H-WhB and achieves a resolution FOM comparable to that of Wheatstone-bridge (WhB) sensor-based pressure sensors.

Index Terms-Analog front-end, bit-level oversampling (OS), glaucoma, OS, pressure sensor, RC delay, resistive sensor.

I. INTRODUCTION

OW-POWER integrated circuits (IC)have enabled the emergence of implantable biomedical systems [1], [2], [3], [4], [5], [6], resulting in accurate and real-time in vivo monitoring with ultrasmall biocomfortable

Manuscript received 20 January 2023; revised 10 April 2023 and 31 May 2023; accepted 8 June 2023. Date of publication 28 June 2023; date of current version 26 September 2023. This article was approved by Associate Editor SeongHwan Cho. This work was supported in part by the Ministry of Science and ICT (MSIT), Korea under Grant IITP-2023-2020-0-01821 and in part by Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) under Grant P0017305 [Human Resource Development Program for Industrial Innovation (Global)]. (Corresponding authors: David Blaauw; Yoonmyung Lee.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3286796.

Digital Object Identifier 10.1109/JSSC.2023.3286796

transducers and wireless power transmission (WPT). With the evolution of implantable sensing systems, the paradigm of medical care is shifting from the existing treatment-based medical services and medicines to preventive medical services and medicines, avoiding the development of disease all together [7].

The pressure in our bodies provides significant health information. For example, bladder pressure is used as a diagnostic and indicator of bladder diseases, including urinary incontinence [8], and cardiovascular problems can be diagnosed based on pulmonary artery pressure [9]. Moreover, intracranial pressure is measured to assess and control real-time pressure in the brain during surgery and to diagnose and manage cerebral hemorrhage and ischemic stroke [10], [11]. Thus, the ability to measure pressure within the body is a critical component of disease prevention.

Glaucoma is a prime example of a disease where pressure monitoring is critical in disease prevention. The disease can cause intraocular pressure (IOP) to rise, damaging the optic nerve and potentially causing irreversible blindness. Glaucoma can occur when the IOP is above 21 mmHg [12], [13] (millimeters of mercury, relative pressure to atmospheric pressure).

For effective management and treatment of glaucoma, frequent and accurate IOP monitoring is crucial to adequately track real-time IOP changes. Today, the most widely used method is Goldmann applanation tonometry, a contactless procedure that measures eye pressure by blowing air into the eye. The Goldmann applanation tonometer (GAT) is the gold standard for measuring IOP, but it could be affected by various factors, such as corneal hysteresis, resistance factor, curvature, hydration, central thickness, and physician's experience level [14], [15], [16], [17].

In addition, GAT requires complex measuring equipment not appropriate for home use, making it difficult to achieve necessary frequency of measurements necessary for effective disease management. Hence, there is a growing interest in developing new technologies for continuous and direct IOP monitoring to detect disease without requiring visits to a

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Fig. 1. Conceptual illustration of the glaucoma implant system and target implant system location for IOP monitoring.

hospital and eliminate the impact of various factors of cornea in the IOP measurement.

Several miniature pressure sensor systems have been proposed for measuring pressure monitoring in earlier studies: a contact-lens-type form-factor device with strain-type sensors [18], [19], a MEMS-capacitive-type sensor [20], and a Wheatstone-bridge (WhB) piezo-resistive MEMS-type sensors [21], [22], [23], [24], [25]. However, they could not meet both limitations, the stringent volume constraints and <1-mmHg pressure sensing resolution for glaucoma implant systems, and many of them also had too high power consumption compared to what is expected for implanted systems, given the limited energy storage/delivery in such systems.

For instance, in a conventional WhB-based pressure-sensing system [21], a low-noise amplifier and analog-to-digital converter (ADC) are used to digitize the differential voltage signal generated by a WhB. However, this approach has a low energy efficiency due to the large excitation current with the low bridge resistance (typically 1–10 k Ω). In order to reduce the energy consumed in the bridge, duty-cycled excitation of the bridge has been suggested [22], [23]. However, those WhB-based sensing systems are still too large for implanted IOP monitoring systems, primarily because of the large volume and height of the WhB pressure sensor frontend (0.4 mm³ and 0.4 mm in [22] and [23] and 2.53 mm³ and 1.45 mm in [25]). As shown in Fig. 1, there is a height constraint on the cavity used for a glaucoma implant. Therefore, the pressure monitoring sensor system must have a thickness of 0.5 mm or less in order to fit. For such implantable systems, minimizing the volume and height of the pressure transducer and integrated circuit is therefore critical to ensure that the sensing system can be securely placed in the limited space without damaging the eye.

To address this, an IOP monitoring sensor system with a half-Wheatstone-bridge (H-WhB) sensor [26] was presented to comply with this stringent volume constraint. However, bridge-to-digital conversion was achieved through a voltage-controlled oscillator (VCO) generated frequency with direct application of a dc bias voltage to the H-WhB, which resulted in a high power consumption and a long conversion time. Such high energy consumption could be impractical for battery-operated miniature systems [27], [28].

In this article, we introduce a pressure-sensing system [30] that includes an *RC* delay-based half-Wheatstone-bridge-todigital converter (HBDC) designed to meet the volume/height, energy, and precision requirements of implantable IOP monitoring systems. The key contributions of our work can be summarized as follows:

- Resistance measurement/quantization through *RC* delay comparison: Instead of directly measuring the voltage generated by the sensor with ADC, we have introduced a novel resistance quantization scheme, where *RC* charging delay is compared—CDAC capacitance is adjusted to find the capacitance value that matches *RC* delays and the CDAC capacitance code can be converted to resistance value of interest. Such approach allows to overcome the lower sensitivity of H-WhB sensor (compared to the WhB sensors in previous works): proposed method converts and amplifies the resistance difference to time difference in time domain, allowing more accurate measurement.
- 2) Energy-efficient oversampling (OS): The proposed bit-level OS (BOS) technique enhances resolution by reducing noise through repeated *RC* delay evaluations yet only voting on noise-critical bit positions. By suppressing noise at the selected bit, our BOSR strategy reduces conversion time and energy consumption by up to 88% while achieving the same resolution as conventional OS approaches.
- 3) Applicability: To minimize system volume/height, we utilized an H-WhB pressure sensor front-end [29], resulting in a >8× smaller volume and >2.2× lower height (0.05 mm³ and 0.18 mm) compared to the WhB-based sensor counterpart used in [22], [23], and [25]. Although the H-WhB sensor contains only two passive elements, resulting in half the pressure sensitivity (10 μ V/V/mmHg versus 17–30 μ V/V/mmHg with WhB [22], [23], [24], [25]), the energy-efficient, high-precision resolution HBDC creates a versatile sensor platform. This platform has the potential to be applied to a variety of implantable miniature sensor system applications, expanding its applicability beyond the existing solutions.

The rest of this article is organized as follows. Section II presents the principle of the *RC* delay readout circuit. Section II details the proposed HBDC implementation and operation. Section IV introduces the proposed energy-efficient BOS techniques. The measurement results are shown in Section V, and Section VI concludes this article.

II. RC DELAY-BASED HALF-BRIDGE SENSING SCHEME

A. Principle of RC Delay Readout Circuit

Fig. 2(a) shows the simplified diagram of the proposed HBDC: two resistors (R_1 and R_2) in the H-WhB are connected to variable capacitor banks (C_1 and C_2) to form a differential pair of R-C charging structures. For pressure sensing, the precise ratio between R_1 and R_2 needs to be determined. Instead of measuring the resistance of R_1 and R_2 directly, the C_1 and C_2 values that equalize the RC charging delays ($\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$) can be determined by fixing C_1 (or C_2) to a reference capacitance value and binary searching for the C_2 (or C_1) value that equalizes τ_1 and τ_2 . To compare the RC charging delays, C_1 and C_2 are first reset (T_{RST}), and



Fig. 2. (a) Structure of the simplified HBDC and (b) description of conversion process steps and waveforms $(R_1C_1 > R_2C_2)$.

then, both charging paths are connected for a fixed amount of time (T_{Charge}) to charge C_1 and C_2 . The charging currents are self-limited during this process, which makes it energy efficient. The charged voltages V_1 and V_2 can be compared to compare τ_1 and τ_2 : if $V_1 > V_2$, then $\tau_1 < \tau_2$, and vice versa. The optimal T_{Charge} (= t_{max}) should be selected to maximize the voltage difference ($V_{\text{Diff}} = V_1 - V_2$) for an accurate comparison.

B. Optimal Charging Time (t_{max})

The theoretically optimal $T_{\text{Charge}}(t_{\text{max}})$ is approximately RC, and this can be derived as follows. $V_1(t)$ and $V_2(t)$ in Fig. 2(b) are determined as

$$V_1(t) = 1 - \exp\left(\frac{-t}{R_1 C_1}\right), \quad V_2(t) = 1 - \exp\left(\frac{-t}{R_2 C_2}\right)$$
(1)

where R_1 and R_2 denote the resistance of the resistors in the H-WhB, and C_1 and C_2 denote the variable capacitor banks. Then, the voltage difference at C_1 and C_2 can be written as follows:

$$V_{\text{Diff}}(t) = \left\{ \left\{ 1 - \exp\left(\frac{-t}{R_2 C_2}\right) \right\} - \left\{ \left\{ 1 - \exp\left(\frac{-t}{R_1 C_1}\right) \right\}. (2) \right\}$$

By differentiating $V_{\text{Diff}}(t)$ with respect to time (t) and solving for t when $V'_{\text{Diff}}(t) = 0$ provides the RC delay time corresponding to the maximum voltage difference

$$t_{\max} = \frac{C \cdot R_2 \cdot R_1 \cdot \ln\left(\frac{R_2}{R_1}\right)}{R_2 - R_1}.$$
(3)

The following three assumptions can be made for simplified approximation of the optimal T_{Charge}

$$\begin{cases} R \gg \Delta R, \, \Delta R = \text{Resistance change due to pressure change} \\ R_1 = R + \Delta R, \, R_2 = R - \Delta R, \, R_1 > R_2 \\ C \approx C_1 \approx C_2. \end{cases}$$
(4)

Simplifying the t_{max} equation using the assumptions in (4) gives the following equation:

$$t_{\max} = \frac{C \cdot (R + \Delta R) \cdot (R - \Delta R) \cdot \ln\left(\frac{R + \Delta R}{R - \Delta R}\right)}{2 \cdot \Delta R}.$$
 (5)

By approximating $\Delta R = 0$ and taking the limit, the logarithmic part of (5) can be simplified using L'Hôpital's rule

1

$$\frac{n}{\Delta R} \frac{\frac{R+\Delta R}{R-\Delta R}}{\Delta R} = \frac{2}{R}.$$
(6)

The charging time of optimal T_{Charge} , which is the point that finally maximizes the voltage difference, can be found by simplifying (5) using (6)

$$Dptimal \ T_{Charge} = t_{max} = RC.$$
(7)

Assuming a nominal resistance *R* value of 3.2 k Ω and a nominal capacitance *C* value of 716 pF, the *RC* product would be

$$t_{\rm max} = 3.2 \ {\rm k}\Omega \cdot 716 \ {\rm pF} = 2.3 \ \mu {\rm s.}$$
 (8)

Substituting the optimal T_{Charge} of (9) into (1), V_1 and V_2 are voltages near 63.2% of VDD.

$$V(\text{Optimal}T_{\text{Charge}}) = V(t_{\text{max}}) = \text{VDD} \cdot 63.2\%.$$
 (9)

Note that the theoretical margin for T_{Charge} to limit V_{Diff} error to 5% is +39%/-27%, which is large enough for robust *RC* charging operation against time variations.

III. HALF-WHEATSTONE-BRIDGE-TO-DIGITAL CONVERTER (HBDC)

A. Overall Architectures

Fig. 3 shows a detailed circuit diagram of the proposed HBDC. Each resistive element (R_1 and $R_2 \approx 3.2 \text{ k}\Omega$) in the H-WhB is connected to a load capacitor bank (C_1 and C_2), which consists of a fixed delay cap (C_{Delay} ,716 pF) and 14b-CDAC (C_T and C_B). The charged voltages of C_1 and C_2 (V_1 and V_2) are compared using an autozeroing (AZ) amplifier and clocked comparator, and the comparison result is forwarded to the digital controller for the HBDC.

In the design of our HBDC system, we considered the tradeoffs between resolution, energy consumption, and data granularity when determining the values of C_{Delay} and unit capacitor. To achieve better resolution while balancing switching loss, we chose a C_{Delay} value of 716 pF. For our target application, which is an implantable glaucoma monitoring system, we used a 6.3-fF unit-capacitor value to allow a 0.21 mmHg/LSB. However, such small unit capacitor can make it more susceptible to noise. To address this issue, we introduced a new OS method called BOS, which achieves the desired resolution while consuming less energy than conventional OS. The details of this new method will be presented in Section IV.

B. Half-WhB-to-Digital Converter Conversion Process

Fig. 4(a) shows the simplified description of the *RC* delaybased HBDC conversion process. In the initial round of *RC* delay evaluation, all capacitors in both CDACs (C_T and C_B) are connected for a pre-programmed time t_{max} . The purpose of this initial step is to find the larger resistance between R_1 and R_2 by comparing τ_1 and τ_2 . Then, the reference *RC* charging delay is set by opening all CDAC connections to the larger resistance. For example, if it is found that $R_1 > R_2$ in the

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Fig. 3. Structure of the HBDC circuit.



Fig. 4. (a) Simplified description of HBDC conversion process and (b) detail of single conversion process waveforms.

first evaluation round, then, in the following round, $\Phi_{T[13:0]}$ is set to 14'h0000 and the reference delay is $\tau_1 = R_1 \cdot C_{\text{Delay}}$. At the same time, successive approximation to find the C_B value that gives $\tau_1 = \tau_2$ will be performed on the other CDAC (C_B) . In this example, $\Phi_{B[13:0]}$ is set to 14'h2000 to start the binary search. On the other hand, if $R_2 > R_1$, $\Phi_{B[13:0]}$ is set to 14'h0000 for reference set up and $\Phi_{T[13:0]}$ is set to 14'h2000 to start the binary search. For every round, $\Phi_{T[13:0]}$ or $\Phi_{B[13:0]}$ is adjusted, and both C_1 and C_2 are discharged for the reset phase (Φ_{RST}) and then charged for the duration of t_{max} for the charging phase (Φ_{Charge}).

 V_1 and V_2 can be compared after charging to compare τ_1 and τ_2 to help determine the next $\Phi_{B[13]}$ configuration. For example, assuming $\Phi_{T[13:0]} = 14'h0000$ and $\Phi_{B[13:0]} = 14'h2000$ in the first SAR round, if $V_1 > V_2$, it implies $\tau_1 < \tau_2$, and the next $\Phi_{B[13:0]}$ should be 14'h1000. This SAR operation can be continued until the C_2 value that makes $\tau_1 = \tau_2$ is found. When $\tau_1 = \tau_2$ ($R_1 > R_2$), the value of C_2 is determined by the C_{Delay} and CDAC code (ΔC). The capacitance difference (ΔC) increases linearly with the resistance difference (ΔR). As a result, both ΔR and ΔC show a linear relationship to pressure.

The details of the HBDC timing diagram are shown in Fig. 4(b). At the start of each cycle, capacitors (C_1 and C_2) are reset through Φ_{RST} . Then, nonoverlapping Φ_{Charge} is asserted, so that the two signals do not overlap to avoid short-circuit current, and the capacitor is charged through the H-WhB. The

charged voltages of C_1 and C_2 (V_1 and V_2) are amplified with an AZ amplifier and then compared with a comparator. The comparator is a conventional two-stage clocked comparator that compares the amplified output at Φ_{COMP} . Comparison output (COMP) is then sent to a digital controller for 14b CDAC control.

During the initial charging phase, all capacitors, including C_{Delay} , CDAC, and parasitic capacitors, are pre-charged to a voltage close to 63.2% of VDD. This voltage is intentionally kept on unselected capacitors in the CDAC by disconnecting the switches before discharging them. By doing so, leakage current through the CDAC switches can be minimized and closely matched during the following evaluation steps. Without this scheme, if unselected capacitors are discharged, the switch transistor would face drain–source voltage (V_{ds}) of 63.2% of VDD, incurring large leakage after the charging phase. Such a pre-charging scheme helps minimizing potential error due to leakage mismatch. The simulation results shown in Fig. 5 confirm that the switch leakage current for unselected capacitors in the CDAC can be reduced up to 331.6× times with the pre-charging scheme.

C. Capacitor Bank

When designing a CDAC, a component of a typical successive approximation register (SAR) ADC, the capacity of the LSB capacitor is determined by considering the thermal noise of the capacitor. In conventional SAR-ADC structures,



Fig. 5. (a) Principle of switch leakage current reduction and (b) switch leakage current simulation in implementation of CDAC switch.



Fig. 6. Layout pattern of CDAC common-centroid and CDAC color chart.



D. AZ Amplifier and Dynamic Comparator

Amplifier offset voltage (V_{OS}) typically does not have a significant effect on the performance of HBDC. The primary impact of V_{OS} is a whole code shift, which can be easily corrected. However, V_{OS} drift can result in nonlinearity for HBDC in precise analog circuits. To address this issue, we utilize an AZ adjustment amplifier in each cycle, with an AZ capacitance (C_{AZ}) of 25 pF to reduce kT/C noise to below 12.6 μ V. The circuit details of the AZ amplifier and dynamic comparator are shown in Fig. 7(a) and (b), respectively, while Fig. 7(c) presents the opamp and dynamic comparator circuit layout.

Fig. 7(d) shows the V_{OS} drift simulation results. We obtained the average V_{OS} drift values using 5000 Monte-Carlo simulation samples across temperatures ranging from -40 °C to 120 °C, both with and without AZ. With AZ, the V_{OS} drift of the AZ amplifier demonstrates stable operation against temperature variations up to 216 nV, resulting in a code drift of up to 0.04 code. However, without AZ, the $V_{\rm OS}$ drift can reach up to 1.22 mV, leading to a significant code drift of up



E. Constant Parasitic Capacitance Switch (CPCS)

opamp offset voltage with and with autozeroing.

For the switch implementation in the CDAC, it is important to minimize the impact of parasitic capacitance. When conventional transmission gates (TG), which typically consist of an NMOS and a PMOS, are used for CDAC switches, the parasitic capacitances seen by the charging node can vary depending on the ON/OFF state of the switch, as shown in Fig. 8(a). The discrepancy in the number of parasitic channel capacitors (C_{CH}) and overlap capacitors (C_{OV}) seen by the charging node (node A in Fig. 8) can create nonlinearity on CDAC capacitance, which will ultimately result in pressure measurement accuracy degradation.

To minimize state-dependent parasitic capacitance variation, a constant parasitic capacitance switch (CPCS) scheme is adopted, as shown in Fig. 8(b). This scheme guarantees that the number of parasitic C_{CH} and C_{OV} between nodes A and B is always constant, regardless of the on/off status by using an identically sized dummy switch. Fig. 8(c) shows the simulation results confirming that the RC delay drift errors vary depending on the switch operation state between the CPCS and TG. The results are based on 5000 Monte-Carlo simulations at each point. A reference RC charging delay is set with the case, where all switches are in the OFF state in the CDAC under an ideal condition without device variation (non-Monte-Carlo case). To compare the RC charging delay as the number of turn-on switches increases, we calculate the RC charging delay using the time it takes to reach 63.2% of VDD. The RC delay error represents the extent to which the

and dynamic comparator layout, and (d) Monte-Carlo simulation results of

Voltage (V) 4m

6m

300

(a)

CAZ

OPAMP

(b)

Offset Shift =40.6 µV/°C



Fig. 8. Switch schematic of (a) conventional transmission gate switch, (b) proposed CPCS, and (c) average RC delay drift error according to the number of on/off switches (*5k Monte-Carlo simulation).

RC charge delay deviates from the reference RC charge delay, depending on the switch operation state. In other words, the larger the RC delay error, the more significant the deviation from the reference due to the parasitics of the switch.

When utilizing TG as CDAC switches, the *RC* delay escalates as the number of turned-on switches increases, as shown in Fig. 8(c), where the maximum *RC* delay drift error reaches 738.98 ppm. Conversely, when implementing CPCS for the CDAC switch, the variation in *RC* charging delay remains negligible, with a maximum variation of 29.74 ppm. Despite some errors, the disparity in *RC* delay drift error is up to 24.8 times higher with TG than the CPCS.

Due to the consistent parasitic capacitance, the switches can be sized up to lower the resistance. Due to the CPCS, high system linearity with an R^2 value of 0.99998 was obtained as a measurement result.

IV. ENERGY-EFFICIENT BOS

OS is a widely used technique for sensor interface circuits or ADCs, in which the measurement results are read multiple times and accumulated for improved accuracy/resolution. The proposed *RC*-delay-based HBDC can also benefit from OS, potentially improving IOP monitoring accuracy for better glaucoma diagnosis. However, OS increases the sensor system's energy consumption and measurement time. Therefore, the



Fig. 9. (a) Conventional OS operation. (b) Concept of the proposed BOS method and example operation.

level of resolution that can be achieved with OS is limited by the available energy and conversion time of the system.

Given this, an energy-efficient BOS technique is presented in this section that reduces the *RC* delay sampling noise and comparator noise in a more energy-efficient manner as compared to the conventional OS approach.

A. Conventional OS

Fig. 9(a) shows a conventional OS method widely used to suppress noise in sensor interfaces [22], [23]. With SAR-type sensor interfaces, OS is usually done by repeatedly performing successive approximations for all bits. The conventional OS method is a straightforward noise-removal technique that effectively improves the sensor resolution. This approach repeats the entire conversion process as many times as the OS ratio (OSR) and accumulates the output codes. With the OSR N, sensor resolution is improved by accumulating Nmeasurement results at the cost of N times higher energy consumption. When the process is repeated to get better resolution, conventional OS can require a large amount of energy consumption for a sensing system, which can potentially be a significant burden in a battery-operated miniature system.

B. Bit-Level OS (BOS)

Applying a conventional OS scheme in an energy-limited sensing system (e.g., battery-based implanted system) can potentially limit the amount of improvement that can be obtained due to the limited energy budget. If conventional OS is applied to the proposed HBDC, the entire SAR process needs to be repeated. However, it is clear that the probability of the output bit being flipped is very low at most significant bits (MSBs). Therefore, a BOS scheme is proposed to suppress the noise in the pressure sensor by repetitively evaluating bits with a high probability of error. Since the small form factor



Fig. 10. Details waveform of BOS conversion process using the majority voting system.

of the implantable miniature sensor system is limited with regard to the amount of energy it can consume, a balance must be found between energy consumption and resolution. The proposed BOS technique efficiently improves resolution by only repeating the bits that need to be oversampled, which is determined based on measurement data, rather than repeating the entire data conversion process. As a result, the same resolution can be achieved with much less energy consumption and a shorter conversion time.

Fig. 9(b) conceptually shows how the BOS is different from conventional OS: BOS is capable of setting the OSR differently for each bit, i.e., each bit can have a different bit-level OSR (BOSR). Since the number of iterations can be set per bit, efficient noise shaping is achieved by consuming more energy on noise-critical bits than on noise-insensitive bits to save energy by reducing the number of iterations. When the BOSR is larger than 1, majority voting is performed by the control logic to decide whether the current bit is 0 or 1.

Fig. 10 shows an example of a waveform illustrating the details of the BOS operation. The RC delay comparison, i.e., bit evaluation, is repeated four times for $\Phi_{[7]}$ versus eight times for $\Phi_{[6]}$ and $\Phi_{[5]}$. BOS logic accumulates the results of every RC-charging comparison to determine the bit value. When conducting the bit conversion process of $\Phi_{[N]}$, the result of the *RC* delay comparison is temporarily saved using Vote₀ and Vote₁ registers. If, for example, the RCdelay comparison result is 1 ($R_1C_1 < R_2C_2$), as shown in Fig. 10, BOS logic is to count up vote₁ and vice versa (count up Vote₀ for $R_1C_1 > R_2C_2$). After repeating the RC delay comparison as many times as the BOSR, we can obtain the *RC* delay comparison result (COMP_{Vote}) of the $\Phi_{[N]}$ with the result of obtaining majority voting between Vote₀ and Vote₁. The COMP_{Vote} signal determines the CDAC switch operation during the next clock cycle. The errors caused by noise are effectively suppressed through the majority voting process.

C. BOS Strategy

Since the BOSR can be adjusted for each bit, it is necessary to determine which bit needs to be oversampled more and which should be oversampled less.

The "probability of the first bit flip" in Fig. 11(a)–(e) refers to the probability of having the first bit error due to noise at a specific bit position during successive approximation operation of the CDAC from $\Phi_{[13]}$ to $\Phi_{[0]}$. For example, if the original data value is 14'h10011000100010 and the result is 14'10011000100100, it means that the first bit flip occurs at $\Phi_{[2]}$.

Upon examining the measurement results in Fig. 11(a) for the CDAC's first bit flip probability, it was observed that errors did not occur in the bit range of $\Phi_{[13]}-\Phi_{[8]}$, implying that these bits are not noise-critical. Consequently, bit evaluation for this range is carried out only once in the proposed BOSR strategy because of the low probability of bit flip. However, for bits lower than $\Phi_{[7]}$, where the likelihood of first flip bit errors becomes nonnegligible, a BOSR higher than 1 is utilized.

Fig. 11(a)-(e) shows the probability of CDAC first bit flip as the BOSR is increased from 1 (without OS) to BOSR = 32. We used these results to develop our BOSR strategy by increasing the BOSR in areas with a higher probability of bit flips. However, indiscriminately increasing the BOSR in regions with bit flips could lead to excessive energy consumption. Hence, we established a BOSR strategy that takes into account the tradeoff between energy-efficiency and resolution, incrementing the BOSR value accordingly.

Fig. 11(a) depicts the probability distribution of the first bit flips, which are concentrated in the bit range of $\Phi_{[7]}-\Phi_{[0]}$ at pressure levels of 700, 750, 800, and 850 mm Hg. Based on this observation, the BOSR strategy in BOSR = 4 increased the BOSR values for the bit range of $\Phi_{[7]}-\Phi_{[0]}$, as presented in Fig. 11(g). Moreover, the BOSR32 column of Fig. 11(g) assigned the highest BOSR value to $\Phi_{[3]}$ due to the high probability of CDAC first bit flip at $\Phi_{[3]}$ in BOSR = 16, as shown in Fig. 11(d).

Fig. 11(f) shows the distribution of the pressure code measured with the proposed HBDC, where 25k samples were obtained with five different BOSR strategies, as shown in Fig. 11(g). The *Y*-axis of this figure represents the magnitude of error between the ideal value and measured value (code), and the color of each data point represents in which bit position the first bit flip occurred. For instance, if the original value is 14'h10011000100010 and the result is 14'h10011000100100, the CDAC first bit flip occurs at $\Phi_{[2]}$, with an error amount of 2.

By using the newly proposed BOS, the noise of selected bits can be effectively suppressed. The BOSR strategy also reduces conversion time and energy consumption by up to 88% while



Fig. 11. Measured distribution of probability for CDAC first bit flip with a BOS rate of (a) BOSR = 1 (without BOS), (b) BOSR = 4, (c) BOSR = 8, (d) BOSR = 16, (e) BOSR = 32, and (f) pressure data error distribution of 25k sample measurement data with a BOS strategy for a BOSR of 1–32. (g) Details of the BOSR numbers of the proposed BOS ratio strategy.



Fig. 12. (a) HBDC and pressure sensor die micrograph and system specification. (b) Measurement setup with pressure control system.

achieving the same resolution compared to conventional OS approaches.

V. MEASUREMENT RESULTS

A test chip for the proposed HBDC was fabricated in 180-nm CMOS process. The pressure sensor used for the evaluation was a piezo-resistive H-WhB (NovaSensor P330). Fig. 12(a) shows the micrograph and specification of the HBDC and H-WhB. To minimize the difference in parasitic components between the HBDC and H-WhB, the wires of the same length are used, and the H-WhB sensor was stacked on the HBDC. Furthermore, the use of an H-WhB allowed us to keep the volume small, and the height of the H-WhB and HBDC stack is 0.48 mm, which does not exceed the 0.5 mm limit even with stacking. The pressure measurement environment is shown in Fig. 12(b). The HBDC was measured in a precision pressure controller (GE PACE5000) and a

stainless steel pressure chamber to eliminate electromagnetic interference.

A. RC Charging Margin Time for t_{max}

The impact of *RC* charging time (T_{Charge}) variation on the resolution of the system is evaluated by sweeping T_{Charge} from 68% to 145% of a pre-programmed time t_{max} . The reference *RC* charging period (t_{max}) is determined as the *RC* charging time to reach 63.2% of VDD, which is externally measured through the test buffer, i.e., set as time constant of the *RC* network. For the tested chip, the absolute value of t_{max} is 3 μ s at 760 mmHg, as shown in Fig. 13(a). The measurement results indicate that the HBDC resolution remains consistent across a wide range of T_{Charge} values. Furthermore, we observe no significant decrease in resolution from 73% to 139% of t_{max} , and negligible differences are detected for 90%–120% of t_{max} , thereby ensuring robust operation with T_{Charge} fluctuations.



Fig. 13. Measurement results. (a) Pressure sensing resolution over a range of T_{Charge} values. (b) HBDC system linearity.



Fig. 14. Measurement results of system resolution. (a) Resolution of HBDC in pressure range 700–850 mmHg according to BOS strategy. (b) Comparison of HBDC resolution according to conversion time between BOS and OS according to OS ratio (or BOSR).

B. Linearity

The measurement results in Fig. 13(b) demonstrate that the proposed HBDC exhibits a high degree of linearity, with an R_2 value of 0.99998 for the pressure range of 500–1000 mmHg. The pressure was measured at 1-mmHg intervals from 500 to 1000 mmHg, and an average of 200 samples per point were taken. The results shown in Fig. 13(b) were obtained without calibration process—due to the high linearity of the pressure transducer, common-centroid layout matching, and CPCS, high system linearity could be achieved.

C. Resolution and FoM

Fig. 14(a) shows the measurement result of the HBDC resolution using a BOS strategy with a BOSR of 1–32 in order to confirm the improvement in resolution as the BOSR increases in the pressure range of 700–850 mmHg. As glaucoma can occur when the IOP is 21 mmHg or higher in a normal state, measurement was performed in a sufficient pressure range of 700–850 mmHg, considering the external environment and physical movement of a human body. The results showed that a BOSR of 4 achieved 0.24-mmHg resolution with 11.52-ms conversion time, which is equivalent to the time it would take for 2.4 full evaluations using the conventional OS methods.

Due to BOS, the conversion time (and hence the energy consumption) required to achieve the same target resolution is reduced by 40% with a BOSR of 4 (compared with conventional OS of 4) and by 88% with a BOSR of 256 (compared with conventional OS of 256), as shown in Fig. 14(b). Overall, the proposed energy-efficient BOS enables a reduction in energy consumption and conversion time while using the low sensitivity of the H-WhB. As a result, the HBDC has a resolution FoM of 20.79 nJ·mmHg².

D. System Inaccuracy

The measurement result in Fig. 15(a) shows that the inaccuracy of the HBDC for 15 chips is ± 1.04 mmHg (3 σ) after two-point calibration in a pressure range of 500–1000 mmHg. The two-point calibration was performed at 600 and 900 mmHg.

E. Supply Voltage Sensitivity

The supply sensitivity of HBDC is characterized in the range of 1.6–1.9 V and 500–1000 mmHg for three chips, as shown in Fig. 15(b). The measurement results show that a code shift value of 0.02 mmHg/mV in the range of 1.6–1.9 V can be easily corrected after the first-order compensation. The maximum supply sensitivity error is -0.78/0.88 mmHg.



Fig. 15. Measurement results of system sensitivity to process/supply voltage/temperature variations. (a) Pressure measurement error for 15 chips with two-point calibration, (b) pressure measurement error with supply voltage variation, and (c) pressure measurement error with temperature variation with the first-order compensation.

TABLE I	
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR	Arts

v	This v/o BOSR	Work w/ BOSR = 4	ISSCC2017 H. Bhamra [26]	VLS12020 S. Jeong [22]	ISSCC2018 S. Oh [23]	Sens.J2014 T. T. Nguyen [24]	JSSC2018 M. J. Weber [25]
Technology (nm)	1	80	180	180	180	90	180
Sensor Read Voltage (V)]	.8	1.35	3.6	3.6	1	1.94
Power (µW)	12	.79	35.6	8.52	2.65	52	100 ^d
Sensor Type	Half	WhB	Half-WhB	WhB	WhB	WhB	WhB
Glaucoma Implantable	١	es	Yes	No	No	No	No
Pressure Sensor Size (mm) (Volume)	0.9×0. (0.05	0.9×0.33×0.18 (0.05mm ³)		$1 \times 1 \times 0.4$ (0.4mm ³)	$1 \times 1 \times 0.4$ (0.4mm ³)	$2 \times 2.5 \times 1.5$ (6.66mm ³)	NR
Pressure Sensor Sensitivity (μV/V/mmHg)		10	11	20	20	17	30
Conversion Time (ms)	4.80	11.52	233	10	4	0.096	1 ^d
Energy/Conversion (nJ/Conv)	61.4	147.4	8290	85.2	10.6	5	100
Resolution (mmHg, 1o)	0.44 ^a	0.24 ^a	0.67	0.3	1.1	11.4	0.78 ^c
Resolution FOM (nJ [·] mmHg ²)	11.97	8.58	3721.38	7.67	12.83	649.80	60.84 ^d
Oversampling	No	Yes (BOSR=4)	NR	Yes (OSR = 8)	Yes (OSR = 4)	NR	NR
Effective Oversampling Ratio ^e	1	2.4	NR	8	4	NR	NR
Inaccuracy (mmHg) (Number of Samples)	±] (l.04 ^f 15)	0.81 (1)	±0.75 ^f (24)	NR	NR	0.34 ^g (1)
Supply Voltage Sensitivity (mmHg)	-0.78	-0.78/+0.88		NR	-0.4/+0.3	NR	NR
Temperature Sensitivity (mmHg, Temperature Range)	-0.3/ (15 -	-0.3/+0.13 ^h (15 - 45°C)		-0.5/+0.6 (0 - 85°C)	NR	NR	NR
Pressure Range (mmHg)	500	500-1000		90-900	100-900	0-1500	400-1200
^a Average of 700–850mmHg Resolu ^g From 620–1070mmHg	tion ^b Gauge pres ^h Manufactur	^b Gauge pressure Range ^c mmHg/LSB ^d Include Ultrasonic data upink ^e Total # of bit evaluation / # of output bit ^b Manufacturer provided operating temp - Resolution FOME Energy/Conv. (Resolution) ² *NR - Not reported					

F. Temperature Sensitivity

The HBDC was characterized in a temperature-controlled chamber (Vötsch VT4004) from 15 °C to 45 °C, which is the operating temperature range provided by the manufacturer for the H-WhB. As shown in Fig. 15(c), the measured HBDC temperature performance at a pressure of 760 mmHg exhibits stable operation over 15 °C–45 °C with a maximum temperature-induced error of -0.3/+0.13 mmHg after individual first-order compensation for the innate temperature dependence of the H-WhB.

G. Power Breakdown

As depicted in Fig. 16, the total conversion power consumption of the HBDC is 12.79 μ W at a conversion time of 11.52 ms. The H-WhB resistance conduction loss and C_{Delay} switching loss are the major contributors to power consumption, accounting for 77.27% of the total power consumption. For accurate comparison of *RC* delays, the AZ amplifier consumes 17.36% of the power. Among the remaining components, the digital controller consumes 5.21% of the power, the CDAC switching loss consumes 0.16%, and the comparator consumes the rest.

H. Comparison to Pervious Work

Table I summarizes the measured performance of the proposed HBDC and compares it with recent prior-art pressure sensors. This work achieved significantly better performance compared to the prior H-WhB-based pressure sensor [26]; the system power consumption has been reduced by $2.8\times$, the energy consumption has been reduced by $56.24\times$, and the resolution has been improved by $2.8\times$. Fig. 17 compares the performance of this work to other pressure sensors [22], [23], [24], [25], [26], including capacitive pressure sensors. This work has overcome the low sensitivity of an



Total Power = 12.79 µW

Fig. 16. Power breakdown.



Fig. 17. Performance benchmark of the state-of-the-art pressure sensors.

H-WhB with small volume, resulting in an FoM comparable to the state-of-the-art sensors based on WhBs. It also achieved the finest resolution among H-WhB-based sensors.

VI. CONCLUSION

An RC delay-based HBDC with energy-efficient BOS and high-precision resolution has been proposed for use in an implantable IOP monitoring system with 1.8-V low sensor read voltage for low-power operation. The proposed HBDC achieved significantly better performance than the prior H-WhB-based pressure sensor, overcoming the limitations associated with this type of sensor to achieve an FOM comparable to those of WhB-based pressure sensors. To overcome the inferior sensitivity of the H-WhB, the use of an RC delaybased readout circuit and an energy-efficient BOS scheme was adopted, which significantly improves resolution compared to prior H-WhB-based pressure sensors and is comparable to the state-of-the-art WhB pressure sensors. Together, these proposed techniques create an ultralow power sensor platform, opening up new opportunities for future implantable miniature sensor system applications.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

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