YI SHEN

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INTERESTS

Wireless transceiver and mixed-signal VLSI circuit system.

EDUCATION

University of Michigan - Ann Arbor *Ann Arbor MI, US*
PhD Electrical & Computer Engineering - IC & VLSI *09/2023 - Present*
Advisor: Prof. David Blaauw

University of Michigan - Ann Arbor *Ann Arbor MI, US*
MS Electrical & Computer Engineering - IC & VLSI *08/2022 - Present*
GPA: 4.3/4.0

University of Liverpool *Liverpool, UK*
Xi'an Jiaotong-Liverpool University (XJTLU) *Suzhou, China*
BEng (Hons) Electronics Science and Technology (Joint Degree) *09/2018 - 07/2022*
First-class (Honors) Degree, Department Ranking: 1/233
GPA: 3.93/4.0 (Major 4.0/4.0)

EXPERIENCE

Michigan Integrated Circuits Laboratory (MICL) Ann Arbor MI, US
Graduate Student Research Assistant (GSRA) *02/2023 - Present*

· RF & Mixed-signal IC design. (Supervisor: Prof. David Blaauw)

Ravsense Microelectronics Co, Ltd. Suzhou, China
IC Design Intern *03/2022 - 08/2022*

· Developed a 60-64 GHz mm-Wave FMCW bio-radar Transceiver IC for human health monitoring.
  – Designed and optimized 3rd-order MASH ΣΔ Fractional-N PLL, including VCO, Frequency Divider (IJL/CML/digital), PFD and Charge Pump.
  – Designed and optimized Tx chain including the Frequency Doubler, Mixer, and PA.

Suzhou Municipal Key Laboratory for New Energy Techniques Suzhou, China
Undergraduate Research Assistant *09/2020 - 05/2022*

· Developed various blocks of all-GaN smart power IC (PMIC)
  – Designed voltage reference, PWM Controller, DC-DC Converter, and over-temp protection block.
  – Achieved a high-temperature (up to 250°C) and high-voltage (up to 100V) operation.
· Designed and characterized several GaN HEMTs structures
  – Experienced in device characterization and reliability investigation (NBTI, PBTI, TDDB).
  – Fabricated IC/device in the clean room, familiar with the processes and devices physics.

ACDAMIC PUBLICATIONS

[1] **Y. Shen**, Z. Li, A. Li, W. Liu, "Monolithically Integrated PWM Circuit Based on AlGaN/GaN MIS-HEMTs for All-GaN Smart Power System", IEEE 14th International Conference on ASIC (ASICON), 2021.

[2] A. Li, **Y. Shen**, Z. Li, R. Sun, I. Z. Mitrovic, H. Wen, S. Lam, and W. Liu, "A 4-Transistor Monolithic Solution to Highly Linear On-chip Temperature Sensing in GaN Power Integrated Circuits," in IEEE Electron Device Letters, Early Access, Dec. 2022. (JCR Q1, IF = 4.816)

[3] A. Li, **Y. Shen**, Z. Li, Y. Zhao, I. Z. Mitrovic, H. Wen, S. Lam, and W. Liu, "A Monolithically Integrated 2-Transistor Voltage Reference with a Wide Temperature Range Based on AlGaN/GaN Technology," IEEE Electron Device Letters, vol. 43, no. 3, pp. 362-365, March 2022. (JCR Q1, IF = 4.816)

[4] A. Li, M. Cui, **Y. Shen**, Z. Li, W. Liu, I. Z. Mitrovic, H. Wen, and C. Zhao, "Monolithic Comparator and Sawtooth Generator of AlGaN/GaN MIS-HEMTs With Threshold Voltage Modulation for High-Temperature Applications," IEEE Transactions on Electron Devices, vol. 68, no. 6, pp. 2673-2679, June 2021. (JCR Q2, IF = 3.221)

[5] Z. Li, **Y. Shen**, A. Li and W. Liu, "A 5 to 50 V, -25 to 225 °C, 0.065%/°C GaN MIS-HEMT Monolithic Compact 2T Voltage Reference," IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), 2022.

SELECTED COURSE PROJECTS

CNN Accelerator Chip with PLL & LDO for DVFS Ann Arbor MI, US
EECS627 VLSI Design II | Instructor: Prof. David Blaauw *23 Winter*

- Designed a Type-II analog PLL and a programmable LDO for dynamic voltage & frequency scaling, PLL supports 20MHz to 200MHz output frequency under 0.48 mW. LDO has a max output power of 80 mW, V_{out} range of 0.7 V-1.28 V, -45 dB PSRR, and 99.3% current efficiency.
- Implemented block and top-level APR. Floor planed and integrated SRAM, digital and analog block with power grids and pad rings. The final design is tape-out-ready.

Low-Power High Precision ADC with 2nd-order $\Sigma\Delta$ Noise-Shaping Ann Arbor MI, US
EECS413 Intro to Analog & Mixed Signal Design | Instructor: Prof. Ehsan Afshari *22 Fall*

- Designed a 2nd-order DSM ADC with a 4-bit SAR quantizer in IBM 0.13μm CMOS, achieved an SNDR of 96.7 dB and ENOB of 15.77 bits under 0.5 mW power consumption.
- Designed a 2-stage high-gain Telescope OTA with Switched-Capacitor CMFB for DSM loop filter.

TECHNICAL STRENGTHS

Analog/RF Circuit Design & Modeling	Cadence Virtuoso, Keysight ADS, CppSim
Digital & Physical Design	Synopsys DC/Verdi/PrimeTime, Cadence Innovus
Programming Skills	System Verilog, Python, C/C++, MATLAB, Tcl

HONORS & AWARDS

IET Prize for the most outstanding graduate student in the department (1/233) *07/2022*
Best Overall Academic Performance (1/50), Best Final Year Project (1/50) *07/2022*
XJTLU Academic Excellence Award (Top5%) *08/2021 & 08/2020*
XJTLU Academic Achievement Award (Top10%) *08/2019*

RELEVANT COURSEWORK

Analog (RF) ICs [A+] (Prof. David Wentzloff), High-performance VLSI [A+] (Prof. David Blaauw),
VLSI Design I [A+] (Prof. David Blaauw), VLSI Design II [A+] (Prof. David Blaauw),
Intro to Analog & Mixed Signal Design [A+] (Prof. Ehsan Afshari),
Advanced Analog & Mixed-Signal IC - PLL [A+] (Prof. Mike Flynn),
VLSI for ML & Communication [A] (Prof. Hun Seok Kim).