Jungho Lee

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EDUCATION

University of Michigan — Ann Arbor, MI
Ph.D. in Electrical Engineering and Computer Science — *Aug. 2020 – Present*
- Advisor: Prof. David Blaauw

POSTECH (Pohang University of Science and Technology) — Pohang, Republic of Korea
M.S. in Electrical Engineering — *Mar. 2018 – Feb. 2020*
- Advisor: Prof. Jae-Yoon Sim, GPA: 4.20/4.3

POSTECH (Pohang University of Science and Technology) — Pohang, Republic of Korea
B.S. in Electrical Engineering — *Mar. 2012 – Feb. 2018*
- Graduated 1st in College of Engineering, GPA: 4.14/4.3, *summa cum laude*
- Two-year absence for military service, 2014-2016

EXPERIENCE

Graduate Research Assistant — Aug. 2020 – Present
Michigan Integrated Circuits Laboratory (MICL), University of Michigan
- Designed sub-mm wireless Neural Stimulator IC chip for Visual Cortical Prosthesis (VCP) for vision restoration
- Designed sub-mm Micro-Robot IC chip with energy harvesting, sensing, processing, communication, and actuation
- Contributed to sub-mm wireless Neural Recorder IC for signal probe and on-chip spiking-band-power (SBP) calculation
- Verified chips optically by Near-Infrared (NIR) laser diode modulation, and bio-medically by *in vivo* rat test

Graduate Research Assistant — Jan. 2018 – Aug. 2020
Analog IC Systmes Lab, POSTECH
- Designed Neuromorphic IC chip with Analog-domain Multiplication-and-Accumulation (MAC) processor
- Designed on-chip Machine Learning algorithm to classify handwritten digits using MNIST database
- Developed FPGA-based evaluation setup for on-chip learning and real-time handwriting recognition demonstration
- Proposed epileptic seizure detection algorithm based on Unsupervised Machine Learning using Restricted Boltzmann Machine
- Designed signal process and feature generation method for neuromorphic chip using CHB-MIT electroencephalogram (EEG) data

Undergraduate Research Assistant — Sept. 2016 – Nov. 2017
Analog IC Systmes Lab, POSTECH
- Designed a nano-watt Bandgap Reference (BGR) generator and Phase-Locked Loop (PLL) circuits
- Funded by the university Undergraduate Research Program (URP) and earned Best Paper Award among 20 program beneficiaries

PUBLICATIONS

- **J. Lee**, J. Letner, J. Lim, G. Atzeni, J. Liao, A. Kamboj, B. Mani, S. Jeong, Y. Kim, Y. Sun, B. Koo, J. Richie, E. della Valle, P. Patel, D. Sylvester, H. Kim, T. Jang, J. Phillips, C. Chestek, J. Weiland, D. Blaauw, "**A Sub-mm^3 Wireless Neural Stimulator IC for Visual Cortical Prosthesis With Optical Power Harvesting and 7.5-kb/s Data Telemetry**," *IEEE Journal of Solid-State Circuits*, Apr. 2024.
- **J. Lee**, J. Letner, J. Lim, Y. Sun, S. Jeong, Y. Kim, B. Koo, G. Atzeni, J. Liao, J. Richie, E. della Valle, P. Patel, T. Jang, C. Chestek, J. Phillips, J. Weiland, D. Sylvester, H. Kim, D. Blaauw, "**A Wireless Neural Stimulator IC for Cortical Visual Prosthesis**," *IEEE Symposium on VLSI Technology and Circuits (VLSI)*, Jun. 2023.
- G. Atzeni, J. Lim, J. Liao, A. Novello, **J. Lee**, E. Moon, M. Barrow, J. Letner, J. Costello, S. Nason, P. Patel, P. Patil, H.-S. Kim, C. Chestek, J. Phillips, D. Blaauw, T. Jang, "**A 260×274 μm^2 572 nW Neural Recording Micromote Using Near-Infrared Power Transfer and an RF Data Uplink**," *IEEE Symposium on VLSI Technology and Circuits (VLSI)*, Jun. 2022.
- J. Costello, S. Nason, H. An, **J. Lee**, M. Mender, H. Temmar, D. Wallace, J. Lim, M. Willsey, P. Patil, T. Jang, J. Phillips, H.-S. Kim, D. Blaauw, C. Chestek, "**A low-power communication scheme for wireless, 1000 channel brain–machine interfaces**," *Journal of Neural Engineering*, Jun. 2022.
- Y. Sun, J. Letner, **J. Lee**, N. Ahmed, C. Chestek, D. Blaauw, J. Phillips, "**GaAs-Based Photovoltaic Infrared Energy Harvesting for Microscale Biomedical Implants**," *IEEE Photovoltaic Specialists Conference (PVSC)*, Jun. 2022.
- J. Lim, **J. Lee**, E. Moon, M. Barrow, G. Atzeni, J. Letner, J. Costello, S. Nason, P. Patel, Y. Sun, P. Patil, H.-S. Kim, C. Chestek, J. Phillips, D. Blaauw, D. Sylvester, T. Jang, "**A Light-Tolerant Wireless Neural Recording IC for Motor Prediction With Near-Infrared-Based Power and Data Telemetry**," *IEEE Journal of Solid-State Circuits*, Apr. 2022.
- R. Rothe, M. Cho, K. Choo, S. Jeong, S. Oh, **J. Lee**, D. Sylvester, D. Blaauw, "**A Delta Sigma-Modulated Sample and Average Common-Mode Feedback Technique for Capacitively Coupled Amplifiers in a 192-nW Acoustic Analog Front-End**," *IEEE Journal of Solid-State Circuits*, Apr. 2022.
- L. Xu, M. Lassiter, X. Wu, Y. Kim, **J. Lee**, M. Yasuda, M. Kawaminami, M. Miskin, D. Blaauw, D. Sylvester, "**A 210×340×50μm Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation**," *IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2022.

- J. Lim, **J. Lee**, E. Moon, M. Barrow, G. Atzeni, J. Letner, J. Costello, S. R. Nason, P. R. Patel, P. G. Patil, H.-S. Kim, C. A. Chestek, J. Phillips, D. Blaauw, D. Sylvester, T. Jang, "**A Light Tolerant Neural Recording IC for Near-Infrared-Powered Free Floating Motes**," *Symposium on VLSI Circuits (VLSI)*, Jun. 2021. (invited to *JSSC*)
- E. Moon, M. Barrow, J. Lim, **J. Lee**, S. R. Nason, J. Costello, H. Kim, C. Chestek, T. Jang, D. Blaauw, J. Phillips, "**Bridging the "Last Millimeter" Gap of Brain-Machine Interfaces via Near-Infrared Wireless Power Transfer and Data Communications**," *ACS Photonics*, May. 2021.
- Y. Ji, **J. Lee**, B. Kim, H.-J. Park, J.-Y. Sim, "**A 192-pW Voltage Reference Generating Bandgap-V_{th} With Process and Temperature Dependence Compensation**," *IEEE Journal of Solid-State Circuits*, Dec. 2019.
- H. Son, H. Cho, **J. Lee**, S. Bae, B. Kim, H.-J. Park, J.-Y. Sim, "**A Multilayer-Learning Current-Mode Neuromorphic System With Analog-Error Compensation**," *IEEE Transactions on Biomedical Circuits and Systems*, Oct. 2019.
- Y. Ji, **J. Lee**, B. Kim, H.-J. Park, and J.-Y. Sim, "**A 192pW Hybrid Bandgap-V_{th} Reference with Process Dependence Compensated by a Dimension-Induced Side-Effect**," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2019. (invited to *JSSC*)

Technical Skills

Languages	: Python, MATLAB, SPICE, Verilog, Verilog-A, Tcl, Assembly, C, C++, C#, CUDA, LaTeX
CAD Tools	: Cadence Virtuoso/Innovus, Synopsys Design Compiler/IC Complier, Xilinx Vivado
Simulators	: HSpice, Spectre, CustomSim, FineSim, VCS, Incisive, AMS
Developer Tools	: Vim, VS Code, Visual Studio, Juyter Notebook, Git
Operating Systems	: Linux RedHat/CentOS/Ubuntu, Windows, Android, iOS

Awards and Honors

Best Teaching Assistant Award | Department of Electrical Engineering, POSTECH — Sept. 2018
- Awarded as the best TA of Spring 2018 for teaching *Electronic Circuits I* and *Introductory Experiments on Electronics*

Graduated 1st rank | College of Engineering, POSTECH — Feb. 2018
- Awarded as the highest GPA among B.S. graduates of engineering disciplines and won a gold medal

Best Paper Award | Undergraduate Research Program, POSTECH — Dec. 2017
- Awarded for excellent research in Prof. J.-Y. Sim's Analog IC Systems Lab and its paper

Scholarships

Kwanjeong Educational Foundation Scholarship — 2014 – 2017
- Selected as a future global leader, and awarded full tuition with living expenses for 4 semesters

GE Foundation Scholar-Leaders Award and Scholarship — 2013 – 2017
- Combined global affiliation of General Electric (GE) Foundation, Fulbright, and Institute of International Education
- Selected as one of 6 future leaders in natural science and engineering in S. Korea and awarded scholarship for 6 semesters

The National Scholarship for Science and Engineering — 2012 – 2013
- Selected as an undergraduate with strong academic performance in engineering, awarded full tuition for 4 semesters

Teaching

Teaching Assistant | Department of Electrical Engineering, POSTECH
- *Electronic Circuits I* and *Introductory Experiments on Electronics* — Spring 2018

Undergraduate Tutor | Department of Electrical Engineering, POSTECH
- *Electronic Circuits I* — Spring 2017

After-school Class Teacher | Samsung Dream Class Project
- Middle-School Mathematics — Spring 2017

Freshmen Tutoring Program | Samsung Dream Class Project
- *Applied Linear Algebra* — Fall 2017
- *Programming and Problem Solving* — Spring 2014

Extracurricular Activities

Internship | DRAM Core Design Team, SK Hynix — Jun. 2018 – Jul. 2018

Military Service | Intelligence & Signal Corps, The 25th Infantry Division, S. Korea — Sept. 2014 – Jun. 2016