PARIN SENTA

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EDUCATION

University of Michigan **Ann Arbor, MI**
Master of Science in Electrical and Computer Engineering, IC & VLSI *April 2025*
GPA: **4.00/4.00**
Coursework: EECS 470: Computer Architecture (A+), EECS 570: Parallel Computer Architecture (A+), EECS 598: VLSI for Machine Learning & Communication, EECS 498: Quantum Programming (A+)

Indian Institute of Technology Bombay (IIT Bombay) **Mumbai, India**
Bachelor of Technology in Electrical Engineering & Minor in Computer Science *August 2023*
GPA: **9.45/10.00**

WORK EXPERIENCE

Qualcomm **Bengaluru, India**
Hardware Engineering Intern *May 2022 – July 2022*

- Automated hierarchy generation of Hard Macros (HM) of any specified chip using Python to correct its die area as part of the SoC Synthesis Team, reducing 15+ person hours for the task
- Showcased the hierarchy as an interactive HTML table to analyze variations in chip area due to changes in the instance count of HMs, particularly helpful in the area estimation of a derived chip

Defense Research & Development Organization (DRDO), Govt. of India **Delhi, India**
Research Intern *Dec 2021 – Jan 2022*

- Explored the process of modelling and simulating junction devices to examine their electrical properties
- Designed and simulated InGaAs PIN diode using Silvaco TCAD to test the effect of lateral temperature gradient at cryogenic temperatures on charge transport

PROJECT EXPERIENCE

University of Michigan **Ann Arbor, MI**
N-way MIPS R10k-Style Out-of-Order Singe-Core Processor in SystemVerilog *Aug 2023 – Dec 2023*

- Designed, tested, and synthesized an N-way Superscalar CPU with RISC-V RV32IM ISA, using Synopsys VCS & DC
- Key Features: Early Tag Broadcast, Store to Load Forwarding, Non-Blocking D-cache, Gshare Predictor, Return Address Stack, Instruction Prefetching, Mult-Banked Reorder Buffer, Pipelined Functional Units, Victim Cache
- Attained average cycles per instruction (CPI) of 1.10 (best among 98 students) and clock period of 20 ns for N=4, and passed all test programs for N = 2,3,4,5 and 8.

D-CNN: Dilated Convolution Neural Network Accelerator *Aug 2023 – Dec 2023*

- Implemented a systolic array-based accelerator for 3-D dilated convolution (D-conv) capable of input and kernel folding
- Incorporated delay cells – array of shift registers – to speed up D-conv by skipping redundant zero computations
- Synthesized the accelerator using 32 nm CMOS technology, at 100 MHz frequency and convolution power of 6 mW

Indian Institute of Technology Bombay **Mumbai, India**
Selective Out-of-Order (OoO) Warp Scheduling in GP-GPUs *July 2022 – Dec 2022*

- Reviewed literature on warp-scheduling and compiler-assisted OoO scheduling of instructions during stall cycles to explore ways to improve the performance of GPU through dynamic scheduling
- Devised a novel strategy that considers instructions with false data dependencies as valid candidates for OoO scheduling, incurring hardware overhead of only 4 extra registers
- Implemented two rounds of OoO warp scheduling and simulated benchmark suites from NVIDIA SDK on GPGPUSim - a cycle-accurate simulator, obtaining performance gain of 12% over baseline

TECHNICAL SKILLS

Programming: System Verilog | C++ | Python | VHDL | Latex | Matlab | C | Embedded C | Assembly | HTML | Rust
Software: Synopsys VCS & DC | Quartus | Git | LTSpice | Sentaurus TCAD | Arduino IDE | Keil | SolidWorks

ACADEMIC ACHIEVEMENTS & LEADERSHIP EXPERIENCE

- Jee Advanced 2019: All-India Rank 105 out of 170,000 | JEE Mains 2019: All-India Rank 219 out of 1,000,000
- Undergraduate Teaching Assistant, Media and Marketing Coordinator for Techfest - Footfall = 175,000+